AIR FORCE T.O. 31W2-2GSC24-2
ARMY TM 11-5805-688-14-1
NAVY NAVELEX 0967-LP-545-3010

TECHNICAL MANUAL

SERVICE AND MAINTENANCE INSTRUCTIONS

AN/GSC-24(V) MULTIPLEXER SET

MARTIN MARIETTA AEROSPACE
ORLANDO DIVISION
COMMUNICATIONS AND ELECTRONICS

Contract Number
F30602-75-C-0009

This is a reprint which includes current pages from Changes 1 and 2.

Published under authority of the Secretary of the Air Force, under authority of the Secretary of the Army, and by direction of Commander, Naval Electronics Systems Command.

1 JANUARY 1976

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INTRODUCTION

This manual contains the combined service and maintenance instructions necessary for servicing and maintaining the AN/GSC-24(V) multiplexer set in an operationally ready condition. The multiplexer set is a versatile asynchronous time-division multiplexer that can be configured for simplex or full-duplex operation. Up to 15 channels of voice data, high-speed and low-speed digital data with timing, and/or selected low-speed digital data without timing can be multiplexed and demultiplexed in the multiplexer set. The technical capabilities of the multiplexer set are listed in chapter 1.

This manual is divided into six chapters. Chapter 1 contains descriptive information, operating parameters, and other pertinent data by which service personnel can familiarize themselves with the multiplexer set. The installation logistics considerations and installation procedures are in chapter 2. Chapter 3 contains the procedures for making the equipment operational, as well as the procedures for preparing the equipment for reshipment. Chapter 4 contains the operating procedures and associated information required to ensure that the equipment performs its designated functions. The theory of operation is in Chapter 5. Chapter 6 prescribes the maintenance instructions that maintenance personnel require for servicing the equipment. The circuit diagrams (schematic, logic, and wiring) for the equipment are in the circuit diagrams manual.

Nonstandard symbols and abbreviations appearing in this manual are defined at their first appearance. Standard symbols and abbreviations appearing in this manual are defined in the appropriate Military Standards as referenced in the following technical content specification that was used in the preparation of this manual: MIL-M-38798A - Manuals, Technical: Operation Instructions, Maintenance Instructions, Circuit Diagrams, Alignment Procedures, and Installation Planning.

CHAPTER 1

GENERAL INFORMATION

1-1. DESCRIPTION AND PURPOSE.

1-2. The AN/GSC-24(V) multiplexer set provides asynchronous time division multiplexing and demultiplexing capabilities in digital transmission networks. The multiplexing function accepts up to 15 channels of various lower rate digital input streams and interleaves them into a single high-speed digital stream output. In turn, the demultiplexing function accepts a high-speed digital stream and separates the digital stream input into a given number (up to 15) of lower rate digital streams. The multiplexer set provides full duplex operation, performing independent and simultaneous multiplexing and demultiplexing functions.

NOTE

In this manual, the circuits are divided into one of three functional groups. The circuits that perform the multiplexing function are referred to as the multiplexer. The circuits that perform the demultiplexing function are referred to as the demultiplexer. The circuits that perform the power supply function are referred to as the power supply.

1-3. The multiplexer set also has the following unique capabilities:

a. Voice data and digital data, supplied with and without timing, can be processed and multiplexed in the multiplexer set by the use of optional plug-in cards.

b. Automatic diagnostic circuits in the multiplexer set provide visual indications of error conditions and their probable causes. The diagnostic circuits also produce associated electrical alarm signals that can be transmitted to a remote facility for monitoring purposes.

c. The multiplexer set acquires frame synchronization and maintains bit count integrity on all channels while accepting input data whose bit rates can vary within prescribed limits. Also, the multiplexer set automatically determines when an out-of-frame (synchronization) condition exists in the data message. When in an out-of-frame condition, the equipment automatically and continuously attempts to reacquire frame synchronization. The reacquisition of frame synchronization is automatically accomplished when the cause of an out-of-frame condition is removed.

d. In the multiplexer, the overhead data required for the proper operation of the far-end demultiplexer are automatically generated and transmitted in the multiplexer high-speed digital stream output. The demultiplexer, in turn, automatically decodes and uses the overhead data to maintain bit count integrity.

1-4. As shown in figure 1-1, the multiplexer set is contained in a ruggedized aluminum chassis that is suitable for mounting in a standard relay rack. When the unit is rack mounted, slide assemblies on each side of the chassis allow it to be extended from the rack for maintenance purposes. When fully extended on the slides, the chassis can be tilted up or down and locked in position at an angle of 45° or 90°. The functional circuits, less the power supply, in the

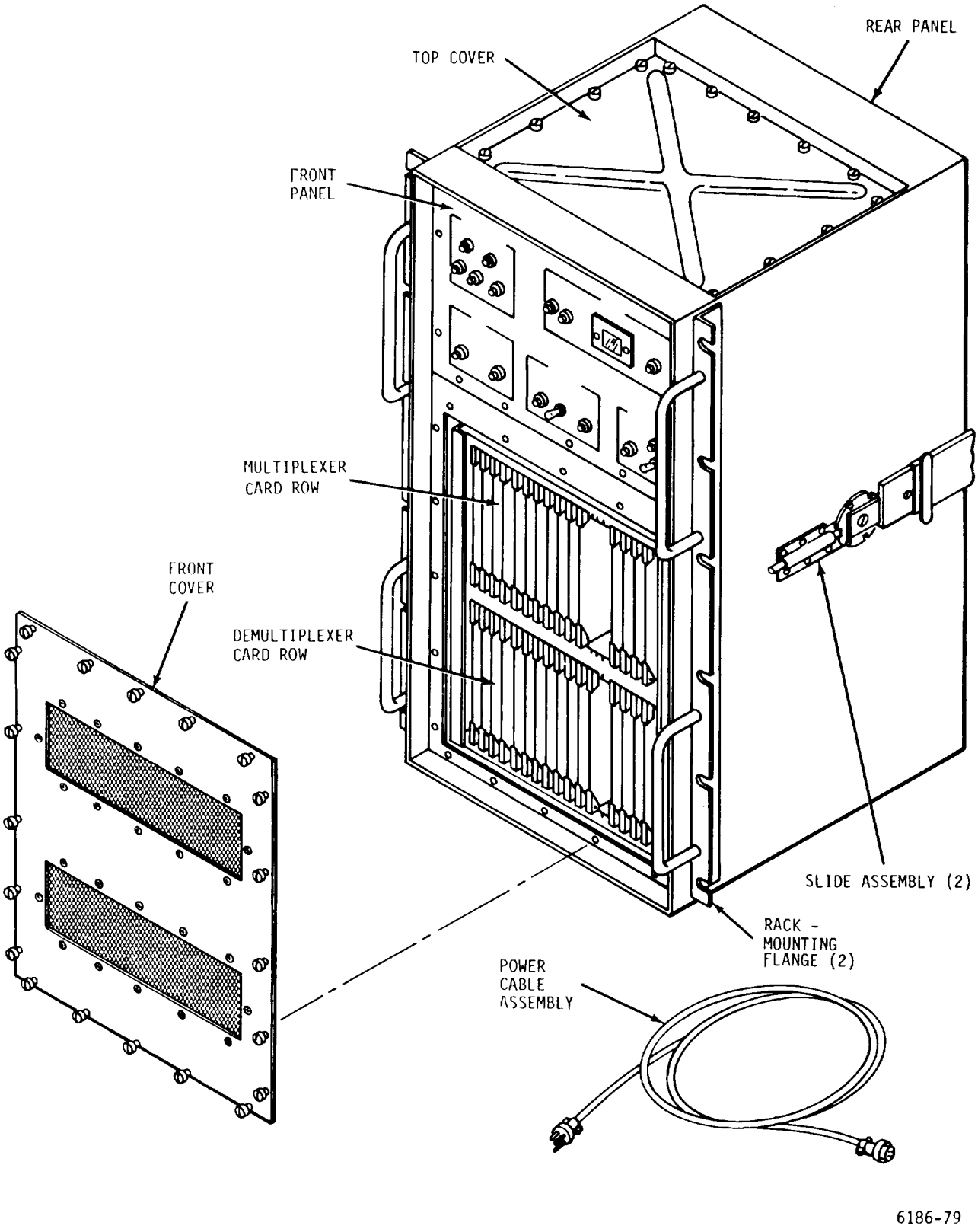


Figure 1-1. AN/GSC-24 (V) Multiplexer SET

multiplexer set are mounted on plug-in printed circuit cards that are accessible from the front of the equipment (figures 1-2 and 1-3). The power supply (figure 1-4) is a removable assembly that is mounted in the top of the multiplexer set. All interconnecting cables associated with the multiplexer set are connected to receptacles on the rear of the chassis.

1-5. The printed circuit cards in the MULTIPLEXER (upper) row (figure 1-2) comprise the multiplexer; the printed circuit cards in the DEMULTIPLEXER (bottom) row comprise the demultiplexer. The one exception is the display card in the upper row, which is common to both the multiplexer and the demultiplexer. Within the multiplexer and the demultiplexer, the cards are further designated as common cards or channel cards. The quantity and types of common cards are fixed, whereas the quantity and types of channels cards are determined by system application. The common cards generate the timing and control signals for the multiplexing and demultiplexing functions. The channel cards provide the input and output interface between the applied channel data and the common processing electronics. Information on the quantity and types of printed circuit cards associated with the multiplexer set is contained in paragraph 1-11.

1-6. LEADING PARTICULARS.

1-7. Leading particulars of the multiplexer set are listed in table 1-1.

1-8. CAPABILITIES AND LIMITATIONS.

1-9. Physical and electrical capabilities and limitations of the multiplexer set are listed in tables 1-2 and 1-3.

1-10. EQUIPMENT SUPPLIED.

1-11. The equipment supplied is listed in table 1-4 and shown in figure 1-1. The plug-in printed circuit cards used in the multiplexer and the plug-in printed circuit cards used in the demultiplexer are listed in separate groups. Three cards (seq, OEG, and GC/ DM) are common to the multiplexer and the demultiplexer, and are therefore listed twice. The single display card is associated with the demultiplexer and the multiplexer. The quantity of each of the three channel cards in the multiplexer is marked AR (as required) the quantity of each of the four channel cards in the demultiplexer is also marked AR. The quantity and types of channel cards installed in a multiplexer set depend on system application. The maximum number of multiplexer or demultiplexer channel cards used in a given system application is 15.

1-12. RELATED TECHNICAL MANUALS.

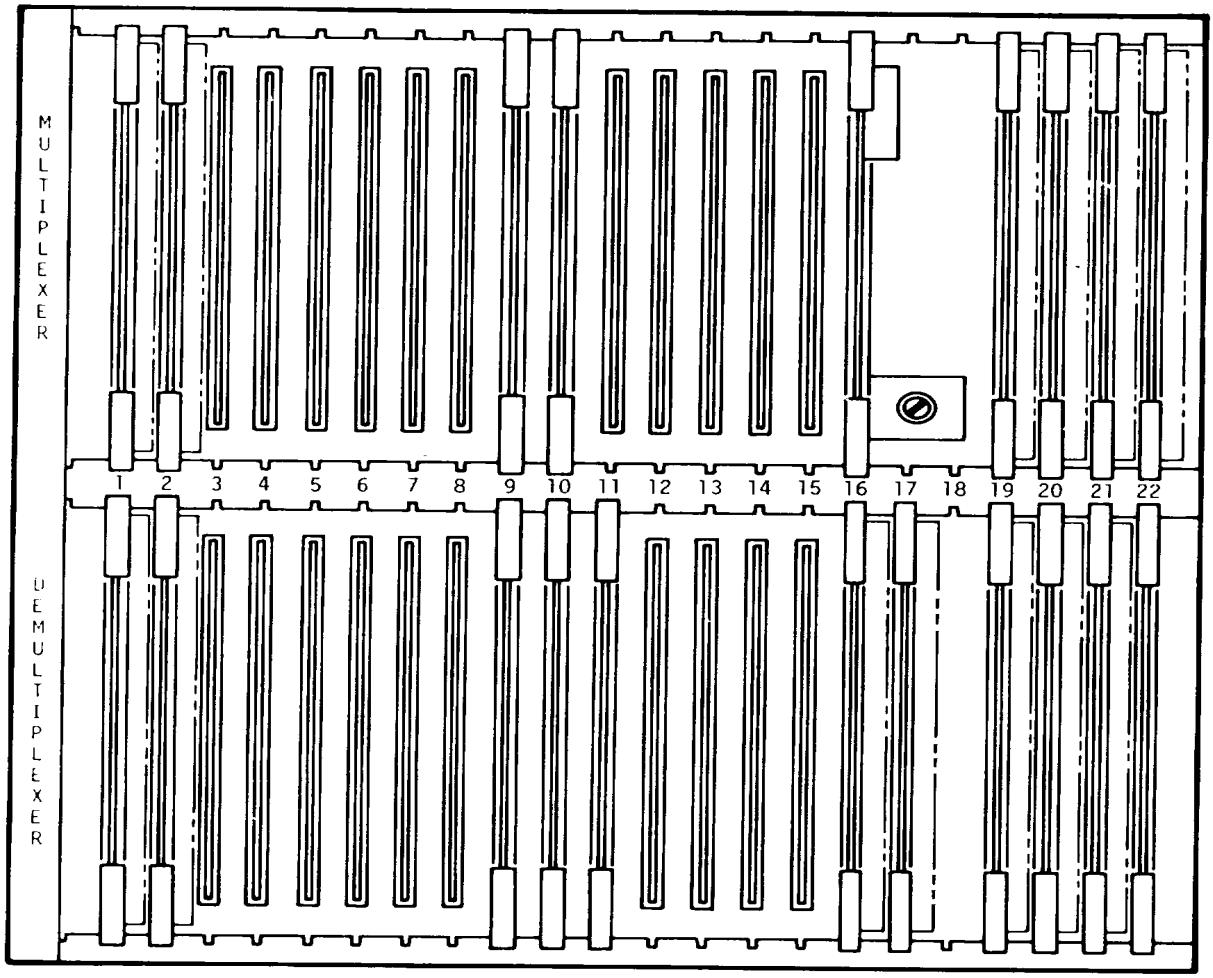
1-13. Technical manuals related to the multiplexer set are listed in table 1-5.

1-14. SPECIAL TOOLS.

1-15. The special tools required for maintenance of the multiplexer set are listed in table 1-6.

1-16. TEST EQUIPMENT.

1-17. The test equipment required for maintenance of the multiplexer set is listed in table 1-7.



MULTIPLEXER LOCATIONS:

1 THRU 15	CHANNEL CARDS	
16	RT CARD	COMMON CARDS
17, 18	NOT USED	
19	OEG CARD	
20	GC/DM CARD	
21	SEQ CARD	
22	DISPLAY CARD	

DEMULTIPLEXER LOCATIONS:

1 THRU 15	CHANNEL CARDS	
16	FS CARD	COMMON CARDS
17	ERD CARD	
18	NOT USED	
19	OEG CARD	
20	GC/DM CARD	
21	SEQ CARD	
22	EXTENDER CARD	

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Figure 1-2. Printed Circuit Card - Location View

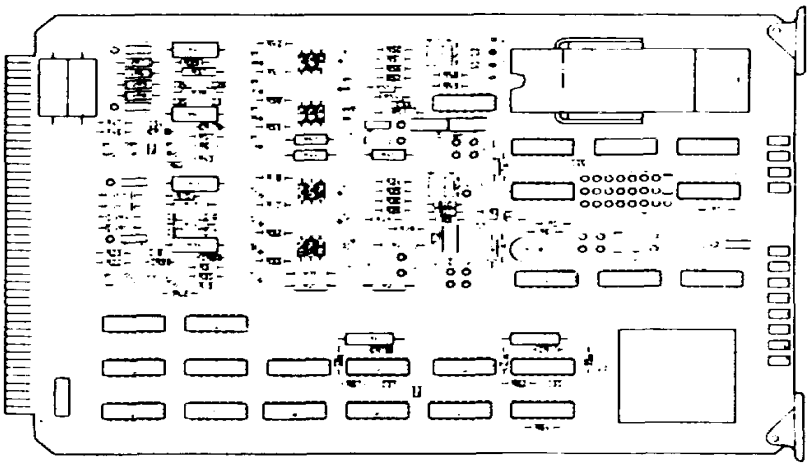

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Figure 1-3. Typical Printed Circuit Board - Physical View

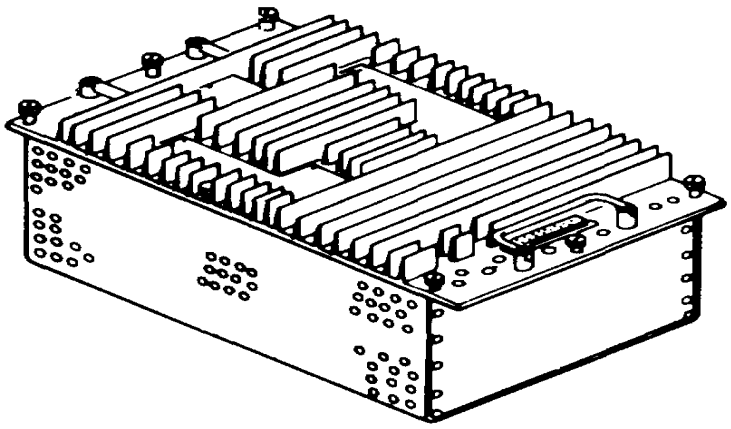

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Figure 1-4. Power Supply - Physical View

Table 1-1. Leading Particulars

Item	Data
Overall dimensions	
Height	24.5 inches
Width	17.0 inches
Depth	19.0 inches
Weight (fully configured)	140 pounds
Primary power	115 vac ±10%, single phase, 47 to 410 Hz, 634 watts
Mounting	Standard 19-inch relay rack
Interface connectors	
Signal (timing and data)	Bendix 30340-5 or equivalent (mates with Bendix 33449-1 or equivalent)
Signal (remote alarms)	MS3470E14-19P (mates with MS3470E14-19S)
Power	MS3126F12-3P (mates with MS3126F12-3S)
Transportability	Suitable for transport by rail, air, ship, or highway carrier

Table 1-2. Physical Capabilities and Limitations

Parameter	Capability
Temperature	
Operating	-180 to +520°C (00 to +1250F)
Nonoperating, transit, storage	-620 to +710C (-80° to +1600F), including solar radiation
Atmospheric pressure	
Operating	Sea level to 10,000 feet (20.58 inches Hg)
Nonoperating, transit, and storage	Sea level to 50,000 feet (3.44 inches Hg)

Table 1-2. Physical Capabilities and Limitations (Cont)

Parameter	Capability
Shock and vibration	As normally encountered during operation and during shipment by land, sea, or air
Humidity	High and low extremes as specified in MIL-STD-210, paragraphs 2.3.2 and 2.4.1

Table 1-3. Electrical Capabilities and Limitations

Parameter	Capability
Multiplexer output rate (R_c)	Any rate within the limits of 155 bps and 10 Mbps
Ports in use (N)	Variable, 15 through 31
Ports assigned to a channel (K)	Variable, 1 through 25
Channels	Variable, 1 through 15
Channel data forms	
Type I - digital data with associated timing	Data rate within the limits of 50 bps and 3 Mbps fitting the expression: $0.96 \geq K\left(1 - \frac{C}{KR_P}\right)$ where R_c = channel rate R_P = port rate K = number of used ports assigned to the channel
Type II - digital data without associated timing (transition encoding/decoding technique)	Data rates within the limits of 0 bps and 400 bps

Table 1-3. Electrical Capabilities and Limitations (Cont)

Parameter	Capability
Type II - digital data without associated timing (timing recovery processing technique)	Data rates up to 9600 bps, which have a data sense transition (1 to 0 or 0 to 1) at least once each 100 data bit times and fitting the expression: $R_c = 75 \times 2^n$ bps where: n = integer from 0 to 7
Voice	300 to 3400 Hz, using a sample rate (KRp) equal to or greater than 19.2 kbps. Slower sample rates may be used with a corresponding decrease in performance parameters.
Channel rate variation	
Type I	±250 parts per million (ppm)
Type II	±250 ppm. Channel input rates, including rate variation, being processed by the transition encoding technique cannot exceed 400 bps.
Voice	Not applicable
Channel input levels	
Types I and II	+0.5v minimum (logical 1) and -0.5v minimum (logical 0)
Voice	-16 dBm at 1000 Hz for full modulation
Channel output levels	
Types I and II	Positive and negative 6±1 volts, open circuit
Voice	+7 dBm at 1000 Hz with fully modulated channel input

Table 1-3. Electrical Capabilities and Limitations (Cont)

Parameter	Capability
Channel input impedance	
Types I and II	6000 ohms minimum or 75 ohms ±10%, switch selectable
Voice	600 ohms (balanced)
Channel output impedance	
Types I and II	6000 ohms minimum or 75 ohms ±10%, switch selectable
Voice	600 ohms (balanced)
Frame synchronization-acquisition and reacquisition time	Less than 15×10^3 bit times for 90% of the time (standard error environment of 1/100 assumed)
Bit count integrity (BCI)	At least 10^{13} bit times in an error-free environment. Other environments are as follows:

Random Error Rate	Mean Time to Loss of BCI
1 error per 8 bits	2×10^4 bits or greater
1 error per 16 bits	1×10^7 bits or greater
1 error per 32 bits	1.5×10^9 bits or greater
1 error per 100 bits	1×10^{13} bits or greater

Table 1-4. Equipment Supplied

Official Nomenclature	Common Name	Part No.	Qty	Card Location (fig. 1-2)	Description
Multiplexer					
Display circuit card assembly	Display card	61864050-009	1	A22	Display card - provides diagnostic combining and priority encoding function for multiplexer and demultiplexer cards.
Gated clock/data mux circuit card assembly	GC/DM card	61864030-009	1	A20	Common card - provides multiplexer timing and gating signals that multiplex channel data from channel cards into high-speed serial data stream.
Timing and overhead enable generator circuit card assembly	OEG card	61864020-009	1	A19	Common card - provides multiplexer timing signals and multiplexes overhead stuffing signals from channel cards into one serial overhead data stream.
Rate comparison buffer circuit card as-	RCB card	61864010-009	AR	A1-A15	Channel card - provides input buffering for one digital data channel with timing.
Reference timer circuit card	RT card	61864150-009	1	A16	Common card - provides master timing signals and conditions outgoing high-speed data stream.
Sequencer circuit card assembly	Seq card	61864040-009	1	A21	Common card - provides timing signals and channel address sequence signals to sequence data from channel cards to GC/DM card.

Table 1-4. Equipment Supplied (Cont)

Official Nomenclature	Common Name	Part No.	Qty	Card Location (fig. 1-2)	Description
			Multiplexer (Cont)		
Transition encoder and timing recovery circuit card	TE/TR	61864060-card	AR	A1-A15 009	Channel card - provides input buffering for one digital data channel without timing.
Voice encoder circuit card assembly	VE card	61864070-009	AR	A1-A15	Channel card - provides analog-to-digital interface for one voice channel.
			Demultiplexer		
Card extender circuit card assembly	Extender card	61864080-009	1	A22	Extender card for adjustments and testing of multiplexer and demultiplexer functional cards.
Error rate detector and remote alarms circuit card assembly	ERD card	61864120-009	1	A17	Common card - monitors error rates of demultiplexer input data, and generates remote alarm signals for multiplexer and demultiplexer.
Frame sync circuit card assembly	FS card	61864110-009	1	A16	Common card - maintains synchronization of demultiplexer timing circuits with those of transmitting multiplexer. Also receives and distributes incoming high-speed serial data stream to channel cards.

Table 1-4. Equipment Supplied (Cont)

Official Nomenclature	Common Name	Part No.	Qty	Card Location (fig. 1-2)	Description
Demultiplexer (Cont)					
Gated clock/ data mux circuit card assembly	GC/DM card	61864030-009	1	A20	Common card - provides demultiplexer timing signals, and gating signals to gate channel data to channel
Narrow band smoothing buffer circuit card assembly	NBSB card	61864160-009	AR	A1-A15	Channel card - provides output buffering for one digital data channel.
Sequencer circuit card assembly	Seq card	61864040-009	1	A21	Common card - provides timing signals, and channel address sequence signals to sequence data to channel cards.
Smoothing buffer circuit card assembly	SB card	61864090-	AR	A1-A15 009	Channel card - provides output buffering for one digital data channel.
Timing and overhead enable generator circuit card assembly	OEG card	61864020-009	1	A19	Common card - provides demultiplexer timing signals, and processes diagnostic error signals for demultiplexer channels.
Transition decoder circuit card assembly	TD card	61864130-009	AR	A1-A15	Channel card - provides output buffering for one low-speed digital data channel without. timing.

Table 1-4. Equipment Supplied (Cont)

Official Nomenclature	Common Name	Part No.	Qty	Card Location (fig. 1-2)	Description
Demultiplexer (Cont)					
Voice de-coder cir-cuit card assembly	VD card	61864140-009	AR	Al-Al5	Channel card - provides digital- to -analog out-put interface for one voice channel.
Additional Equipment					
Cable as-sembly (power)	Power cable	61861700-009	1		AC power input cable.
Connector set assembly		61867000-009 and -019	Variable		Mating connectors for rear panel Twinax recep-tacles. Quantity determined by channel requirements.

Table 1-5. Related Technical Publications

Publication Number	Publication Title	Equipment Nomenclature
T.O. 31W2-2GSC24-3 (Air Force) T.M. 11-5805-688-14-2 (Army) NAVELEX 0967-LP-545-3020 (Navy)	Technical Manual - Circuit Diagrams	AN/GSC-24(V) multiplexer set
T.O. 31W2-2GSC24-4 (Air Force) T.M. 11-5805-688-14-3 (Army) NAVELEX 0967-LP-545-3030 (Navy)	Technical Manual - Illustrated Parts Breakdown	AN/GSC-24(V) multiplexer set
T.O. 31W2-2GSC24-6WC-1	Scheduled Periodic Work Cards	AN/GSC-24(V) multiplexer set

Table 1-5. Related Technical Publications (Cont)

Publication Number	Publication Title	Equipment Nomenclature
T.O. 31W-1-06-2	Work Unit Code Manual	AN/GSC-24(V) multiplexer set
To be assigned	Technical Manual - Harris Model 7003 Data Communications Test Set	To be assigned
To be assigned	Technical Manual - Power Supply Test Set	To be assigned
To be assigned	Technical Manual for Subassembly Test Set	To be assigned

Table 1-6. Special Tools List
(Equivalent equipment is authorized.)

Part (Tool) Number	Mfr Code or Name/ Address	Figure and Index No.	Nomenclature	Use (para)
SK62759367	09439		Wire-wrap repair tool set consisting of:	
14XA2-B3C-(28)	24047	6-7	Wire wrapping tool	6-28
507100	24047	6-7	Wrapping sleeve	6-28
508748	24047	6-7	Wrapping kit	6-28
511203	24047		Unwrapping tool	6-28
515654	24047	6-7	Cut/strip accessory	6-28
SK63759367	04939		Connector repair tool set consisting of:	6-66
CCT-DL	71468		Hand crimp tool	
CET-DL-2	71468		Extraction tool	
CET 12-14	71468		Extraction tool	
CET 6CB	71468		Extraction tool	
MS18278-1	96906		Insertion/extraction tool	
274-7304-00	71468		Contact Removal Tool	

Table 1-6. Special Tools List (Cont)
(Equivalent equipment is authorized.)

Part (Tool) Number	Mfr Code or Name/ Address	Figure and Index No.	Nomenclature	Use (Para)
M22520/2-01			Crimp tool	
M22520/2-08			Crimp tool	
WT-311	59730		Crimp tool	
			Chassis repair tool set consisting of:	Note 1.
B22	98291	6-24	Insertion tool	
CHM1	72962	6-20	Handle	
CHM2	72962	6-20	Handle	
CPFA10	72962	6-20	Punch	
CPFA6	72962	6-20	Punch	
CPFB6	72962	6-20	Dolly	
CPFB8	72962	6-20	Dolly	
HT-1	98291	6-24	Hand insertion tool	
H7503-10	08524	6-17	Installation tool	
KT7200	92631	6-22	Handle	
KT7202-046	92631	6-22	Squeeze tool	
KT7202-083	92631	6-22	Squeeze tool	
29-47-101-10	94222	6-16	Installation tool	
TK-105/G			Electronic equipment tool kit	Note 2.

NOTES: 1. Depot level use only.
2. General Repair at intermediate and depot level.

Table 1-7. Test Equipment List
(Equivalent equipment is authorized.)

Table 1-6.

Type Designation	Alternate Type Designation	Figure No.	Nomenclature	Use (para)
GR Model 1321-N			Decade Resistance Box	Note 3
HARRIS Model 7003			Digital communications test set	6-42
HP Model 204D			Signal generator	Note 3
HP Model 331A			Distortion Analyzer	Note 3
HP Model 3310A			Function generator	Notes 3, 4
HP Model 3400A			Voltmeter Note 3	
HP Model 3490A			Digital Multimeter	Notes 3, 4
HP Model 3550B			Portable test set	6-41
HP Model 3555B			Transmission and noise meter	Note 3
HP Model 4329A			Insulation resistance	Note 4
HP Model 5245M			Frequency counter	6-34, 35 Notes 3, 4
HP Model 6205B			Power supply	Notes 3, 4
HP Model 630A			Multimeter	Note 1
Tektronix Model R7704A			Oscilloscope main frame	Note 1
Model P6063A			Probe	Notes 1, 2
Model 7A26			Dual vertical amplifier	Notes 1, 2
Model 7B92			Time base	Notes 1, 2
Model 7D15			Universal counter	Notes 1, 2
61868300-009			Power supply test set	Note 5
61868000-009			Subassembly test set	Note 6

NOTES:
1. General troubleshooting at intermediate and depot level.
2. Used with oscilloscope main frame.
3. Used with subassembly test set for printed circuit card maintenance at depot level
4. Used with power supply test set for power supply maintenance at depot level.
5. Power supply maintenance at depot level.
6. Printed circuit card maintenance at depot level.

CHAPTER 2

INSTALLATION

SECTION I

INSTALLATION LOGISTICS

2-1. GENERAL..

2-2. This section contains general instructions for unpacking and storing the multiplexer set prior to installation as prescribed in section II.

2-3. UNLOADING AND UNPACKING.

WARNING

The multiplexer set weighs 140 pounds. Use a mechanical lifting device whenever possible. To prevent injury to personnel, it is recommended that a minimum of four men be used when a multiplexer set is to be lifted manually.

2-4. During the unpacking procedures, the multiplexer set should be positioned on a firm, level surface in an area that is protected from the elements. No special or unique procedures are required for unpacking the multiplexer set.

NOTE

Use care when opening the shipping container to prevent unnecessary damage to the container so that it may be stored and reused for repacking a multiplexer set for reshipment.

1. Open the shipping container and carefully remove loose padding and fill material.

CAUTION

Use care when lifting multiplexer set from container to prevent damage to protruding controls, indicators, and receptacles on the unit.

2. Remove multiplexer set from shipping container. Remove moisture resistant barrier material from multiplexer set.

3. Inspect exterior surfaces of multiplexer set for shipping damage, missing or damaged controls and indicators, and evidence of water damage.

4. Check received equipment against shipping documents and/or packing slip.

5. When equipment is incomplete or damaged, fill out and forward appropriate forms in accordance with prescribed directives.

2-5. STORAGE HOUSING REQUIREMENTS.

2-6. The multiplexer set should be housed to protect it from inclement weather. The unit should be stored within an ambient temperature range of -80° to +160°F (-62° to +71°C). The multiplexer set in a nonoperating condition can be stored at altitudes from sea level to 50,000 feet (3.44 inches Hg). The multiplexer set can be stored on a flat surface capable of supporting 50 pounds per square foot. The accessories listed in paragraph 2-8 should be inventoried

and stored with the multiplexer set or in a area designated for storage of small items.

2-7. RECEIVING DATA.

2-8. The multiplexer set is shipped with a set of plug-in cards installed in the unit. The quantity and type of plug-in cards will be determined by system application of the equipment. The appropriate shipping literature will identify the quantity and card types. Two separate accessories are shipped with the multiplexer set: power cable assembly P/N 61861700-009 (ac power cable) and connector kit assembly P/N 61867000009 or P/N 61867000-019. The contents of each connector kit assembly are listed in the following chart.

2-9. INSTALLATION HOUSING REQUIREMENTS.

2-10. The multiplexer set is constructed so that it can be mounted in a standard 19-inch relay rack or equivalent. The ruggedized chassis also allows the multiplexer set to be installed on a flat, open surface that is capable of supporting 50 pounds per square foot. The installation data in table 2-1 should be considered when selection of an installation location for the multiplexer set is under consideration.

Item/Part No.	Quantity -019	-009
Backshell M83723-15S-14	1	1
Plug MS3476E14-19S	1	1
Connector plug (Bendix P/N 33449-1)	37	65

Table 2-1. Installation Data

Item	Data
Chassis dimensions	
Height	24.5 inches
Depth	19.0 inches
Width	17.0 inches
Chassis weight	140 pounds
Rack requirement	Standard 19-inch relay rack that is firmly mounted to a floor to prevent tipping when multiplexer set is mounted on slides and extended out of rack.

Table 2-1. Installation Data (Cont)

Item	Data
Rack clearances	
Front	Allow approximately 48 inches for installation or removal of multiplexer set from rack. Allow same area for servicing multiplexer set extended on slides for servicing.
Rear	Allow approximately 24 inches for routing of cable assemblies connected to rear of multiplexer set, and for circulation of exhaust air from cooling air blower in upper rear of multiplexer set.
Operating position	Normal (level) to 90° inclination
Operating temperature	0°to +125° F (-18° to +52°C) ambient temperature
Operating altitude	Sea level to 10,000 feet (20.58 inches Hg)
Primary power	115 vac ±10%, single phase, 47 to 410 Hz
Power dissipation	634 watts
Electrical connectors on rear panel	
Signal (timing and data)	Bendix 30340-5 or equivalent - mates with Bendix 33449-1 or equivalent.
Signal (remote alarm)	MS3470E14-19P - mates with MS3470E14-19S
Power	MS3126F12-3P - mates with MS3126F12-3S

SECTION II

INSTALLATION PROCEDURES

2-11. GENERAL.

2-12. This section contains general instructions for installing the multiplexer set in a standard 19-inch relay rack. Since there are different equipment rack configurations in which the multiplexer set may be installed, it may be necessary to modify the installation procedures for a particular installation. As specified in the following procedures, a multiplexer set can be installed in a rack in one of two ways: the unit can be mounted and supported in a rack by the two slide assemblies (figure 1-1) provided (paragraph 2-13); or the unit can be bolted directly in a rack, using the two rack-mounting flanges (figure 1-1) on the front of the chassis (paragraph 2-15).

2-13. INSTALLATION PROCEDURES.

NOTE

Before installing a multiplexer set in a rack, check the installation data in table 2-1 to ensure the mounting and operating conditions are adequate.

2-14. Perform the following procedures to install the multiplexer set in a rack, using the slide assemblies.

1. Determine the exact physical position in which the multiplexer set will be mounted in the rack. Then determine the positions in which the two slide assemblies on the chassis will be attached to the rack frame. Remove the outer section of each slide assembly and use it as a template to mark the locations where the forward and aft pairs of mounting holes align with the interior of the rack frame. If required, mark and drill rack frame as necessary to mount the slide assembly to the rack frame.

WARNING

When performing step 2, secure each outer slide section to rack frame, using four screws. The use of less than eight screws (four on each side) to secure the two outer slide sections may cause the multiplexer set to break loose and cause serious injury to personnel.

2. Connect each outer slide section to the rack frame, using a minimum of four 10-32 (minimum size) screws with flat washers, lockwashers, and nuts.

3. Note that sufficient clearance is provided for insertion of remaining slide sections into the front of the rack-mounted outer slide sections. If such clearance is not provided or is marginal, the forward lip of the rack should be suitably notched.

4. Fully extend (toward rear of chassis) the two inner slide sections attached to each side of the multiplexer set chassis.

WARNING

A multiplexer set weighs 140 pounds. Use a mechanical lifting device whenever possible. To prevent injury to personnel, it is recommended that a minimum of four men be used when a multiplexer set is to be lifted manually.

5. Lift multiplexer set and position extended inner slide sections on unit so that they mate with outer slide sections installed in rack. Slowly position multiplexer set fully into rack until rack-mounting flanges on multiplexer set contact the front of the rack frame.

6. With multiplexer set in place in rack, install twelve 10-32 (minimum size) screws, with washers, to secure rack-mounting flanges on multiplexer set to rack.

7. On rear of multiplexer set, connect power cable assembly to POWER INPUT receptacle on unit and to a suitable ac power source outlet.

8. Connect signal cables between receptacles on rear of multiplexer set

as prescribed for the specific system configuration.

9. Remove front cover from multiplexer set (figure 1-1) and ensure that the plug-in card complement is correct for the designated system application.

10. Visually inspect plug-in cards and interior of multiplexer set for damage.

11. Perform the procedures prescribed in section III of chapter 3 to electrically configure the multiplexer set for the selected system application.

2-15. Perform the following procedures to mount a multiplexer set to a rack, using only the two rack-mounting flanges on the multiplexer set.

1. Determine the exact physical location in which the multiplexer set will be mounted in the rack.

NOTE

When the two slide assemblies on the multiplexer set interfere with the installation of the unit in a rack, the slide assemblies should be removed as prescribed in step 2. If the slide assemblies are already removed or do not interfere with the installation, proceed to step 3.

2. Remove two slide assemblies from chassis by removing seven screws securing each slide assembly to multiplexer set. Store removed slide assemblies for future use.

WARNING

A multiplexer set weighs 140 pounds. Use a mechanical lifting device whenever possible. To prevent injury to personnel, it is recommended that a minimum of four men be used when a multiplexer set is to be lifted manually.

3. Lift multiplexer set into rack and secure rack-mounting flanges to rack frame, using twelve 10-32 (minimum size) screws with washers.

4. On rear of multiplexer set, connect power cable assembly to POWER INPUT receptacle on unit and to a suitable ac power source outlet.

5. Connect signal cables between receptacles on rear of multiplexer set as prescribed for the specific system configuration.

6. Remove front cover (figure 1-1) and note that the plug-in card complement is correct for the designated system application. Visually inspect plug-in cards and interior of multiplexer set for damage.

7. Perform the procedures prescribed in section III of chapter 3 to electrically configure the multiplexer set for the selected system application.

CHAPTER 3

PREPARATION FOR USE

SECTION I

GENERAL

3-1. INTRODUCTION.

3-2. This section and sections II and III contain introductory information and detailed instructions for preparing the multiplexer set for operation. Instructions for preparing the multiplexer set for reshipment are prescribed in section IV.

3-3. This section contains general information about the multiplexer set and its application within various data communications systems. The purpose of this section is to assist the user in understanding equipment configuration planning as prescribed in sections II and III.

3-4. Detailed instructions for configuration of an actual multiplexer set are contained in section III. The procedures are predicated upon the availability of a set of completed configuration worksheets. Section II describes, by example, procedures for preparing the worksheets and also discusses supplemental factors that should be considered in planning a multiplexer set system application. Normally, the user is provided with worksheets that describe how a multiplexer set is to be configured for a specific application. In such cases, the user may regard the instructions in section II as supplementary information.

3-5. TYPICAL SYSTEM APPLICATIONS.

3-6. The multiplexer set is a flexible equipment capable of simultaneously performing multiplexing and demultiplexing functions. Except for operating power and certain display and alarm features, the functions are independent of each other. Because of their functional independence, a multiplexer and demultiplexer within a given equipment may each be configured to simultaneously process channel data of different and unrelated forms.

3-7. Figure 3-1 depicts the multiplexer set in typical duplex system applications. As shown in configuration A of figure 3-1, input channels of the forms a, b, and c are applied to the multiplexer (MUX) function of multiplexer set No. 1. These inputs are combined (multiplexed) into a single output data stream and are routed via a transmission link to a far-end demultiplexer (DEMUX) that is a part of multiplexer set No. 2. Channels a, b, and c are outputs of the far-end demultiplexer, and are subsequently routed to the assigned users. In return, the far-end multiplexer accepts channel inputs of the forms a, b, and c, and routes them via the transmission link to the demultiplexer portion of multiplexer set No. 1. Thus, in this example, channel data of the same forms (a, b, and c) are transmitted in both directions.

3-8. Configuration B of figure 3-1 depicts an unsymmetrical duplex system application in which channel data transmitted in one direction are in a different form than the data transmitted in the other direction. This configuration is made possible by the independence of multiplexer and demultiplexer functions within a given multiplexer set.

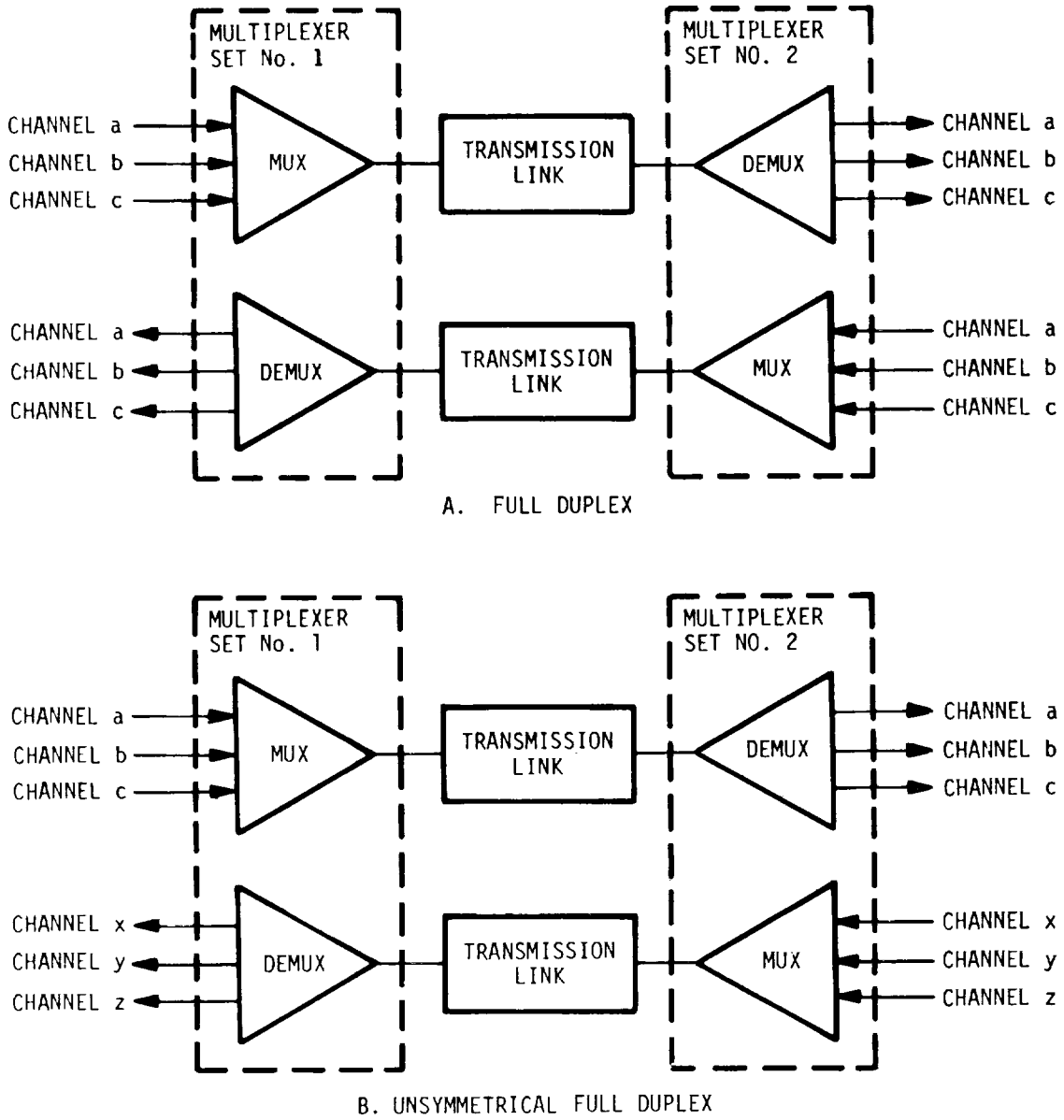


Figure 3-1. Typical Duplex Configurations

3-9. Figure 3-2 depicts the multiplexer set in typical simplex system configurations. In simplex system applications, the independence of multiplexer and demultiplexer functions enables one function, or portions thereof, to operate while the other function remains unused. As shown in configuration A of figure 3-2, the multiplexer portion of multiplexer set No. 1 combines inputs a, b, and c for transmission to a farend demultiplexer that is a part of multiplexer set No. 2. In such an application, the near-end demultiplexer and far-end multiplexer functions are not used.

3-10. Configuration B of figure 3-2 depicts another type of simplex application, which is sometimes referred to as a broadcast arrangement. In this application, data from a near-end multiplexer are transmitted to several farend demultiplexers. Each demultiplexer is configured to output one (or more) of the channels applied to the transmitting multiplexer. In such an arrangement, the near-end demultiplexer, the far-end multiplexers, and portions of the farend demultiplexers are not used.

3-11. CHANNEL AND PORT RELATIONSHIPS.

3-12. Data applied to the multiplexer's channel inputs are converted, when necessary, into a prescribed digital form and are held in buffer storage until they are synchronously inserted into the multiplexer's serial output data stream. Since data from multiple channels must enter this stream, they are inserted at a predetermined time in an established channel sampling sequence. The interval of time during which data from a given channel are allowed to enter the multiplexer's output stream is termed a port. Thus, in a given multiplexer configuration, a port is permanently assigned to a particular channel and will convey that channel's data into the multiplexer's output when the port occurs.

3-13. When a port assigned to a given channel occurs, a single bit of the channel data passes to the multiplexer's output. Therefore, the rate at which the porting occurs must equal the channel's input data rate (R_c). However, since the multiplexer set must be capable of simultaneously accepting channel inputs of different rates, multiple ports may be assigned to a single channel. The number of ports thus assigned to a given channel may vary up to a maximum of 25, and is termed K. The assignment of more than one port to a given channel is termed port strapping. The first port assigned to a channel is known as the active port, and subsequent ports assigned to that channel are known as strapped ports. The product of the rate that each port is sampled, known as port rate (R_p), and the total number of ports (K) assigned to a channel must be equal to or greater than the channel's input data rate (R_c), or $KR_p \geq R_c$. In a given multiplexer configuration, the total number of ports assigned to the multiplexer's channels is known as N, and must be an integer between 15 and 31.

3-14. Regardless of configuration, a single port within the multiplexer is automatically reserved for conveying overhead data generated within the multiplexer into the multiplexer's output data stream. Thus, in any given multiplexer configuration, the total quantity of ports used for processing channel and overhead data is N + 1, and is between 16 and 32. The multiplexer's output data rate, termed R_o, is simply the product of port rate (R_p) and the total quantity (N + 1) of ports used, or $R_o = R_p (N + 1)$.

3-15. The port assignments in a receiving demultiplexer must exactly match those used in the transmitting multiplexer. This enables the demultiplexer to disassemble its serial input data stream into individual channel outputs matching the multiplexer's inputs. In applications where several

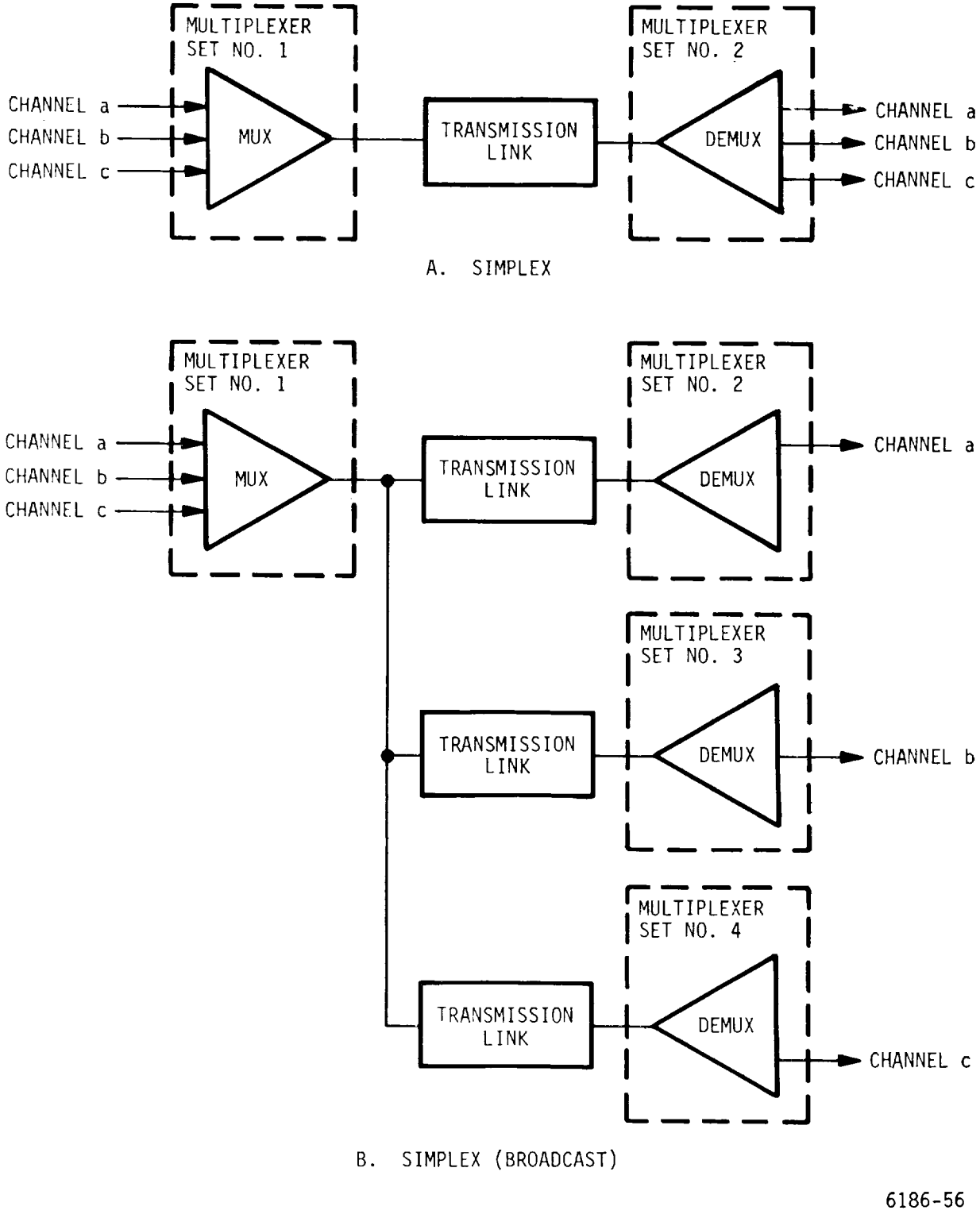


Figure 3-2. Typical Simplex Configuration

demultiplexers are receiving inputs from a single multiplexer (paragraph 3-9), port assignments within each demultiplexer must match those of the transmitting multiplexer.

3-16. In summary, a port is an interval of time during which a bit of data is inserted into the multiplexer's serial output stream. For a given configuration, one or more ports may be assigned to a particular channel; the total for the channel is termed K. The product of K and the rate at which porting occurs (R_0) must equal or exceed the channel input rate (R_0). The total quantity of ports assigned to channels in a given multiplexer configuration is termed N, and when the overhead port is considered, the total number of ports in use is N + 1. The value for N + 1 varies between 16 and 32. Multiplexer output rate ($R_{0)}$ is equal to R_0 (N + 1). Regardless of system application, port-to-channel assignments in a receiving demultiplexer must exactly match those of the transmitting multiplexer.

3-17. CHANNEL RATES AND FORMS.

3-18.The multiplexer set will accept and properly process charnel inputs of varying forms and rates. Input forms include the following: digital data with associated timing; digital data without associated timing; and voice data. The rates at which data inputs may occur depend upon the input form and the mode in which they are processed by the multiplexer set. Specific form and rate limitations are discussed in paragraphs 3-19 through 3-24.

3-19. DIGITAL DATA WITH ASSOCIATED TIMING.

3-20. One of the channel input/output data forms accepted and processed by the multiplexer set is digital data with associated timing. This data form is commonly referred to as Type I, and is illustrated in figure 3-3. Note that one complete cycle of the input/output timing signal occurs for each bit time (T) of the data signal in figure 3-3. The multiplexer set accepts and processes Type I channel data at any rate between 50 bps and 3.0 Mbps, provided the rate satisfies the expression:

$$0.96 \geq K\left(1 - \frac{R_C}{KR_p}\right)$$

where

R_C = channel data rate

R_p = port rate

K = number of ports assigned to the channel

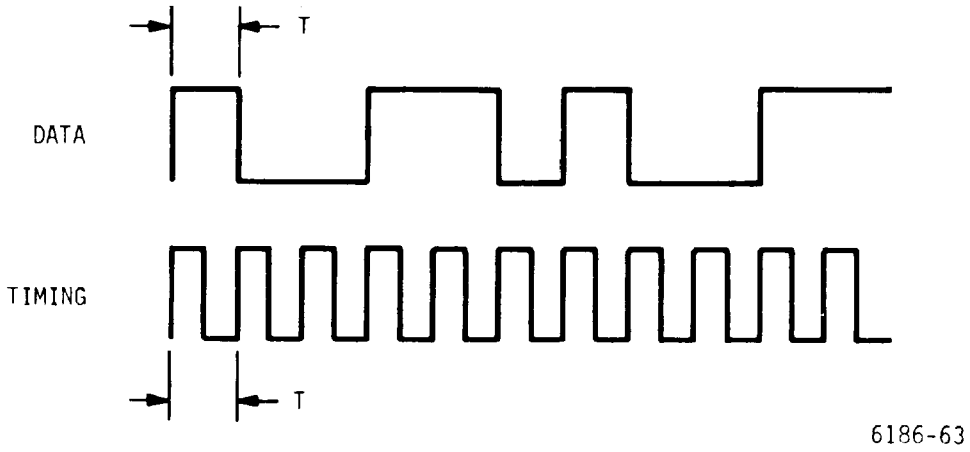


Figure 3-3. Typical Type I Channel Input/Output Data and Timing Waveforms

Normally, R_c is nominally equal to KR_p. In cases where R_c is not equal to KR_p, the channel rate is adjusted within the multiplexer set and processed at a rate of the form $R_c = KR_p$. The rate adjustment process is termed coarse rate conversion, and is performed completely within the multiplexer set. Therefore, although coarse rate conversion may be used, the demultiplexer's channel output rate is the same as the multiplexer's channel input rate.

3-21. Type-I channel input/output rates may vary from their assigned nominal value by plus or minus 250 parts per million (±250 ppm;. The multiplexer set automatically compensates for such rate deviations, using a process of internal bit insertion and deletion termed stuffing. The stuffing capability enables the multiplexer set to process channel input/outputs not synchronous with the set or with each other. For example, a channel input rate of 1.0 Mbps that varies between 1.000250 and 0.999750 Mbps is properly processed in the multiplexer set. Deviations appearing in a multiplexer input channel rate are automatically reinserted in the corresponding demultiplexer output channel rate. The multiplexer is therefore considered to be transparent to applied rate variations within prescribed limits.

3-22. DIGITAL DATA WITHOUT ASSOCIATED TIMING.

3-23. A second form of input/output channel data accepted and processed by the multiplexer set is digital data without timing. This data form is commonly referred to as Type II data. When provided with Type II channel data inputs, the multiplexer accepts the incoming data and processes the data by means of timing signals generated within the multiplexer. Data inputs of the Type II form are processed within the multiplexer set by the use of one of two techniques: timing recovery or transition encoding/decoding. Type II data to be processed by the timing recovery technique must be at rates fitting the expression:

$$R_c = 75 \times 2^n \text{ bps}$$

where

R_c = channel data rate

n = an integer from 0 to 7.

Rates fitting this expression are as follows:

n	R_c (bps)
0	75
1	150
2	300
3	600
4	1200
5	2400
6	4800
7	9600

It is also required that Type II channel data processed by the timing recovery technique reflect a sense transition (1 to 0, or 0 to 1) at least once each 100 data bit times. This enables the multiplexer to internally generate an appropriately synchronized timing signal for subsequent processing of the applied data. Type II data rates may vary from their assigned nominal values in the same manner as that described for Type I data rates (paragraph 3-21).

3-24. Type II data processed by the transition encoding/decoding technique may occur at rates within six ranges as follows:

0 - 75 bps

0 - 100 bps

0 - 150 bps

0 - 200 bps

0 - 300 bps

0 - 400 bps

Upon entering the multiplexer set, data are processed by using a 3-bit transition encoding/decoding process. This process entails use of a KR_p that is three times the upper limit of the data rate range selected. For example, a 75-bps channel rate input being processed with the 0to 75-bps data rate range would require a KR_p of 3 x 75 or 225 bps. It is not necessary that a given input data rate be processed with only the lowest rate range in which it falls. A lower input rate may be processed with any rate range whose upper limit is higher than the applied input rate. Thus, for example, a channel input data rate of 100 bps can be processed with the 0 to 150-bps rate range. It is also important to note that any input rate variation that causes the input rate to exceed the upper limit of the selected rate range may cause data errors to be generated by the multiplexer set. Therefore, if the nominal input data rate is at the upper limit of the rate range selected, and positive variations in the input rate are expected, it is best to select the next higher rate range. Type II channel data processed by the multiplexer using the transition encoding/decoding technique are supplied to the corresponding demultiplexer channel output without associated timing.

3-25. VOICE DATA.

3-26. The multiplexer set will accept and process voice data at frequencies within the range of 300 to 3400 Hz. Channel input/output impedance is 600 ohms(balanced). Full modulation occurs at a multiplexer input level of -16 dBm. The corresponding demultiplexer output level is +7 dBm. Processing of voice channel input data requires use of a KR_p of 19.2 kbps or greater. A KR_p of 38.4 kbps is preferred for voice processing.

3-27. CHANNEL CARD OPTIONS.

3-28. The channel input/output data forms discussed in paragraphs 3-19 through 3-26 are processed by means of a variety of optional multiplexer and demultiplexer channel cards. In appropriate combinations, the cards are plugged into multiplexer and demultiplexer card slots 1 through 15. Table 3-1 lists the optional channel cards used within the multiplexer set, and identifies the channel data form with which each card is associated.

Table 3-1. Multiplexer Set Channel Card Options

Channel Data Form	Multiplexer Channel Card	Demultiplexer Channel Card
Type I, digital data with associated timing	Rate comparison buffer (RCB), P/N 61864010	Smoothing buffer (SB), P/N 61864090
Type I, digital data with associated timing (special smoothing applications (paragraph 3-58)	Rate comparison buffer (RCB), P/N 61864010	Narrow band smoothing buffer (NBSB), P/N 61864160
Type II, digital data without associated timing (timing recovery processing technique)	Transition encoder/timing recovery (TE/TR), P/N 61864060	Smoothing buffer (SB), P/N 61864090
Type II, digital data without associated timing (transition encoding/ decoding technique)	Transition encoder/timing recovery (TE/TR), P/N 61864060	Transition decoder (TD), P/N 61864130
Voice data	Voice encoder (VE), P/N 61864070	Voice decoder (VD), P/N 61864140

SECTION II

PREPARATION OF CONFIGURATION WORKSHEETS

3-29. GENERAL.

3-30. In configuring the multiplexer set as prescribed in section III, the user must have certain information to satisfy a particular set of system application requirements. The information includes a definition of channel input/ output data rates, port assignment instructions, multiplexer output rate, etc. The required configuration information is recorded on a four-page set of configuration worksheets; the worksheets perform the basic functions listed in table 3-2.

3-31. Figure 3-4 depicts the system application requirement that is used as an example in the following discussions on the preparation of the configuration worksheets. More specifically, the discussions center on the preparation of the worksheets to enable the configuration of multiplexer set

Table 3-2. Configuration Worksheet Data

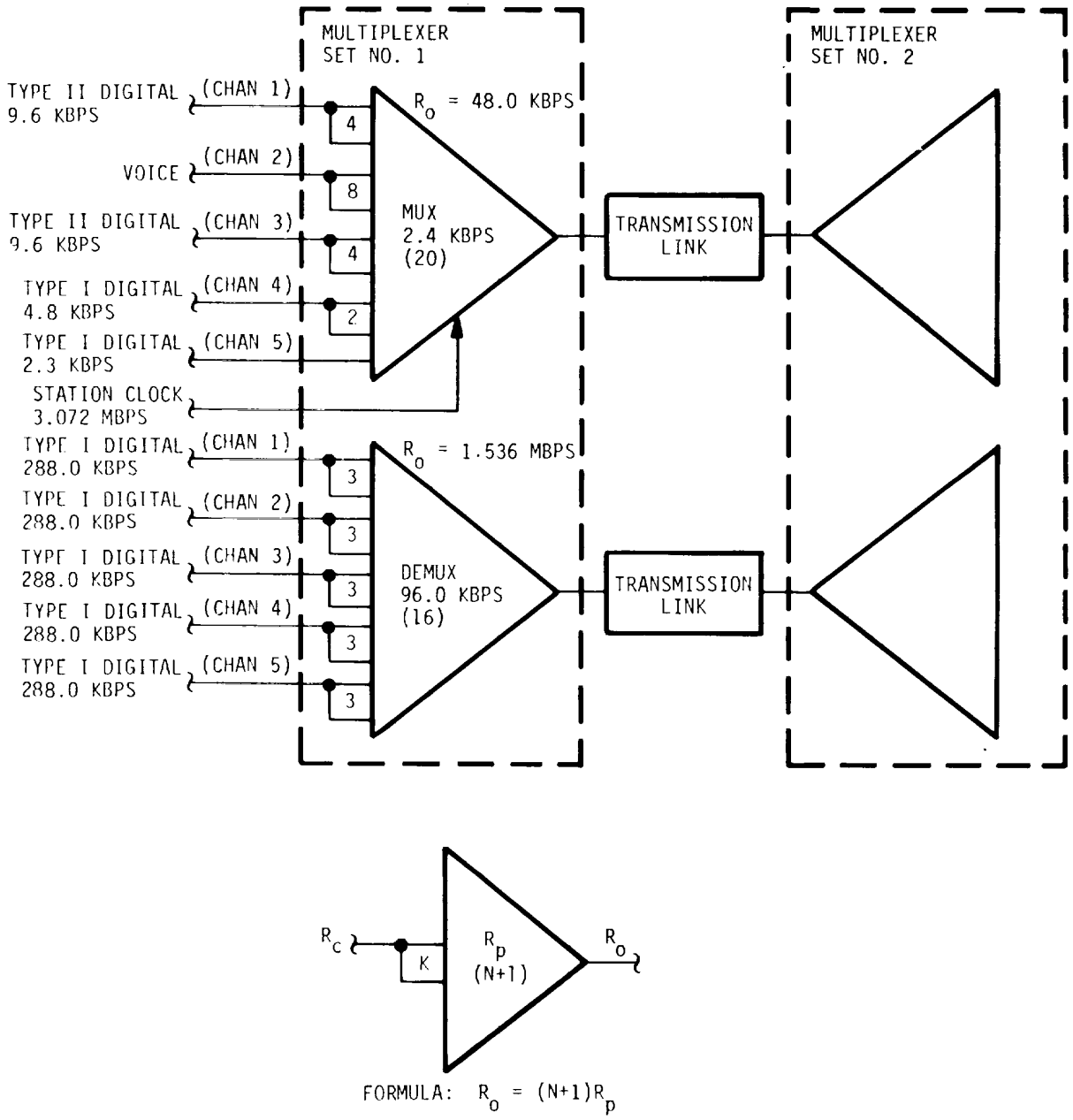
Sheet No.	Figure No.	Function
1	3-5	Provides information necessary to configure channel electronics portion of multiplexer function. Includes information defining channel input rates and forms, and instructions as to type f channel card to be used in processing each channel input.
2	3-6	Provides information necessary to configure common electronics portion of multiplexer function. Includes information defining output rate (R_o) and form, port assignments, and timing source.
3	3-7	Provides information necessary to configure channel electronics portion of demultiplexer function. Includes information defining channel output rates and forms, and instructions as to type of channel card to be used in processing each channel output.
4	3-8	Provides information necessary to configure common electronics portion of demultiplexer function. Includes information defining serial data high-speed input rate (Ro), port assignments, and timing source.

No. 1 in the selected system. In the duplex arrangement shown in figure 3-4, both the multiplexer and demultiplexer are used, but with different sets of channel data rates and forms. A mix of voice, Type I, and Type II (paragraphs 3-20 through 3-26) channel inputs is applied to the multiplexer set. The inputs are multiplexed into a single 48.0-kbps output data stream. The demultiplexer accepts a serial 1.536-Mbps input data stream and demultiplexes it into five Type I channel data outputs.

3-32. MULTIPLEXER CHANNEL ELECTRONICS.

3-33. Sheet 1 of the configuration worksheets (figure 3-5) is prepared to enable setup of the multiplexer channel cards. As shown in the configuration example in figure 3-4, five channels are used to accept a mixture of voice and Type I and Type II data inputs.

3-34. On sheet 1 of the configuration worksheets, each channel's input rate is entered in the applicable INPUT RATE (BPS) R_c block. Since the channel 2 input is voice, the word VOICE is entered instead of a data rate. Next, the type of channel card to be used for the processing of each input channel is listed in the applicable CARD TYPE TE/TR, VE, or RCB block. Thus, for channel 2, an X is entered in the VE (voice encoder) block. Channels 1 and 3 process Type II data inputs that do not have an associated timing input. Such inputs must be processed with a transition encoder/timing recovery (TE/TR) card (paragraph 3-28) operating in either the transition encoder (TE) or timing recovery (TR) mode. A maximum input rate of 400 bps can be processed in the TE mode, and KR_p must be three times the selected input rate range (paragraph 3-24). In the TR mode, the



FORMULA: $R_o = (N+1)R_p$

R_o - MULTIPLEXER OUTPUT RATE

R_p - PORT RATE

K - NUMBER OF PORTS PER CHANNEL
(K = 1 UNLESS OTHERWISE NOTED)

R_c - CHANNEL DATA RATE

(N+1) - TOTAL NUMBER OF PORTS IN USE,
INCLUDING OVERHEAD PORT

6186-62

Figure 3-4. Example of Multiplexer Set Configuration

MULTIPLEXER CHANNEL CONFIGURATION DATA

OUTPUT RATE (R_o) 48000 BPS

CONFIGURATION NO. 5
SHEET 1 OF 4

SITE NO. 17
MULTIPLEXER SET NO. 3
DATE 3-7-76

CHAN NO.	INPUT RATE (BPS) R_c	CARD TYPE TE/TR	CARD TYPE VE	CARD TYPE RCB	RATE CONVERSION DATA 0 1 2 3 4 5 6 7 8 9	PORTS K	INTFC 75	INTFC 6K
1	9600	TR				4		X
2	VOICE		X			8		
3	9600	TR				4		X
4	4800			X		2		X
5	2300			X	0 1 0 1 0 1 0 0 0 0	1		X
6								
7								
8								
9								
10								
11								
12								
13								
14								
15								

6186-144

Figure 3-5. Example of Sheet 1 of Configuration Worksheets

maximum input rate may be 9600 bps (paragraph 3-23). Since the 9600-bps input rate applied to channels 1 and 3 exceeds the maximum TE input rate and KRp is not 3 x $_{Rc,}$ the TR processing mode is selected. Therefore, the letters TR (timing recovery) are entered in the CARD TYPE TE/TR block for these two channels. Channels 4 and 5 process Type I data inputs, and therefore an X is entered in the CARD TYPE RCB block for each channel (paragraph 3-27). In the INTFC block for each channel, an X is entered in either the 75 or 6K (ohms) block, as appropriate, to match the channel source impedance for the given installation under consideration. For example, in figure 3-5, the INTFC block for channel 2 is not marked since the voice input impedance of 600 ohms (balanced) is fixed by channel card design. In the example shown, the source impedance for all digital channel inputs is assumed to be 6K ohms. The worksheet is completed upon entry of the multiplexer output rate $_{(Ro)}$ value of 48000 in the OUTPUT RATE (Ro) BPS block, and entry of the number of the ports (K) assigned to each channel into the PORTS K blocks.

3-35. It should be noted that the input rate (Rc) of 2300 bps for channel 5 is less than that channel's KRp of 2400 bps. In such a situation, coarse rate conversion to KRp must be performed (paragraph 3-19). To enable conversion, a 10-digit binary number is computed and entered on the worksheet. Normally, the computation is performed as part of the actual multiplexer setup process. However, as a convenience to the person setting up the multiplexer, it may be performed at the time the worksheet is prepared. Computation procedures are prescribed in paragraph 3-69, steps 7 and 8.The maximum number of fill bits that may be inserted is 868 bits. A computed fill bit quantity greater than 868 is indicative of an attempted coarse rate conversion that is beyond the capabilities of the multiplexer set. Based on these procedures, the quantity of fill bits required is:

$$\text{Fill bits} = (899)(K)\left(1 - \frac{R_c}{KR_p}\right)$$

$$= (899)(1)(1 - 0.9583333)$$

$$= 37.46$$

$$= 37$$

Since this number is < 868, the conversion may be performed. As shown in table 3-3, the 10-digit binary number that must be used to cause the injection of 37 fill bits is 0101010000 (LSB left) This number is then entered in the RATE CONVERSION DATA block of the worksheet (figure 3-5).

3-36. MULTIPLEXER COMMON ELECTRONICS.

3-37. Sheet 2 of the configuration worksheets (figure 3-6) is prepared to enable setup of the cards in the multiplexer common electronics section. The individual preparing the worksheet uses portions of the information in figure 3-4, combined with a knowledge of the electrical interface cabling and termination arrangements that exist within the facility in which the multiplexer set is installed.

3-38. In figure 3-4, the multiplexer output rate (Ro) is shown as 48.0 kbps; the value 48000 is therefore entered in the OUTPUT RATE (Ro) BPS block of the worksheet. Reference timing is supplied in the form of an external 3.072-MHz station clock. Therefore, an X is entered in the SOURCE EXT block, and the value 3072000 is entered in the EXT FREQ HZ block. All multiplexer set interface circuits are designed to provide an input/output impedance of 6K ohms or 75 ohms. The impedance that matches the station clock source should be selected. For this example, it is assumed that 75 ohms is the proper match; therefore, an X is entered in the INPUT INTFC 75 block.

Table 3-3. Coarse Rate Conversion Strapping Data

Fill Bits	Card Strapping 0123456789
0	0000000000
1	1000000000
2	0100000000
3	1100000000
4	0010000000
5	1010000000
6	0110000000
7	1110000000
8	1001000600
9	0101000000
10	1010000000
11	0110000000
12	0110000000
13	1110000000
14	1110000000
15	0001000000
16	1001000000
17	1001000000
18	0101000000
19	0101000000
20	0110100000
21	1110100000
22	1001100000
23	0101100000
24	1101100000
25	0011100000
26	1011100000
27	0111100000
28	1111100000
29	1000010000
30	0100010000
31	1100010000
32	0010010000
33	1010010000
34	0110010000
35	1110010000
36	1001010000
37	0101010000
38	1101010000
39	0011010000
40	1011010000
41	0111010000
42	1111010000
43	1000110000
44	0100110000
45	1100110000

Fill Bits	Card Strapping 0123456789
46	0010110000
47	1010110000
48	0110110000
49	1110110000
50	1001110000
51	0101110000
52	1101110000
53	1011110000
54	0111110000
55	1111110000
56	1000001000
57	0100001000
58	1100001000
59	0010001000
60	1010001000
61	0110001000
62	1110001000
63	1001001000
64	0101001000
65	1101001000
66	0011001000
67	1011001000
68	0111001000
69	1111001000
70	1000101000
71	0100101000
72	1100101000
73	0010101000
74	1010101000
75	0110101000
76	1110101000
77	1001101000
78	0101101000
79	1101101000
80	1011101000
81	0111101000
82	1111101000
83	1000011000
84	0100011000
85	1100011000
86	0010011000
87	1010011000
88	0110011000
89	1110011000
90	1001011000
91	0101011000

Fill Bits	Card Strapping 0123456789
92	1101011000
93	0011011000
94	1011011000
95	0111011000
96	1111011000
97	1000111000
98	0100111000
99	1100111000
100	0010111000
101	1010111000
102	0110111000
103	1110111000
104	1001111000
105	0101111000
106	1101111000
107	1011111000
108	0111111000
109	1111111000
110	1000000100
111	0100000100
112	1100000100
113	0010000100
114	1010000100
115	0110000100
116	1110000100
117	1001000100
118	0101000100
119	1101000100
120	0011000100
121	1011000100
122	0111000100
123	1111000100
124	1000100100
125	0100100100
126	1100100100
127	0010100100
128	1010100100
129	0110100100
130	1110100100
131	1001100100
132	0101100100
133	1101100100
134	1011100100
135	0111100100
136	1111100100
137	1000010100

Table 3-3. Coarse Rate Conversion Strapping Data (Cont)

Fill Bits	Card Strapping 0123456789
138	0100010100
139	1100010100
140	0010010100
141	1010010100
142	0110010100
143	1110010100
144	1001010100
145	0101010100
146	1101010100
147	0011010100
148	1011010100
149	0111010100
150	1111010100
151	1000110100
152	0100110100
153	1100110100
154	0010110100
155	1010110100
156	0110110100
157	1110110100
158	1001110100
159	0101110100
160	1101110100
161	1011110100
162	0111110100
163	1111110100
164	1000001100
165	0100001100
166	1100001100
167	0010001100
168	1010001100
169	0110001100
170	1110001100
171	1001001100
172	0101001100
173	1101001100
174	0011001100
175	1011001100
176	0111001100
177	1111001100
178	1000101100
179	0100101100
180	1100101100
181	0010101100
182	1010101100
183	0110101100
184	1110101100
185	1001101100
186	0101101100
187	1101101100
188	1011101100
189	0111101100
190	1111101100
191	1000011100
192	0100011100
193	1100011100
194	0010011100
195	1010011100
196	0110011100
197	1110011100
198	1001011100
199	0101011100
200	1101011100
201	0011011100
202	1011011100
203	0111011100
204	1111011100
205	1000111100
206	0100111100
207	1100111100
208	0010111100
209	1010111100
210	0110111100
211	1110111100
212	1001111100
213	0101111100
214	1101111100
215	1011111100
216	0111111100
217	1111111100
218	1000000010
219	0100000010
220	1100000010
221	0010000010
222	1010000010
223	0110000010
224	1110000010
225	1001000010
226	0101000010
227	1101000010
228	0011000010
229	1011000010
230	0111000010
231	1111000010
232	1000100010
233	0100100010
234	1100100010
235	0010100010
236	1010100010
237	0110100010
238	1110100010
239	1001100010
240	0101100010
241	1101100010
242	0011100010
243	1011100010
244	0111100010
245	1111100010
246	1000010010
247	0100010010
248	1100010010
249	0010010010
250	1010010010
251	0110010010
252	1110010010
253	1001010010
254	0101010010
255	1101010010
256	0011010010
257	1011010010
258	0111010010
259	1111010010
260	1000110010
261	0100110010
262	1100110010
263	0010110010
264	1010110010
265	0110110010
266	1110110010
267	1001110010
268	0101110010
269	1101110010
270	1011110010
271	0111110010
272	1111110010
273	1000001010
274	0100001010
275	1100001010

Table 3-3. Coarse Rate Conversion Strapping Data (Cont)

Fill Bits	Card Strapping 0123456789
276	0010001010
277	1010001010
278	0110001010
279	1110001010
280	1001001010
281	0101001010
282	1101001010
283	0011001010
284	1011001010
285	0111001010
286	1111001010
287	1000101010
288	0100101010
289	1100101010
290	0010101010
291	1010101010
292	0110101010
293	1110101010
294	1001101010
295	0101101010
296	1101101010
297	1011101010
298	0111101010
299	1111101010
300	1000011010
301	0100011010
302	1100011010
303	0010011010
304	1010011010
305	0110011010
306	1110011010
307	1001011010
308	0101011010
309	1101011010
310	0011011010
311	1011011010
312	0111011010
313	1111011010
314	1000111010
315	0100111010
316	1100111010
317	0010111010
318	1010111010
319	0110111010
320	1110111010
321	1001111010

Fill Bits	Card Strapping 0123456789
322	0101111010
323	1101111010
324	1011111010
325	0111111010
326	1111111010
327	1000000110
328	0100000110
329	1100000110
330	0010000110
331	1010000110
332	0110000110
333	1110000110
334	1001000110
335	0101000110
336	1101000110
337	0011000110
338	1011000110
339	0111000110
340	1111000110
341	1000100110
342	0100100110
343	1100100110
344	0010100110
345	1010100110
346	0110100110
347	1110100110
348	1001100110
349	0101100110
350	1101100110
351	1011100110
352	0111100110
353	1111100110
354	1000010110
355	0100010110
356	1100010110
357	0010010110
358	1010010110
359	0110010110
360	1110010110
361	1001010110
362	0101010110
363	1101010110
364	0011010110
365	1011010110
366	0111010110
367	1111010110

Fill Bits	Card Strapping 0123456789
368	1000110110
369	0100110110
370	1100110110
371	0010110110
372	1010110110
373	0110110110
374	1110110110
375	1001110110
376	0101110110
377	1101110110
378	1011110110
379	0111110110
380	1111110110
381	1000001110
382	0100001110
383	1100001110
384	0010001110
385	1010001110
386	0110001110
387	1110001110
388	1001001110
389	0101001110
390	1101001110
391	0011001110
392	1011001110
393	0111001110
394	1111001110
395	1000101110
396	0100101110
397	1100101110
398	0010101110
399	1010101110
400	0110101110
401	1110101110
402	1001101110
403	0101101110
404	1101101110
405	1011101110
406	0111101110
407	1111101110
408	1000011110
409	0100011110
410	1100011110
411	0010011110
412	1010011110
413	0110011110

Table 3-3. Coarse Rate Conversion Strapping Data (Cont)

Fill Bits	Card Strapping 0123456789
414	1110011110
415	1001011110
416	0101011110
417	1101011110
418	0011011110
419	1011011110
420	0111011110
421	1111011110
422	1000111110
423	0100111110
424	1100111110
425	0010111110
426	1010111110
427	0110111110
428	1110111110
429	1001111110
430	0101111110
431	1101111110
432	1011111110
433	0111111110
434	1111111110
435	1000000001
436	0100000001
437	1100000001
438	0010000001
439	1010000001
440	0110000001
441	1110000001
442	1001000001
443	0101000001
444	1101000001
445	0011000001
446	1011000001
447	0111000001
448	1111000001
449	1000100001
450	0100100001
451	1100100001
452	0010100001
453	1010100001
454	0110100001
455	1110100001
456	1001100001
457	0101100001
458	1101100001
459	0011100001
460	1011100001
461	0111100001
462	1111100001
463	1000010001
464	0100010001
465	1100010001
466	0010010001
467	1010010001
468	0110010001
469	1110010001
470	1001010001
471	0101010001
472	1101010001
473	0011010001
474	1011010001
475	0111010001
476	1111010001
477	1000110001
478	0100110001
479	1100110001
480	0010110001
481	1010110001
482	0110110001
483	1110110001
484	1001110001
485	0101110001
486	1101110001
487	1011110001
488	0111110001
489	1111110001
490	1000001001
491	0100001001
492	1100001001
493	0010001001
494	1010001001
495	0110001001
496	1110001001
497	1001001001
498	0101001001
499	1101001001
500	0011001001
501	1011001001
502	0111001001
503	1111001001
504	1000101001
505	0100101001
506	1100101001
507	0010101001
508	1010101001
509	0110101001
510	1110101001
511	1001101001
512	0101101001
513	1101101001
514	1011101001
515	0111101001
516	1111101001
517	1000011001
518	0100011001
519	1100011001
520	0010011001
521	1010011001
522	0110011001
523	1110011001
524	1001011001
525	0101011001
526	1101011001
527	0011011001
528	1011011001
529	0111011001
530	1111011001
531	1000111001
532	0100111001
533	1100111001
534	0010111001
535	1010111001
536	0110111001
537	1110111001
538	1001111001
539	0101111001
540	1101111001
541	1011111001
542	0111111001
543	1111111001
544	1000000101
545	0100000101
546	1100000101
547	0010000101
548	1010000101
549	0110000101
550	1110000101
551	1001000101

Table 3-3. Coarse Rate Conversion Strapping Data (Cont)

Fill Bits	Card Strapping 0123456789
552	0101000101
553	1101000101
554	0011000101
555	1011000101
556	0111000101
557	1111000101
558	1000100101
559	0100100101
560	1100100101
561	0010100101
562	1010100101
563	0110100101
564	1110100101
565	1001100101
566	0101100101
567	1101100101
568	1011100101
569	0111100101
570	1111100101
571	1000010101
572	0100010101
573	1100010101
574	0010010101
575	1010010101
576	0110010101
577	1110010101
578	1001010101
579	0101010101
580	1101010101
581	0011010101
582	1011010101
583	0111010101
584	1111010101
585	1000110101
586	0100110101
587	1100110101
588	0010110101
589	1010110101
590	0110110101
591	1110110101
592	1001110101
593	0101110101
594	1101110101
595	1011110101
596	0111110101
597	1111110101

Fill Bits	Card Strapping 0123456789
598	1000001101
599	0100001101
600	1100001101
601	0010001101
602	1010001101
603	0110001101
604	1110001101
605	1001001101
606	0101001101
607	1101001101
608	0011001101
609	1011001101
610	0111001101
611	1000101101
612	1000101101
613	0100101101
614	1100101101
615	0010101101
616	1010101101
617	0110101101
618	1110101101
619	1001101101
620	0101101101
621	1101101101
622	1011101101
623	0111101101
624	1111101101
625	1000011101
626	0100011101
627	1100011101
628	0010011101
629	1010011101
630	0110011101
631	1110011101
632	1001011101
633	0101011101
634	1101011101
635	0011011101
636	1011011101
637	0111011101
638	1111011101
639	1000111101
640	0100111101
641	1100111101
642	0010111101
643	1010111101

Fill Bits	Card Strapping 0123456789
644	0110111101
645	1110111101
646	1001111101
647	0101111101
648	1101111101
649	1011111101
650	0111111101
651	1111111101
652	1000000011
653	0100000011
654	1100000011
655	0010000011
656	1010000011
657	0110000011
658	1110000011
659	1001000011
660	0101000011
661	1101000011
662	0011000011
663	1011000011
664	0111000011
665	1111000011
666	1000100011
667	0100100011
668	1100100011
669	0010100011
670	1010100011
671	0110100011
672	1110100011
673	1001100011
674	0101100011
675	1101100011
676	0011100011
677	1011100011
678	0111100011
679	1111100011
680	1000010011
681	0100010011
682	1100010011
683	0010010011
684	1010010011
685	0110010011
686	1110010011
687	1001010011
688	0101010011
689	1101010011

Table 3-3. Coarse Rate Conversion Strapping Data (Cont)

Fill Bits	Card Strapping 0123456789
690	0011010011
691	1011010011
692	0111010011
693	1111010011
694	1000110011
695	0100110011
696	1100110011
697	0010110011
698	1010110011
699	0110110011
700	1110110011
701	1001110011
702	0101110011
703	1101110011
704	1011110011
705	0111110011
706	1111110011
707	1000001011
708	0100001011
709	1100001011
710	0010001011
711	1010001011
712	0110001011
713	1110001011
714	1001001011
715	0101001011
716	1101001011
717	0011001011
718	1011001011
719	0111001011
720	1111001011
721	1000101011
722	0100101011
723	1100101011
724	0010101011
725	1010101011
726	0110101011
727	1110101011
728	1001101011
729	0101101011
730	1101101011
731	1011101011
732	0111101011
733	1111101011
734	1000011011
735	0100011011

Fill Bits	Card Strapping 0123456789
736	1100011011
737	0010011011
738	1010011011
739	0110011011
740	1110011011
741	1001011011
742	0101011011
743	1101011011
744	0011011011
745	1011011011
746	0111011011
747	1111011011
748	1000111011
749	0100111011
750	1100111011
751	0010111011
752	1010111011
753	0110111011
754	1110111011
755	1001111011
756	0101111011
757	1101111011
758	1011111011
759	0111111011
760	1111111011
761	1000000111
762	0100000111
763	1100000111
764	0010000111
765	1010000111
766	0110000111
767	1110000111
768	1001000111
769	0101000111
770	1101000111
771	0011000111
772	1011000111
773	0111000111
774	1111000111
775	1000100111
776	0100100111
777	1100100111
778	0010100111
779	1010100111
780	0110100111
781	1110100111

Fill Bits	Card Strapping 0123456789
782	1001100111
783	0101100111
784	1101100111
785	1011100111
786	0111100111
787	1111100111
788	1000010111
789	0100010111
790	1100010111
791	0010010111
792	1010010111
793	0110010111
794	1110010111
795	1001010111
796	0101010111
797	1101010111
798	0011010111
799	1011010111
800	0111010111
801	1111010111
802	1000110111
803	0100110111
804	1100110111
805	0010110111
806	1010110111
807	0110110111
808	1110110111
809	1001110111
810	0101110111
811	1101110111
812	1011110111
813	0111110111
814	1111110111
815	1000001111
816	0100001111
817	1100001111
818	0010001111
819	1010001111
820	0110001111
821	1110001111
822	1001001111
823	0101001111
824	1101001111
825	0011001111
826	1011001111
827	0111001111

Table 3-3. Coarse Rate Conversion Strapping Data (Cont)

Fill Bits	Card Strapping 0123456789	Fill Bits	Card Strapping 0123456789	Fill Bits	Card Strapping 0123456789
828	1111001111	842	1000011111	856	1000111111
829	1000101111	843	0100011111	857	0100111111
830	0100101111	844	1100011111	858	1100111111
831	1100101111	845	0010011111	859	0010111111
832	0010101111	846	1010011111	860	1010111111
833	1010101111	847	0110011111	861	0110111111
834	0110101111	848	1110011111	862	1110111111
835	1110101111	849	1001011111	863	1001111111
836	1001101111	850	0101011111	864	0101111111
837	0101101111	851	1101011111	865	1101111111
838	1101101111	852	0011011111	866	1011111111
839	1011101111	853	1011011111	867	0111111111
840	0111101111	854	0111011111	868	1111111111
841	1111101111	855	1111011111		

3-39. The OUTPUT INTERFACE BAL block is marked with an X on the assumption that site cabling is configured for balanced operation. Further, assuming that there are no phase reversals in the site interface circuits or the transmission link, the OUTPUT DATA 0 N and TIMING Ø N blocks are each marked with an X, indicating normal. In normal operation, the positive-to-negative transition of the timing signal occurs in the center of the data bit.

3-40. In figure 3-4, the multiplexer port sampling rate (Rp) is shown as 2.4 kbps; the value 2400 is therefore entered in the PORT RATE (Rp) BPS block of the worksheet. Also, figure 3-4 shows a total port count, including overhead (N + 1), of 20. The N value (19) is entered in the PORTS IN USE (N) block of the worksheet. The PORT STRAPPING blocks are completed to reflect the strapping assignments shown in figure 3-4.Thus, PORT A blocks 1, 5, 13, 17, and 19 are each marked with an X, indicating active, and PORT S blocks 2, 3, 4, 6 through 12, 14, 15, 16, and 18 are each marked with an X, indicating strapped. This completes preparation of sheet 2 of the configuration worksheets to reflect the example shown in figure 3-4. The worksheet provides the information necessary to set up the multiplexer common electronics section as prescribed in paragraph 3-72.

3-41. DEMULTIPLEXER CHANNEL ELECTRONICS.

3-42. Sheet 3 of the configuration worksheets (figure 3-7) is prepared to enable setup of the demultiplexer channel cards. As shown in the configuration example in figure 3-4, the demultiplexer input rate (Ro) is 1.536 Mbps; the value 1536000 is therefore entered in the INPUT RATE (Ro) BPS block. Next, the value 288000 is entered in each of the OUTPUT RATE (BPS) (Rc) blocks for channels 1 through 5. Since all channel outputs are the Type I form (paragraph 3-19), each channel's CARD TYPE SB block is marked with an X, indicating smoothing buffer. Output interfaces are assumed, for this example, to be balanced and without data or timing phase reversals. Therefore, an X is entered in the INTERFACE BAL, DATA Ø N, and TIMING Ø N blocks for each of the

MULTIPLEXER COMMON CONFIGURATION DATA

CONFIGURATION NO. 5
SHEET 2 OF 4

TIMING

OUTPUT RATE (R_o) BPS	SOURCE INT	SOURCE EXT	EXT FREQ HZ	INPUT INTFC 75	INPUT INTFC 6K
48000		X	3072000	X	

PORT RATE (R_p)

BPS
2400

PORTS IN USE (N)

PORTS
19

OUTPUT

INTERFACE BAL	INTERFACE U75	INTERFACE U6K	DATA Ø N	DATA Ø R	TIMING Ø N	TIMING Ø R
X			X		X	

PORT STRAPPING

PORT	A	S	PORT	A	S	PORT	A	S	PORT	A	S
1	X		9		X	17	X		25		
2		X	10		X	18		X	26		
3		X	11		X	19	X		27		
4		X	12		X	20			28		
5	X		13	X		21			29		
6		X	14		X	22			30		
7		X	15		X	23			31		
8		X	16		X	24					

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Figure 3-6. Example of Sheet 2 of Configuration Worksheets

DEMULTIPLEXER CHANNEL CONFIGURATION DATA

INPUT RATE (R_o) 1536000 BPS

CONFIGURATION NO. 5

SHEET 3 OF 4

CHAN NO.	OUTPUT RATE (BPS) (R_c)	CARD TYPE TD	CARD TYPE VD	CARD TYPE SB	RATE CONVERSION DATA 0 1 2 3 4 5 6 7 8 9	INTERFACE BAL	INTERFACE U75	INTERFACE U6K	DATA Ø N	DATA Ø R	TIMING Ø N	TIMING Ø R	PORTS (K)
1	288000			X		X			X		X		3
2	288000			X		X			X		X		3
3	288000			X		X			X		X		3
4	288000			X		X			X		X		3
5	288000			X		X			X		X		3
6													
7													
8													
9													
10													
11													
12													
13													
14													
15													

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Figure 3-7. Example of Sheet 3 of Configuration Worksheets

five channels. Similarly, the value 3 is entered in the PORTS (K) block for each channel. This completes preparation of sheet 3 of the configuration worksheets for the example shown in figure 3-4.

3-43. DEMULTIPLEXER COMMON ELECTRONICS.

3-44. Sheet 4 of the configuration worksheets (figure 3-8) is prepared to enable setup of the demultiplexer common electronics section. As shown in the configuration example in figure 3-4, the demultiplexer input rate (Ro) is 1.536 Mbps; the value 1536000 is therefore entered in the INPUT RATE (Ro) BPS block. Assuming no phase reversals in the transmission link from the far-end multiplexer, the DATA Ø N and TIMING Ø N blocks are each marked with an X, indicating normal. Since the 1.536-Mbps input is assumed for this example to come from a 75-ohm driver, an X is entered in the INTFC 75 block. A link error rate environment of one error per hundred bits (1/100) is considered acceptable for this example; however, it is desired to indicate by an alarm when the error rate exceeds this value, and therefore an X is entered in the ERROR RATE THRESHOLD 10-2 block. Port rate and port assignment entries are made, based on the example in figure 3-4; accordingly, the value 96000 is entered in the PORT RATE (Rp) BPS block, and the number 15 is entered in the PORTS IN USE (N) block. PORT A blocks 1, 4, 7, 10, and 13 are each marked with an X, indicating active, and PORT S blocks 2, 3, 5, 6, 8, 9, 11, 12, 14, and 15 are each marked with an X, indicating strapped. This completes preparation of the four configuration worksheets for the multiplexer set configuration shown in figures 3-5 through 3-8.

3-45. SUPPLEMENTAL CONFIGURATION CONSIDERATIONS.

3-46. The preceding discussions relative to configuration of the multiplexer set have considered its application to be within an overall communications system. Because all elements of such a system must operate in a fully compatible manner, key factors such as output rate (Ro), port rate (Rp), and port strapping assignments for a given multiplexer are fixed by overall system requirements and are not subject to selection by the individual multiplexer set user. In such system applications, the configuration of a selected multiplexer set may be less than optimum in terms of input/output efficiency, while overall system efficiency is in fact optimized. Efficiency here is defined as the proper processing of all applied channel inputs while maintaining the lowest possible output rate (Ro). There are undoubtedly some applications, however, in which one or more factors of a multiplexer set's configuration are left to user selection. In these situations, the user should strive to maximize overall input/output efficiency while continuing to properly process all applied channel inputs.

3-47. The user must consider two primary sources of inefficiency when configuring the multiplexer set. The first source of multiplexer set inefficiency relates to the fact that regardless of configuration, one port is always used for overhead servicing. Since this port occurs at the same port rate (Rp) as all other ports, its contribution to inefficiency can be minimized by selection of the lowest possible port rate consistent with proper processing of the applied channel inputs. With a fixed set of input rates to be processed, reductions in port rate will necessarily require an increase in the

DEMULTIPLEXER COMMON CONFIGURATION DATA

CONFIGURATION NO. 5
SHEET 4 OF 4

TIMING

INPUT RATE (R_e) BPS: 1536000

PORT RATE (R_p) BPS: 96000

INPUT

INTFC 75	INTFC 6K	DATA Ø N	DATA Ø R	TIMING Ø N	TIMING Ø R
X		X		X	

PORTS IN USE (N)

PORTS: 15

ERROR RATE THRESHOLD

10^{-1}	10^{-2}	10^{-3}	10^{-4}
	X		

PORT STRAPPING

PORT	A	S	PORT	A	S	PORT	A	S	PORT	A	S
1	X		9		X	17			25		
2		X	10	X		18			26		
3		X	11		X	19			27		
4	X		12		X	20			28		
5		X	13	X		21			29		
6		X	14		X	22			30		
7	X		15		X	23			31		
8		X	16			24					

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Figure 3-8. Example of Sheet 4 of Configuration Worksheets

total number of ports used. The second major source of multiplexer set inefficiency occurs when the set of input channel rates to be processed is from a mixture of rate families. Since the port rate (Rp) selected for a given configuration is applied to all ports, processing of channel input rates not of the family to which the port rate is related will necessarily induce inefficiency by requiring the use of coarse rate conversion. Inefficiencies resulting from the processing of inputs from multiple-rate families can be minimized by selection of a port rate related to the predominant family.

3-48. The following paragraphs provide brief discussions and examples regarding reduction of inefficiencies resulting from the above-mentioned sources.

3-49. In examining the effects upon overall input/output efficiency resulting from port rate (Rp) selection, consider the example depicted in configuration A of figure 3-9. Five input channels at rates of 48, 48, 8, 8, and 8 kbps are applied to the multiplexer's channel inputs. A port rate ( ) equal to the lowest input rate of 8 kps is selected. This requires the use of six ports for each of the 48-kbps inputs (48/8 = 6) and one port (8/8 = 1) for each of the 8-kbps inputs. The total number of ports used, including the overhead port, is 16. This satisfies the requirements that the number of ports assigned to all channels (N) be equal to or greater than 15. Output rate is simply the product of Rp and the total number of ports, or 8 kbps x 16 = 128 kbps. Expressed as a percentage, overall efficiency for the example shown is expressed as:

$$\frac{(48 \times 2) + (8 \times 3)}{128} \times 100 = 93.75 \text{ percent.}$$

3-50. As shown in configuration B of figure 3-9, the channel inputs remain unchanged from the previous example, but the port rate (Rp) is reduced from 8 kbps to 4 kbps. The number of ports required to process the channel data is doubled from 15 to 30, requiring a total of 31 ports in this configuration. Output rate (Ro) is again the product of port rate and total port count, or 4 kbps x 31 = 124 kbps. Note that this output rate is 4 kbps lower than the 128 kbps required in the first example. The overall efficiency of configuration B in figure 3-9 is expressed as:

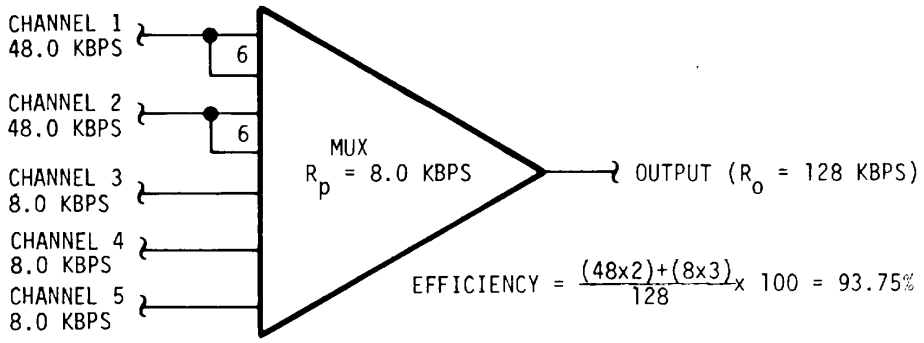
$$\frac{(48 \times 2) + (8 \times 3)}{124} \times 100 = 96.77 \text{ percent.}$$

The efficiency difference of 3.02 percent between the two examples illustrates the importance of processing applied inputs at the lowest possible port rate consistent with the number of ports available.

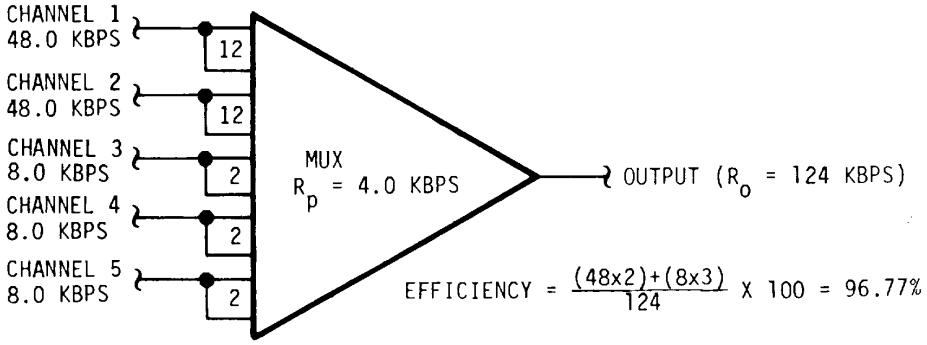
3-51. Configurations A and B of figure 3-10 show the effects of processing mixed input rate families upon overall input/output efficiency.

3-52. Three rate families frequency encountered in digital communications applications are the 8000N, 600N, and C x 75 x 2n. The values selected for N, C, and n in these families are positive integers. Configuration A of figure 3-10 depicts a multiplexer set in which rates from all three families are processed: input channels 1 and 2 of the 8000N family, where N equals 1; channel 3 is of the 600N family, where N equals 10; and channel 4 is of the C x 75 x 2n family, where C equals 23 and n equals 3.

3-53. Representing two of the four channels applied, the 8000N family is predominant. Based on the previously established rule that mixed rate families should be processed with a port rate related to the predominant family, a port rate (Rp) of 2 kbps is used in the example depicted in configuration A of figure 3-10.The 2kbps rate is a

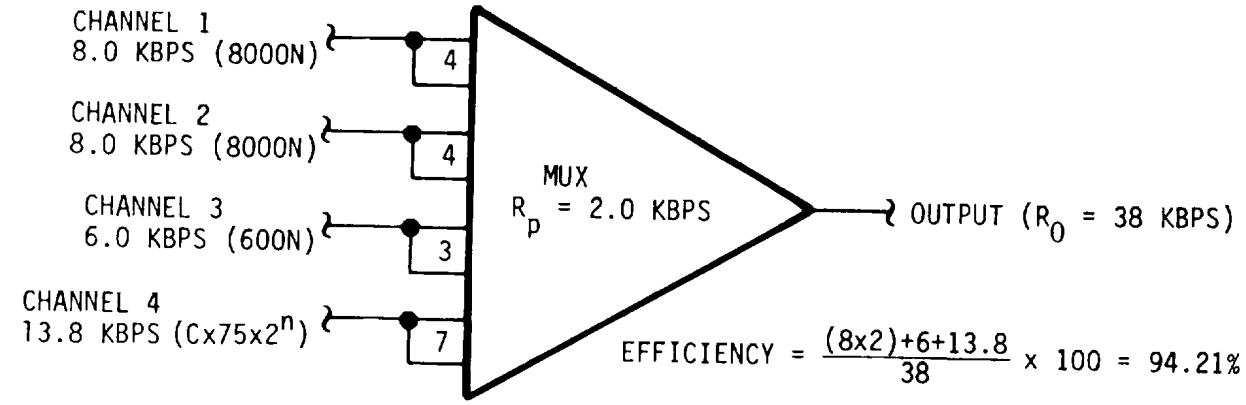


A. SYSTEM USING 8.0 KBPS PORT RATE

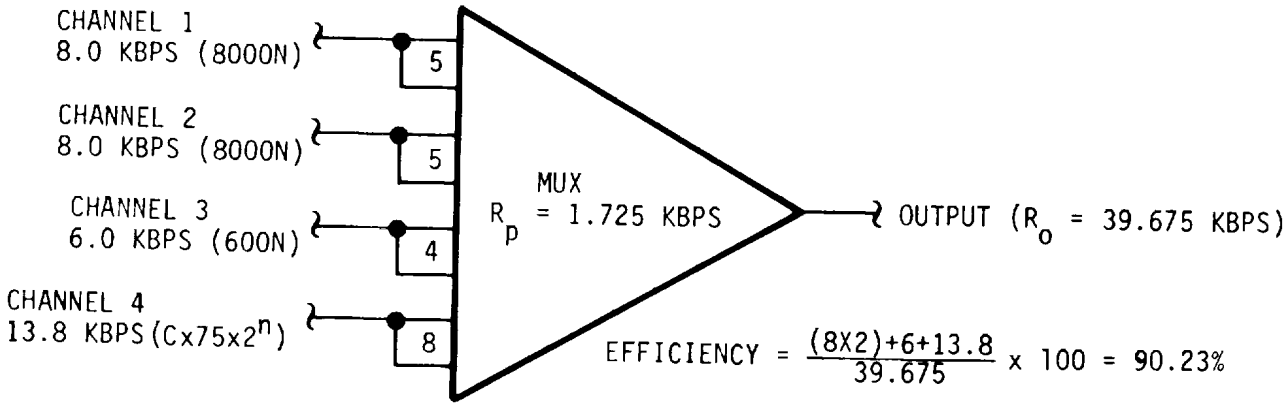


B. SYSTEM USING 4.0 KBPS PORT RATE

Figure 3-9. Port Rate Impact Upon Input/Output Efficiency



A. SYSTEM WITH PORT RATE RELATED TO PREDOMINANT RATE FAMILY



B. SYSTEM WITH PORT RATE NOT RELATED TO PREDOMINANT RATE FAMILY

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Figure 3-10. Input Rate Mix Impact Upon Input/Output Efficiency

direct submultiple of 8000. By chance, the port rate is also a direct submultiple of the 6-kbps (600N family) input to channel 3. A total of 19 ports (including overhead) is used in the configuration, and with a 2-kbps Rp, the Ro is 38 kbps (2 kbps x 19 = 38 kbps). Overall efficiency is expressed as:

$$\frac{(8 \times 2) + 6 + 13.8}{38} \times 100 = 94.21 \text{ percent.}$$

3-54. The example depicted in configuration B of figure 3-10 processes the same inputs as those discussed above, but uses a port rate that is a submultiple of the C x 75 x 2n family. This port rate (1.725 kbps) requires that the port strapping assignments of the previous example be modified to ensure that the product of port rate and port quantity for each channel is equal to or greater than the applied channel input rate. Differences between this product and the input channel rate for channels 1, 2, and 3 are adjusted internal to the multiplexer set by means of coarse rate conversion. In this example, the total port count, including overhead, is 23. The output rate is 1.725 kbps x 23 = 39.675 kbps, and overall input/output efficiency is expressed as:

$$\frac{(8 \times 2) + 6 + 13.8}{39.675} \times 100 = 90.23 \text{ percent.}$$

The efficiency is 3.98 percent lower than that shown in configuration A of figure 3-10, and shows the effects that result when a selected port rate is not related to the more predominant of mixed input rate families. It should also be noted that the decreased efficiency is experienced with a configuration that uses a greater total number of ports (23 versus 19) and a lower port rate. As discussed in paragraph 3-49, and without a mixture of input rate families, an increased port count and lowered port rate tend to increase efficiency.

3-55. The preceding paragraphs have identified and discussed the major sources of multiplexer set input/output inefficiency, and have provided examples of how the inefficiency can be confined. Attention to efficiency, and the selection of configurations to enhance it, is of importance only when the individual multiplexer set user is not otherwise restricted by superseding system configuration dictates.

3-56. VOICE PROCESSING GROUND RULES.

3-57. In the processing of voice channel data, a port rate (Rp) of 19.2 kbps or greater is preferred. In such cases, the voice input is processed by using a single port (K = 1). However, there are certain situations where the use of lower port rates and/or port strapping arrangements may be desired. The ground rules applicable to the processing of voice inputs with port rates lower than 19.2 kbps, or port strapping (K > 2), are as follows:

a. For port rates of 19.2 kbps or greater, improved voice transmission quality may be obtained by using two ports (K = 2), provided that the first (active) port assigned to the voice channel is an even number and the total number of ports used within the multiplexer set, including overhead, is an even number (N + 1 = 16, 18, 20).

b. For port rates between 9.6 and 19.2 kbps, two ports should be used (K = 2), provided the total multiplexer used port count (N + 1) is an even number (N + 1 = 16, 18, 20). If N + 1 is an odd number, a channel sampling rate (KRp) of 38.4 kbps or greater should be used.

c. For port rates less than 9.6 kbps, acceptable voice transmission quality may be obtained, provided that a port strapping arrangement yielding a channel sampling rate (KRp) of 38.4 kbps or greater is used.

3-58. SPECIAL DEMULTIPLEXER OUTPUT SMOOTHING OPTIONS.

3-59. Rate variations and/or offsets appearing in digital channel inputs applied to the multiplexer are adjusted by a bit stuffing process as discussed in paragraph 5-30. At the demultiplexer channel output, an inverse function termed smoothing is performed (paragraph 5-64). Unlike the stuffing operation, which makes an instantaneous 1-bit adjustment in a channel's timing, the demultiplexer smoothing process accomplishes a 1-bit output timing adjustment over an extended interval of channel bit times. The extended rather than instantaneous timing adjustment is necessary to ensure proper synchronization of sink instruments connected to the demultiplexer channel outputs.

3-60. Smoothing circuits in the SB and TD cards are designed to perform a 1-bit output timing adjustment over an interval not exceeding 1000 channel data bit times. However, the smoothing (or slew) rate may still exceed the synchronization capabilities of certain sink instruments. For this reason, options are incorporated on the SB card to enable extension of the smoothing interval for channel data rates between 19.2 kbps and 3.0 Mbps. More specifically, the options provide the following: (1) a smoothing interval of 1500 or more output data bit times for channel data rates over the range of 19.2 kbps to 3.0 Mbps; and (2) a smoothing interval of 2000 or more output data bit times for a channel data rate of 50.0 kbps. The extended smoothing interval options are applicable for multiplexer channel inputs with rate variations of plus or minus 250 parts per million (+250 ppm) or less. Any SB card that is processing a channel rate (Rc) of 1.5 Mbps or higher must have the extended smoothing option selected. In all other tandem and non-tandem applications which involve channel rates between 19.2 kbps and 1.5 Mbps, the extended smoothing option need only be selected on those SB cards which interface with the user's sink instrument.

3-61. Extended smoothing interval options are provided only on the SB card, since channel data rates processed by the TD card are below 19.2 kbps. The options are selected by switch S12 on the SB card as follows: (1) if the channel data rate is between 19.2 and 187.0 kbps (within the B range of switch S5), switch S12 is set to the B'A position; and (2) if the channel data rate is between 187.0 kbps and 3.0 Mbps (within the A range of switch S5), switch S12 is set to the A' position. When a given multiplexer set application requires use of an extended smoothing interval option, appropriate supplementary instructions should be added to the configuration worksheets that describe the configuration to the operator.

3-62. For those applications in which the demultiplexer output smoothing rate must be confined more closely than is possible with the options provided on the SB card, a narrow band smoothing buffer (NBSB) card is provided. The NBSB card may be used for specific channel output data rates of 19.2, 38.4, 50.0, 76.8, or 153.6 kbps .At each of these rates, the NBSB output smoothing interval is 20,000 data bit times for a 1-bit shift or slew in the card's output timing signal.

3-63. When a particular application requires use of the NBSB card, the letters NP are entered in the CARD TYPE SB block on sheet 3 of the configuration worksheets (figure 3-7)Thus the individual setting up the multiplexer set will be informed that the NBSB card instead of a conventional SB card must be used.

SECTION III

EQUIPMENT PREPARATION PROCEDURES

3-64. PREPARATION CONSIDERATIONS.

3-65. This section contains the detailed procedures for configuring the multiplexer and demultiplexer functions in the multiplexer set. The procedures are keyed to the information as presented on the configuration worksheets (figure 3-11). To ensure that a multiplexer set is completely and properly set up for the designated system application, the configuration worksheets should be duplicated and completed for each equipment configuration being used. The configuration worksheets also serve as a record of the configuration and may be subsequently used as checklists to ensure that all multiplexer set switch settings have been properly performed.

3-66. MULTIPLEXER CHANNEL ELECTRONICS SETUP PROCEDURES.

3-67. The information required for the setup of multiplexer channel cards for a given configuration is provided on sheet 1 of the configuration worksheets (figure 3-11). Sheet 1 provides the following information: the identity of each active channel; each channel's input data rate (Rc); the number of ports (K) assigned to the channel; and the type of channel card to be used in processing each channel data input. Space is provided for entry, when applicable, of channel card input impedance data and coarse rate conversion strapping data. Space is also provided for entry of the multiplexer output rate (Ro). Paragraphs 3-68 through 3-71 prescribe the setup procedures for the three optional multiplexer channel cards (paragraph 3-27) based on the information provided.

3-68. RCB CARD (P/N 61864010).

3-69. For each channel that uses an RCB card, set up the card as follows (refer to figure 3-12 for all switch locations):

1. Note the multiplexer output rate (Ro) entered on the worksheet. If Ro is less than 2000 bps, set S1 to the Ro < 2KHZ position. If Ro is 2000 bps or higher, set S1 to the Ro > 2KHZ position.

2. Note the channel INTFC 75 or 6K block on the worksheet; set S4 and S5 to the indicated 75 or 6K position.

3. Set S6 to the ON position.

NOTE

Setting S6 to the OFF position will inhibit the display of any card errors detected by the RCB diagnostic circuits.

4. Set S7 to the ON position,

NOTE

Setting S7 to the OFF position will inhibit the display of any out-of-tolerance (OOT) condition detected by the RCB card diagnostic circuits.

5. Refer to the worksheet, and note in the PORTS K blocks the number of ports (K) assigned to each channel. Note the port rate (Rp) shown on sheet 2 of the worksheets; multiply K and

MULTIPLEXER CHANNEL CONFIGURATION DATA

OUTPUT RATE (R_o) _____ BPS

CONFIGURATION NO. _____
SHEET 1 OF 4

SITE NO. _____

MULTIPLEXER SET NO. _____

DATE _____

CHAN NO.	INPUT RATE (BPS) R_c	CARD TYPE TE/TR	CARD TYPE VE	CARD TYPE RCB	RATE CONVERSION DATA 0 1 2 3 4 5 6 7 8 9	PORTS K	INTFC 75	INTFC 6K
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								
13								
14								
15								

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Figure 3-11. Configuration Worksheets (sheet 1 of 4)

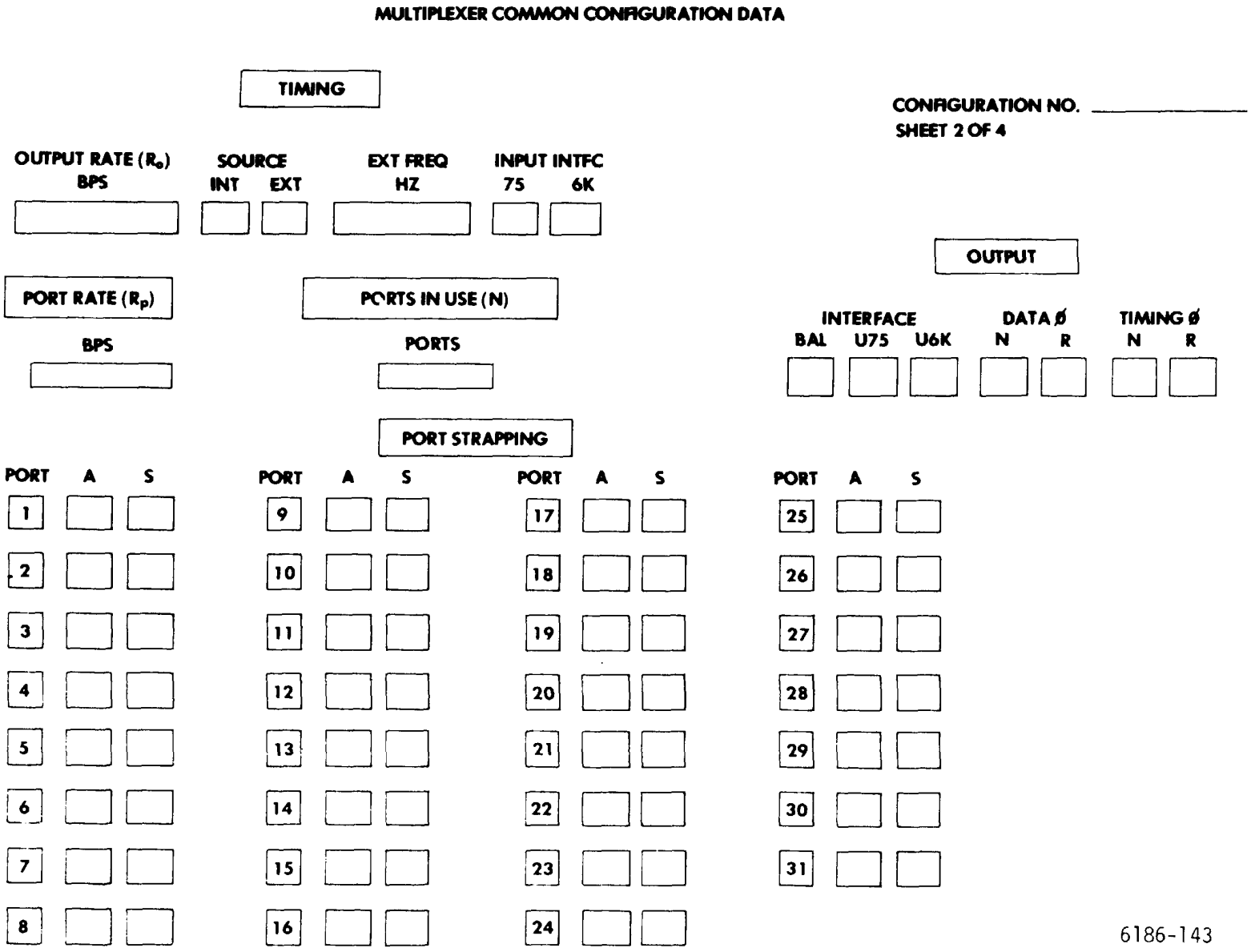

Figure 3-11. Configuration Worksheets (sheet 2 of 4)

DEMULTIPLEXER CHANNEL CONFIGURATION DATA

INPUT RATE (R_a) _____ BPS

CONFIGURATION NO. _____
SHEET 3 OF 4

CHAN NO.	OUTPUT RATE (BPS) (R_c)	CARD TYPE TD	VD	SB	RATE CONVERSION DATA 0	1	2	3	4	5	6	7	8	9	INTERFACE BAL	U75	U6K	DATA Ø N	R	TIMING Ø N	R	PORTS (K)
1																						
2																						
3																						
4																						
5																						
6																						
7																						
8																						
9																						
10																						
11																						
12																						
13																						
14																						
15																						

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Figure 3-11. Configuration Worksheets (sheet 3 of 4)

DEMULTIPLEXER COMMON CONFIGURATION DATA

CONFIGURATION NO. _____
SHEET 4 OF 4

TIMING

INPUT RATE (R_o)
BPS

PORT RATE (R_p)

BPS

PORTS IN USE (N)

PORTS

INPUT

INTFC		DATA Ø		TIMING Ø	
75	6K	N	R	N	R

ERROR RATE THRESHOLD

10^{-1}	10^{-2}	10^{-3}	10^{-4}

PORT STRAPPING

PORT	A	S	PORT	A	S	PORT	A	S	PORT	A	S
1			9			17			25		
2			10			18			26		
3			11			19			27		
4			12			20			28		
5			13			21			29		
6			14			22			30		
7			15			23			31		
8			16			24					

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Figure 3-11. Configuration Worksheets (sheet 4 of 4).

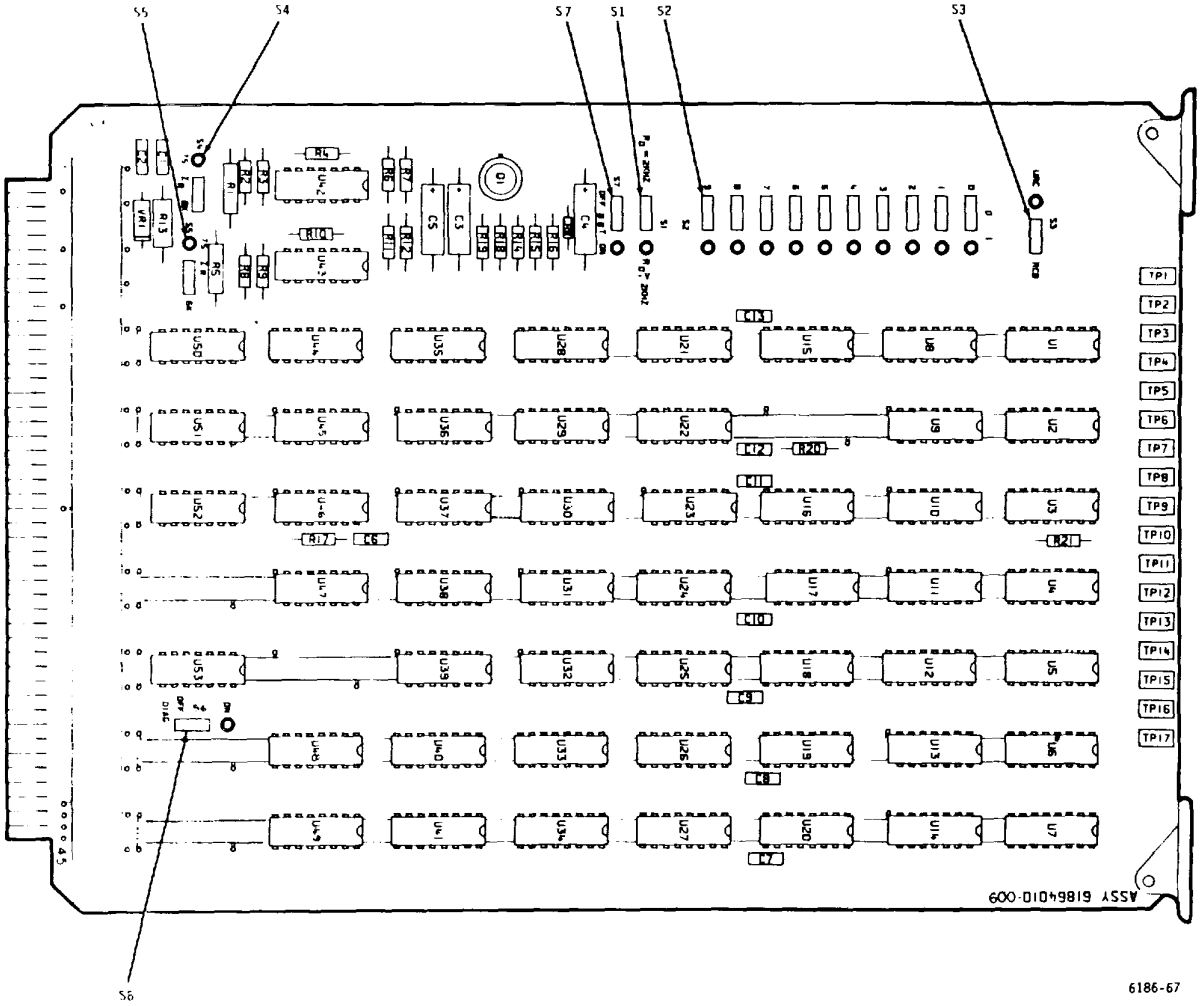


Figure 3-12. RCB Card - Switch Location Diagram

RD, and compare this value (KRp) with the channel's input data rate (Rc).

6. If R_c is equal to KRp (R_c = KRp), set S3 to the RCB position, which completes the RCB card setup process. If $_{Rc}$ is less than KRp (R_c < KRp), set S3 to the URC position and perform steps 7 through 9.

NOTE

In cases where R_c < KRp, coarse rate conversion of R_c to KRp must be performed by the multiplexer. To enable this conversion, a fill bit value must be computed and set into the RCB by 10-position switch S2.

7. Determine the quantity of fill bits required, using the expression:

$$\text{Fill bits} = 899K \left(1 - \frac{R_c}{KR_p}\right)$$

where

K = quantity of ports assigned to the channel (from worksheet)

R_c= channel data rate (from worksheet)

Rp = port rate (from worksheet).

NOTE

To ensure a proper computation of fill bit quantity, the value of 1 - Rc/KRp must be determined to seven decimal places. Overall fill bit quantity, when computed, should be rounded to the nearest whole number; i.e., 316.7 is rounded to 317, etc. The largest number of fill bits the multiplexer can process is 868. If the computed quantity of fill bits exceeds this value, a check for computational errors is suggested. A correctly computed fill bit value greater than 868 is indicative of incorrect configuration data on the worksheet.

8. Refer to table 3-3 and locate the fill bit quantity computed in step
7. Enter the 10-digit binary number associated with this quantity in the RATE CONVERSION DATA block on sheet 1 of the worksheets.

NOTE

In step 9, ensure that the 10-digit number is inserted properly and the 0 and 9 positions are not inadvertently reversed. Removal of all switch jumpers prior to starting the number entry process is suggested.

9. Set 10-digit switch S2 on the RCB card to reflect the 10-digit binary number recorded on the worksheet, This completes the RCB card setup process.

10. Install the RCB card in its appropriate slot (1 through 15) in the MULTIPLEXER row.

3-70. TE/TR CARD (P/N 61864060). For each channel that uses a TE/TR card, set up the card as follows (refer to figure 3-13 for all switch locations):

1. Note the channel INTFC 75 or 6K block on the worksheet; set S4 to the indicated 75 or 6K position.

2. Set S6 and S7 to the NORM position.

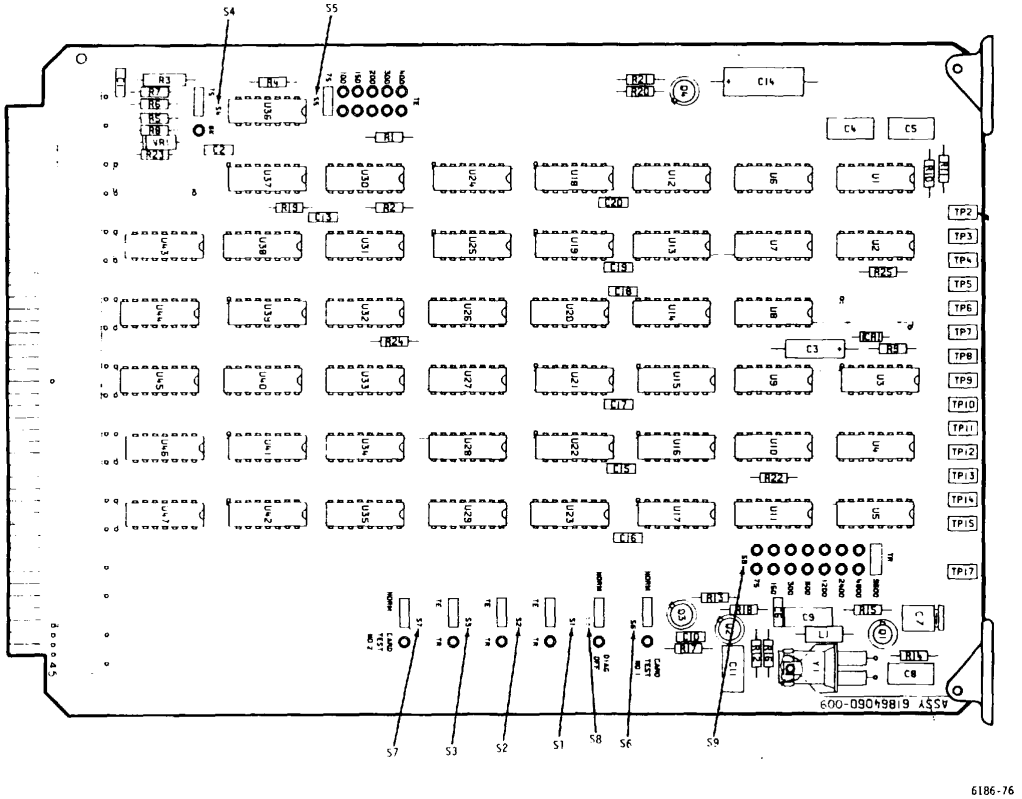


Figure 3-13. TE/TR Card - Switch Location Diagram

3. Set S8 to the NORM position.

NOTE

Failure to set S8 to the NORM position will inhibit the display of any errors detected by the TE/TR card diagnostic circuits.

4. Refer to sheet 1 of the worksheets and note if the CARD TYPE TE/TR block is marked TE or TR. Set card switches S1, S2, and S3 to the indicated TE or TR position. If S1, S2, and S3 are set to the TE position, proceed to step 5. If S1, S2, and S3 are set to the TR position, proceed to step 6.

5. Multiply the number of ports (K) assigned to the channel as indicated on sheet 1 and the port rate (Rp) entered on sheet 2 of the worksheets. Divide the product (KRp) by 3, and set S5 on the TE/TR card to the computed KRp/3 value. This completes the setup of the TE/TR card for the TE mode of operation.

NOTE

The computed KRp/3 value must exactly match one of the six settings of S5. If a match is not obtained, a check of the computation is suggested. A correct computation not yielding a match with one of the settings of S5 indicates incorrect configuration data on the worksheet.

6. Set S9 to the channel data rate listed on the worksheet. This completes the setup of the TE/TR card for the TR mode of operation.

7. Install the TE/TR card in the appropriate slot (1 through 15) in the MULTIPLEXER row.

3-71. VE CARD (P/N 61864070). No setup of the VE card is required. Install a VE card in the appropriate slot in the MULTIPLEXER row for each voice channel input listed on the worksheet.

3-72. MULTIPLEXER COMMON ELECTRONICS SETUP PROCEDURES.

3-73. Procedures for configuring the cards comprising the common electronics portion of the multiplexer are prescribed in paragraphs 3-74 through 3-77. The information necessary to perform these procedures is contained on sheet 2 of the configuration worksheets (figure 3-11).

3-74. RT CARD (P/N 61864150). The RT card is located in slot 16 of the MULTIPLEXER row. Set up the card as follows (refer to figure 3-14 for all switch locations):

1. Refer to the OUTPUT INTERFACE BAL, U75, and U6K block on sheet 2 of the configuration worksheets, and set switches S2E and S8E to the indicated position.

2. If the OUTPUT INTERFACE BAL block is marked, set switches S2A, S2B, S2C, S2D, S8A, S8B, S8C, and S8D to the B position. If the OUTPUT INTERFACE U75 or 6K block is marked, set the switches to the U position.

3. Set both jumpers of switch S7 to the N (normal) or R (reversed) position as indicated in the DATA Ø N or R block on the worksheet.

4. Set both jumpers of switch S1 to the N (normal) or R (reversed) position as indicated in the TIMING Ø N or R block on the worksheet.

5. Set S3 to the 0 position.

6. Refer to the TIMING section on the worksheet, and note which TIMING SOURCE block (INT or EXT) is marked. Set S5 to the indicated position. If S5 is set to the EXT position, proceed to step 14.

NOTE

Row 1 of table 3-4 is applicable only to the RT card fitted with an oscillator whose output frequency is 9, 830, 400 Hz. In such cases, proceed to step 7. When an oscillator of a different frequency is used, and the desired R_o value appears in other than row 1 of table 3-4, perform the procedures in steps 8, 9, and 10. If the desired R_o value is not listed in table 3-4, perform the procedures in steps 11 and 12.

7. Refer to row 1 of table 3-4, and locate the output rate (R_o) value entered on sheet 2 of the worksheets. Set S6 on the RT card to the position corresponding to the column of table 3-4 in which the desired R_o value appears. Proceed to step 13.

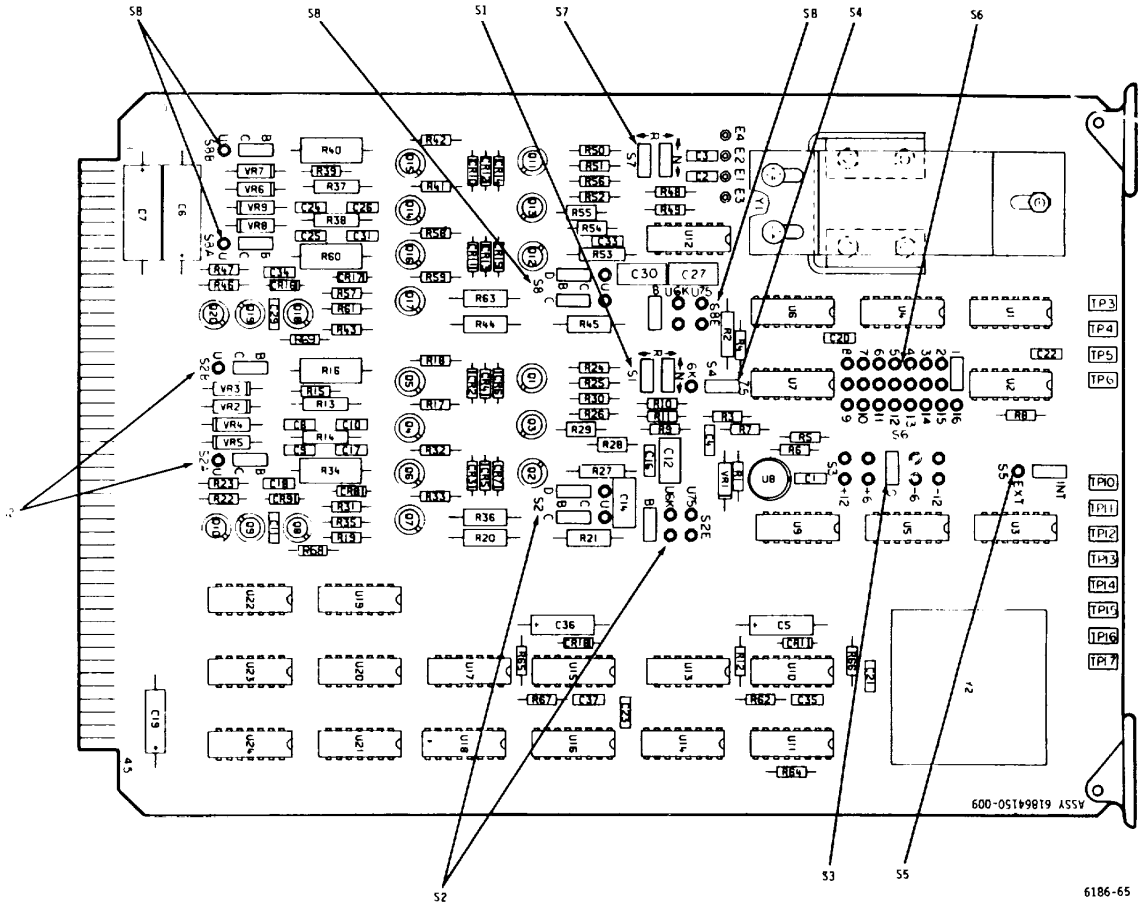


Figure 3-14. RT Card - Switch Location Diagram

8. Determine the row and column of table 3-4 in which the desired R_o value is located

9. Determine the basic frequency of the oscillator (Y1) installed on the RT card.

10. Starting with the column of table 3-4 in which the desired R_o value is located, count that column and the

Table 3-4. Reference Timer Rate Selection Data

Column								
Row	1	2	3	4	5	6	7	8
1	9,830,400	4,915,200	2,457,600	1,228,800	614,400	307,200	153,600	76,800
2	9,523,200	4,761,600	2,380,800	1,190,400	595,200	297,600	148,800	74,400
3	9,216,000	4,608,000	2,304,000	1,152,000	576,000	288,000	144,000	72,000
4	8,908,800	4,454,400	2,227,200	1,114,600	556,800	278,400	139,200	69,600
5	8,601,600	4,300,800	2,150,400	1,075,200	537,600	268,800	134,400	67,200
6	8,294,400	4,147,200	2,073,600	1,036,800	518,400	259,200	129,600	64,800
7	7,987,200	3,993,600	1,996,800	998,400	499,200	249,600	124,800	62,400
8	7,680,000	3,840,000	1,920,000	960,000	480,000	240,000	120,000	60,000
9	7,372,800	3,686,400	1,843,200	921,600	460,800	230,400	115,200	57,600
10	7,065,600	3,532,800	1,766,400	883,200	441,600	220,800	110,400	55,200
11	6,758,400	3,379,200	1,689,600	844,800	422,400	211,200	105,600	52,800
12	6,451,200	3,225,600	1,612,800	806,400	403,200	201,600	100,800	50,400
13	6,144,000	3,072,000	1,536,000	768,000	384,000	192,000	96,000	48,000
14	5,836,800	2,918,400	1,459,200	729,600	364,800	182,400	91,200	45,600
15	5,529,600	2,764,800	1,382,400	691,200	345,600	172,800	86,400	43,200
16	5,222,400	2,611,200	1,305,600	652,800	326,400	163,200	81,600	40,800
17	4,915,200	2,457,600	1,228,800	614,400	307,200	153,600	76,800	38,400
Column								
Row	9	10	11	12	13	14	15	16
1	38,400	19,200	9,600	4,800	2,400	1,200	600	300
2	37,200	18,600	9,300	4,650	2,325	1162.5	581.25	290.625
3	36,000	18,000	9,000	4,500	2,250	1125	562.5	281.25
4	34,800	17,400	8,700	4,350	2,175	1087.5	543.75	271,875
5	33,600	16,800	8,400	4,200	2,100	1050	525	262.5
6	32,400	16,200	8,000	4,050	2,075	1037.5	518.75	259.375
7	31,200	15,600	7,800	3,900	1,950	975	487.5	243.75
8	30,000	15,000	7,500	3,750	1,875	937.5	468.75	243.375
9	28,800	14,400	7,200	3,600	1,800	900	450	225
10	27,600	13,800	6,900	3,450	1,725	862.5	431.25	215.625
11	26,400	13,200	6,600	3,300	1,650	825	412.5	206.25
12	25,200	12,600	6,300	3,150	1,575	787.5	393.75	196.875
13	24,000	12,000	6,000	3,000	1,500	750	375	187.5
14	22,800	11,400	5,700	2,850	1,425	712.5	356.25	178.125
15	21,600	10,800	5,400	2,700	1,350	675	337.5	168.75
16	20,400	10,200	5,100	2,550	1,275	637.5	318.75	159.375
17	19,200	9,600	4,800	2,400	1,200	600	300	150

columns to the left of that column, on the same row, until the column containing the installed oscillator's frequency is reached. Set S6 on the RT card to the number of columns counted. For example, assume that an $_{Ro}$ of 120, 000 bps (row 8, column 7) is desired and the RT card is fitted with an oscillator whose output frequency is 1, 920, 000 Hz (row 8, column 3). Starting with column 7 and counting left through column 3 gives a count of 5 (7, 6, 5, 4, 3). The number 5 would then be set into S6 of the RT card. Proceed to step 13.

11. Note the frequency of the oscillator installed on the RT card, and divide this frequency by the desired $_{Ro.}$ The result of this computation must be of the form 2^n (n = 0, 1, 2, 4 ....); otherwise, the desired Ro cannot be obtained with the oscillator.

12. Locate the computed OSC FREQ/Ro (oscillator frequency divided by (R_o) value in table 3-5, and set S6 on the RT card to the position indicated in the table. For example, if the RT card oscillator frequency is 4, 800, 000 Hz, and the desired R_o is 600, 000 bps, then OSC FREQ/Ro = 8. As shown in table 3-5, the proper setting for S6 is position 4.

13. This completes the setup procedure for RT cards operating from an internal timing source (S5 set to INT). Install the RT card in slot 16 of the MULTIPLEXER row.

14. Set S4 to the 75 or 6K position as indicated in the INPUT INTFC 75 or 6K block on sheet 2 of the configuration worksheets.

15. Determine the frequency of the external timing source being supplied to the multiplexer from the EXT FREQ HZ block on the worksheet, and divide this frequency by the output rate (Ro) entered in the OUTPUT RATE $_{(R_{o)}}$ BPS block of the TIMING section. The result of this computation must be of the ^{2n} form (n = 0, 1, 2, 4 ...); otherwise, the input frequency being supplied will not yield the desired $R_{o.}$

16. Locate the value computed in step 15 in the OSC FREQ/Ro column of table 3-5, and set S6 on the RT card to the corresponding position indicated in the table. This completes the setup of an RT card operating from an external reference timing source (S5 set to EXT).

Table 3-5. Reference Timer Setup Data

OSC FREQ/R_o	S6 Setting
1	1
2	2
4	3
8	4
16	5
32	6
64	7
128	8
256	9
512	10
1024	11
2048	12
4096	13
8192	14
16384	15
32768	16

17. Install the RT card in slot 16 of the MULTIPLEXER row.

3-75. OEG CARD (P/N 61864020). The OEG card is located in slot 19 of the MULTIPLEXER row. To set up this card, set each of the 15 jumpers of S1 to the ON position (figure 3-15).

NOTE

Each position of S1 corresponds to a similarly numbered multiplexer channel. Setting any of the S1 jumpers to the OFF position inhibits display of the channel card's diagnostic error status when the multiplexer set is in the self-test mode of operation. This configuration also prevents the display of errors detected on the card during normal operation. A jumper on S1 should be set to the OFF position only in those unusual cases when the affected channel is active but does not have a channel card installed.

3-76.SEQ CARD (P/N 61864040).The seq card is located in slot 21 of the MULTIPLEXER row. Set up the card as follows (refer to figure 3-16 for all switch locations):

1. Refer to the PORT STRAPPING section on sheet 2 of the configuration worksheets. Set each jumper of 31- position S1 to A (active) or S (strapped) as indicated.

NOTE

Depending upon the multiplexer configuration being implemented, the total number of ports designated as either A or S on the worksheet may vary between 15 and 31. The positions of S1 jumpers for ports not designated as A or S on the worksheet are not important and can be either A or S.

2. Refer to the worksheet, and count the total number of ports indicated as either A or S and ensure that this quantity is the same as the quantity entered in the PORTS IN USE (N) block of the worksheet.

NOTE

If the total number of ports indicated as either A or S does not exactly match the number entered in the PORTS IN USE (N) block, the information in the worksheet is incorrect.

3. Refer to table 3-6 and locate the number entered in the PORTS IN USE (N) block of the worksheet. Set the corresponding 5-digit binary number listed in the table into switch S2 of the seq card. This completes the setup of the seq card.

NOTE

Ensure that the MSB and LSB positions of the 5- digit binary number are not inadvertently reversed; i.e., the LSB digit of table 3-6 must be set into S2 position A, and the MSB digit of table 3-6 must be set into S2 position E.

4. Install the seq card in slot 21 of the MULTIPLEXER row.

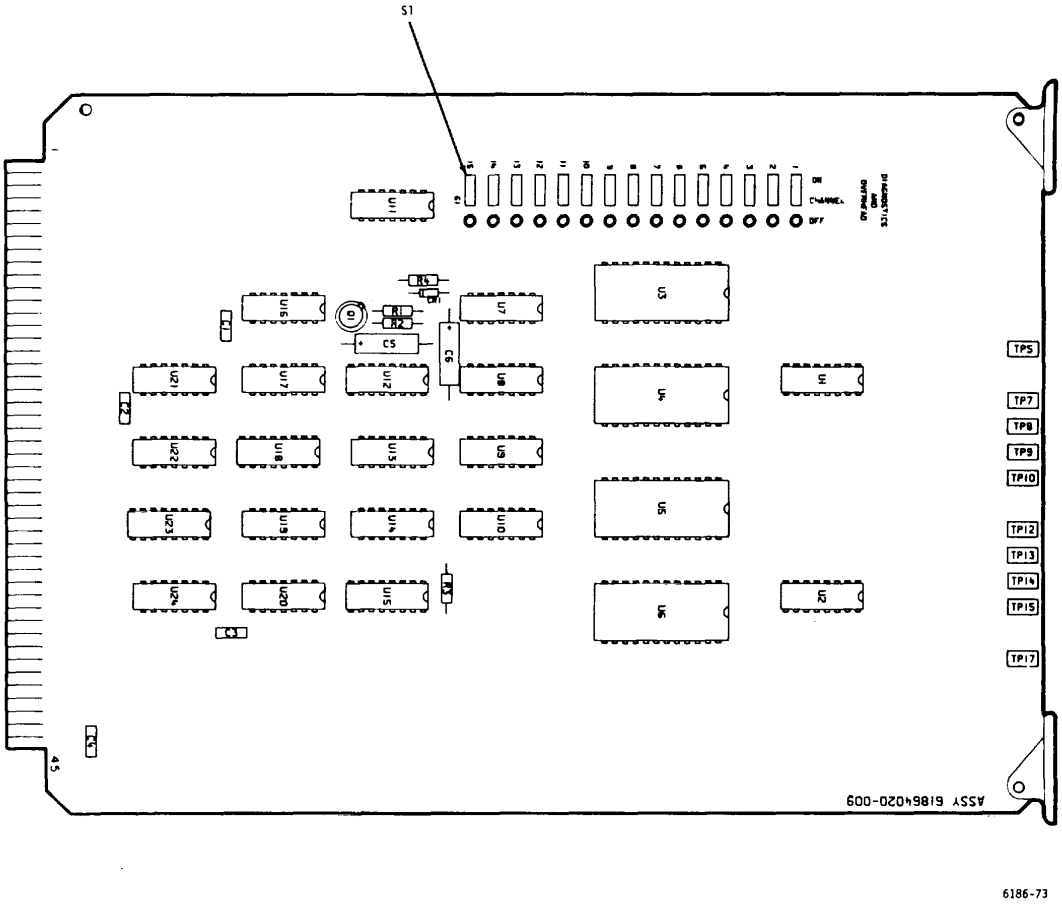


Figure 3-15. OEG Card - Switch Location Diagram

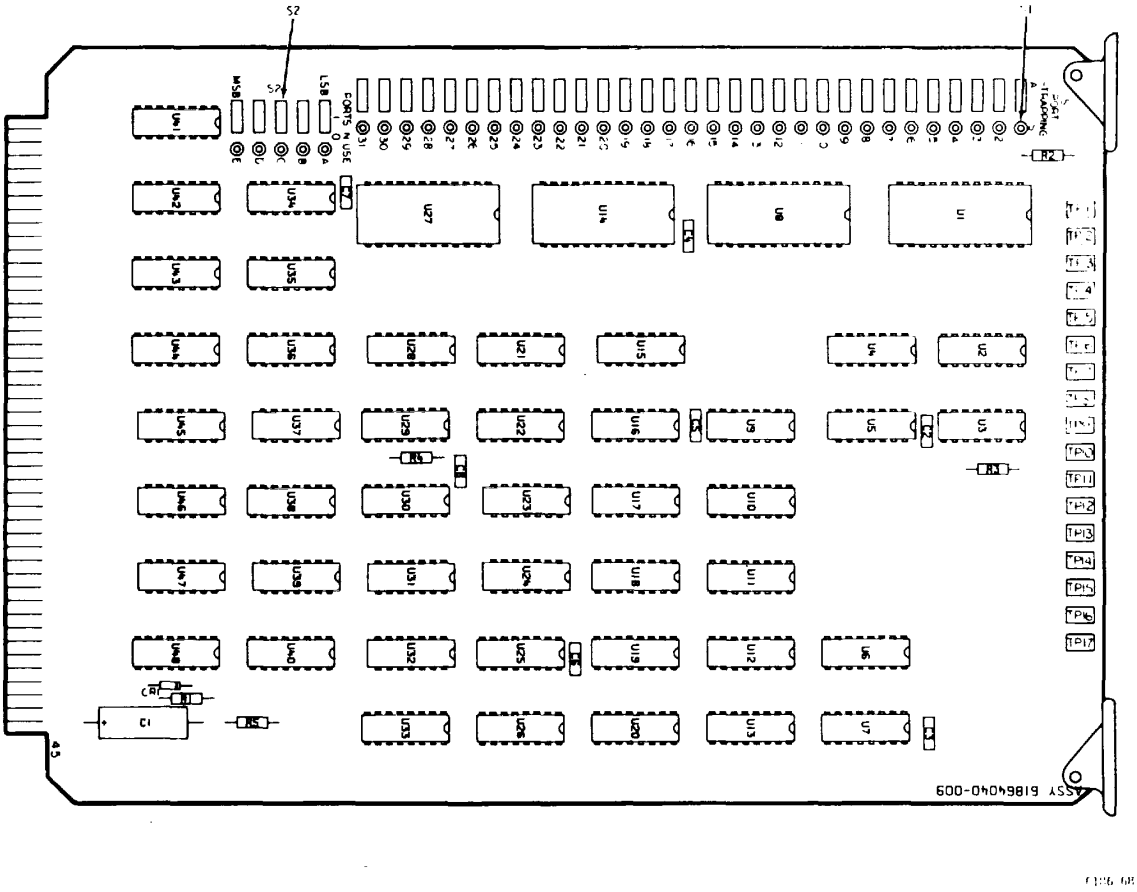


Figure 3-16. Seq Card - Switch Location Diagram

Table 3-6. Seq Card Ports-in-Use Switch Settings

Ports in Use (N)	S2 Settings				
	LSB				MSB
	A	B	C	D	E
15	1	1	1	1	0
16	0	0	0	0	1
17	1	0	0	0	1
18	0	1	0	0	1
19	1	1	0	0	1
20	0	0	1	0	1
21	1	0	1	0	1
22	0	1	1	0	1
23	1	1	1	0	1
24	0	0	0	1	1
25	1	0	0	1	1
26	0	1	0	1	1
27	1	1	0	1	1
28	0	0	1	1	1
29	1	0	1	1	1
30	0	1	1	1	1
31	1	1	1	1	1

3-77. GC/DM CARD (P/N 61864030). Ensure that a GC/DM card is installed in slot 20 of the MULTIPLEXER row. No setup procedures are required for this card.

3-78. DEMULTIPLEXER CHANNEL ELECTRONICS SETUP PROCEDURES.

3-79. Paragraphs 3-80 through 3-83 prescribe the setup procedures for the demultiplexer channel cards. The information required for the setup process is contained on sheet 3 of the configuration worksheets (figure 3-11).

3-80.SB CARD (P/N 61864090).For each channel that uses an SB card, set up the card as follows (refer to figure 3-17 for all switch locations):

NOTE

SB cards are used for each channel marked with an X in the CARD TYPE SB block of the worksheet. If the CARD TYPE SB block is marked with the letters NB, a narrow band smoothing buffer (NBSB) card (P/N 61864160) is used. Procedures for the NBSB card setup are presented in paragraph 3-81.

1. Note the demultiplexer input rate (Ro) value entered on the worksheet. If Ro is less than 2000 bps, set S1 to the Ro < 2KHZ position. If Ro is 2000 bps or greater, set S1 to the Ro ≥ 2KHZ position.

2. Set S9 to the NORM position.

3. Set S4 to the ON position.

NOTE

Setting S4 to the OFF position will inhibit the display of any card errors detected by the SB card diagnostic circuits.

4. Refer to the DATA Ø N or R block of the worksheet, and set both jumpers of S10 to the indicated N (normal) or R (reversed) position.

5. Refer to the TIMING Ø N or R block of the worksheet, and set both jumpers of S11 to the indicated N (normal) or R (reversed) position.

6. Refer to the INTERFACE BAL, U75, or U6K block of the worksheet, and set S19 and S22 to the indicated B (balanced), U75 (unbalanced 75 ohms), or U6K (unbalanced 6K ohms) position.

7. If the INTERFACE BAL block of the worksheet is marked, set S14 through S18, S20, S21, and S23 to the B position. If the INTERFACE U75 or U6K block is marked, set the switches to the U position.

8. Refer to the worksheet, and note the channel's output data rate value entered in the OUTPUT RATE (BPS) (R_c) block.

9. Set S5 on the SB card to one of the four corresponding positions on the board for the family of rate ranges in which the listed channel data rate falls. As an example, if the desired channel data rate is 48000 (48K), S5 would be set to the B position as indicated by the switch position markings for switch S5. As shown on the SB card, the B rate range is for rates from 47 kbps through 94 kbps, and thus

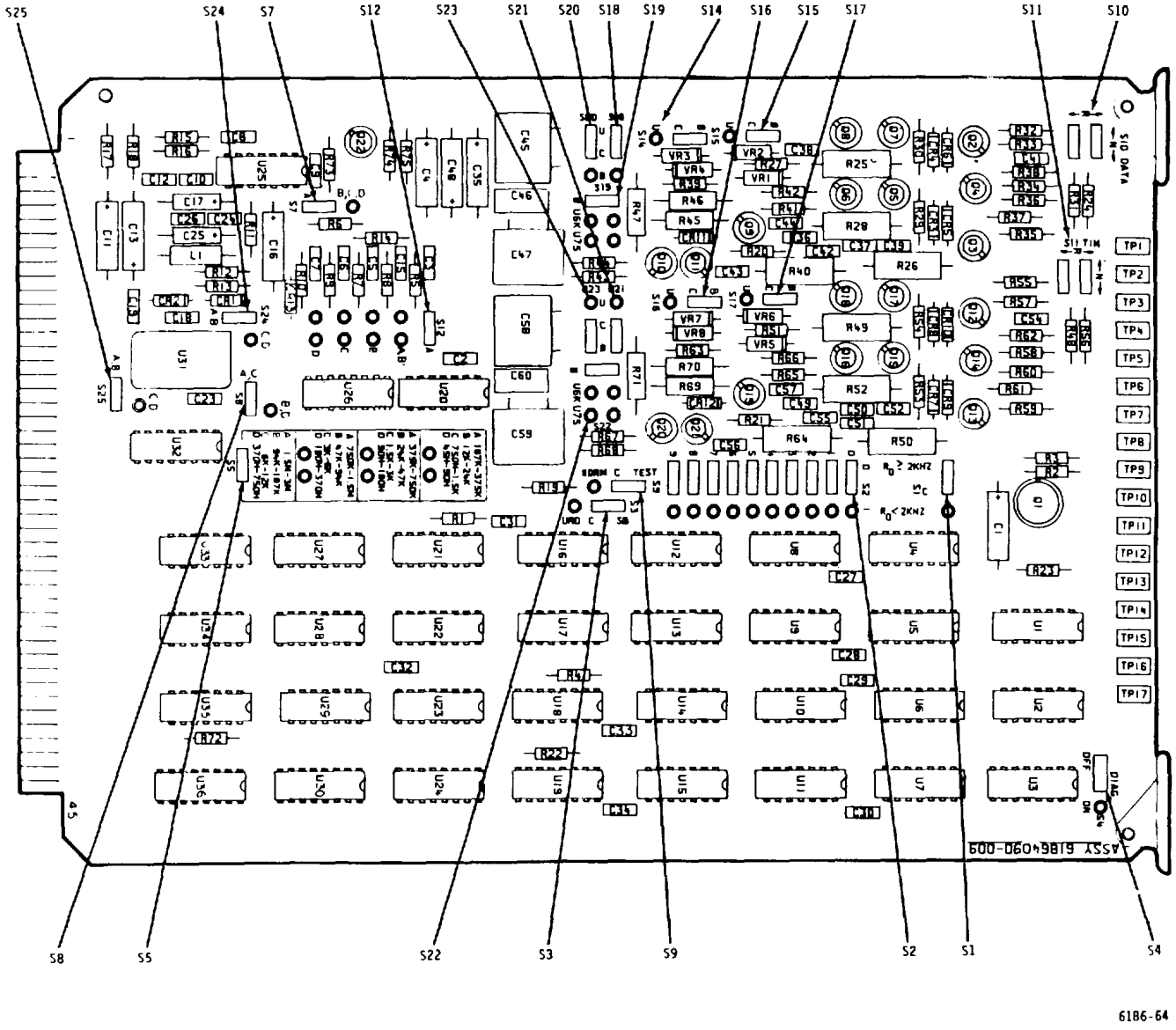


Figure 3-17. SB Card - Switch Location Diagram

includes the 48-kbps channel rate desired.

10. Note the rate range (A, B, C, or D) selected in step 9 and set S7 to the corresponding position. For example, if range B was selected, S7 would be set to the B, C, D position. If range A was selected, 57 would be set to the A position.

11. Set S8 to the rate range selected in step 9.

12. Set S24 to the rate range selected in step 9.

13. Set S25 to the rate range selected in step 9.

NOTE

Certain positions of S12 indicate rate ranges A' (A prime) and B' (B prime). When S5 is set to the A range and the channel rate (R_c) listed on the worksheet is 1.5 Mbs or greater, S12 must be set to the A' position. For channel rates in the A range which are below 1.5 Mbs, and for any channel rate in the B range, the A' and B' positions of S12 are used in cases where the multiplexer's channel output smoothing interval is unacceptable to user sink instruments. In such cases, special instructions will be added to the configuration worksheets. Discussion pertaining to selection and use of S12 A' and B' ranges is contained in paragraph 3-58.

14. Set S12 to the rate range selected in step 9 or as instructed in the above note.

15. Refer to sheet 3 of the worksheets, and note in the PORTS K blocks the number of ports (K) assigned to each channel. Note the port rate (Rp) shown on sheet 4 of the worksheets. Multiply K and Rp, and compare this value (KRp) with the channel's output data rate (R_c).

16. If R_c is equal to KRp (R_c = KRp), set S3 to the SB position, which completes the SB card setup process. Install the SB card in its appropriate slot (1 through 15) in the DEMULTIPLEXER row. If R_c is less than KRp (R_c < KRp), set S3 to the URD position and perform steps 17 through 19.

NOTE

In cases where R_c < KRp, coarse rate conversion of KRp to R_c must be performed by the demultiplexer. To enable this conversion, a fill bit value must be computed and set into the SB by 10-position switch S2.

17. Determine the quantity of fill bits required, using the expression:

$$\text{Fill bits} = 899K\left(1 - \frac{R_c}{KR_p}\right)$$

where
K = quantity of ports assigned to the channel (from worksheet)

R_c = channel data rate (from worksheet)

R_p = port rate (from worksheet).

NOTE

To ensure a proper computation of fill bit quantity, the value of 1 - Rc/KRp must be determined to seven decimal places. Overall fill bit quantity, when computed, must be rounded to the nearest whole number; i.e., 316.7 is rounded to 317, etc. The largest number of

fill bits the demultiplexer can process is 868. If the computed quantity of fill bits exceeds this value, a check for computational errors is suggested. A correctly computed fill bit value greater than 868 is indicative of incorrect configuration data on the worksheet.

18. Refer to table 3-3, and locate the fill bit quantity computed in step 17. Enter the 10-digit binary number associated with this quantity in the RATE CONVERSION DATA block on sheet 3. of the worksheets.

NOTE

In step 19, ensure that the 10-digit number is inserted properly and the 0 and 9 positions are not inadvertently reversed. Removal of all switch jumpers prior to starting the number entry process is suggested.

19. Set 10-digit switch S2 on the SB card to reflect the 10-digit binary number recorded on the worksheet. This completes the SB card setup process.

20. Install the SB card in its appropriate slot (1 through 15) in the DEMULTIPLEXER row.

3-81. NBSB CARD (P/N 61864160). For each channel that uses an NBSB card, set up the card as follows (refer to figure 3-18 for all switch locations):

NOTE

NBSB cards are used for each channel marked with the letters NB in the CARD TYPE SB block of sheet 3 of the worksheets. If the CARD TYPE SB block is marked with an X, a smoothing buffer (SB) card (P/N 61864090) is used. Procedures for SB card setup are presented in paragraph 3-80.

1. Note the demultiplexer input rate (R_o) value entered on the worksheet. If R_o is less than 2000 bps, set S1 to the $_{RO}$ < 2KHZ position. If Ro is 2000 bps or greater, set S1 to the $R_O \geq$ 2KHZ position.

2. Set S9 to the NORM position.

3. Set S4 to the ON position.

NOTE

Setting S4 to the OFF position will inhibit the display of any card errors detected by the NBSB card diagnostic circuits.

4. Refer to the DATA Ø N or R block on the worksheet, and set both jumpers of S10 to the indicated N (normal) or R (reversed) position.

5. Refer to the TIMING Ø N or R block of the worksheet and set both jumpers of S11 to the indicated N (normal) or R (reversed) position,

6. Refer to the INTERFACE BAL, U75, or U6K block of the worksheet, and set S19 and S22 to the indicated B (balanced) U75 (unbalanced 75 ohms) or U6K (unbalanced 6K ohms) position.

7. If the INTERFACE BAL block of the worksheet is marked, set S14, S15, S16, S17, 518, S20, S21, and S23 to the B position. If the INTERFACE U75 or U6K block is marked, set the switches to the U position.

8. Refer to the worksheet, and note the channel's output (data rate

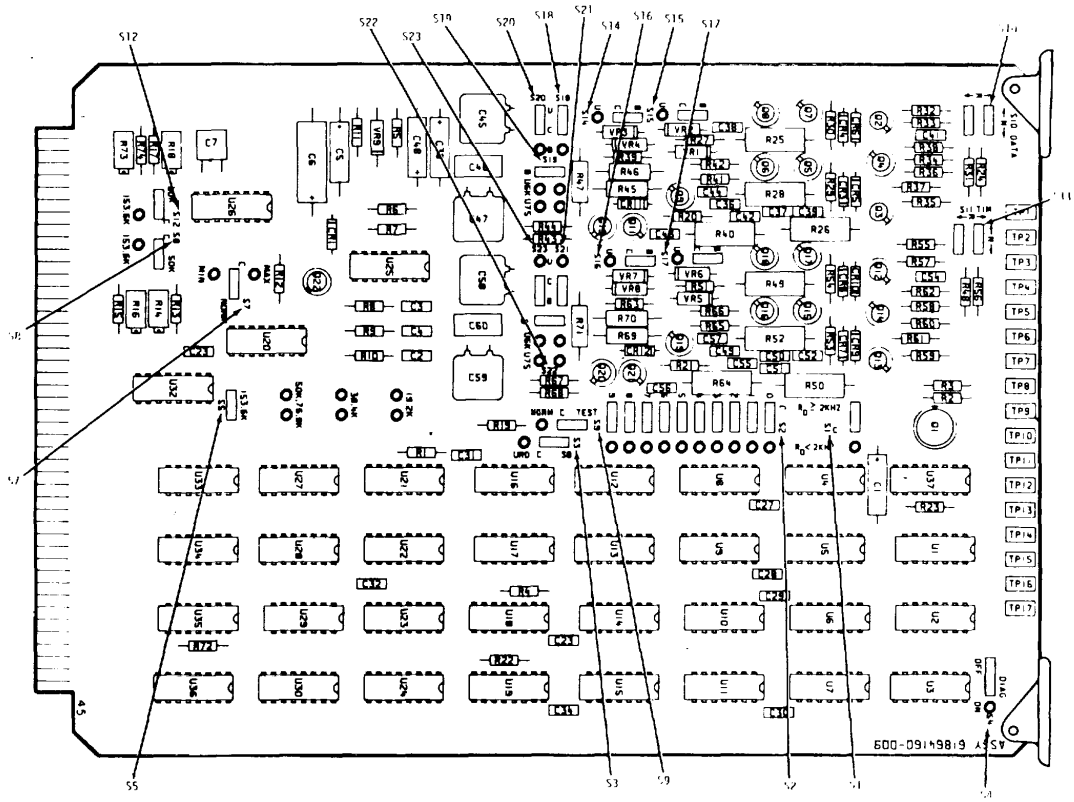


Figure 3-18. NBSB Card - Switch Location Diagram

value entered in the OUTPUT RATE (BPS) R_c block.

9. Set S5 to the rate value shown.

10. If S5 was set to the 50K (50000 bps) position, set S8 and S12 to the 50K position. If S5 was set to a position other than 50K, set S8 and S12 to the 153.6K position.

11. Set S7 to the NORM (normal) position.

12. Refer to sheet 3 of the worksheets, and note in the PORTS K blocks the number of ports (K) assigned to each channel. Note the port rate (Rp) shown on sheet 4 of the worksheets. Multiply K and Rp, and compare this value (KRp) with the channel's output data rate (Rc).

13. If R_c is equal to KRp (R_c = KRp), set S3 to the SB position, which completes the NBSB card setup process. Install the NBSB card in its appropriate card slot (1 through 15) in

the DEMULTIPLEXER row. If R_c is less than KRp (R_C < KRp), set S3 to the URD position and perform steps 14 through 16.

NOTE

In cases where R_c < KRp, coarse rate conversion of KRp to R_c must be performed by the demultiplexer. To enable this conversion, a fill bit value must be computed and set into the NBSB by 10-position switch S2.

14. Determine the quantity of fill bits required, using the expression:

$$\text{Fill bits} = 899K \left(1 - \frac{Rc}{KR_p}\right)$$

where

K = quantity of ports assigned to the channel (from worksheet)

R_c = channel data rate (from worksheet)

R_p = port rate (from worksheet)

NOTE

To ensure a proper computation of fill bit quantity, the value of 1 - Rc/KRp must be determined to seven decimal places. Overall fill bit quantity, when computed, should be rounded to the nearest whole number; i.e., 316.7 is rounded to 317, etc. The largest number of fill bits the demultiplexer can process is 868. If the computed quantity of fill bits exceeds this value, a check for computational errors is suggested. A correctly computed fill bit value greater than 868 is indicative of incorrect configuration data on the worksheet.

15. Refer to table 3-3 and locate the fill bit quantity computed in step 14. Enter the 10-digit binary number associated with this quantity in the RATE CONVERSION DATA block on sheet 3 of the worksheets.

NOTE

In step 16, ensure that the 10-digit number is inserted properly and the 0 and 9 positions are not inadvertently reversed. Removal of all switch jumpers prior to starting the number entry process is suggested.

16. Set 10-digit S2 on the NBSB card to reflect the 10-digit binary number entered on the worksheet. This completes the NBSB card setup process.

17. Install the NBSB card in its appropriate slot (1 through 15) in the DEMULTIPLEXER row.

3-82. VD CARD (P/N 61864140). No setup of the VD card is required. Install a VD card in the appropriate slot in the DEMULTIPLEXER row indicated on the worksheet.

3-83. TD CARD (P/N 61864130). Set up the TD card as follows (refer to figure 3-19 for all switch locations):

1. Set S1 to the ON position.

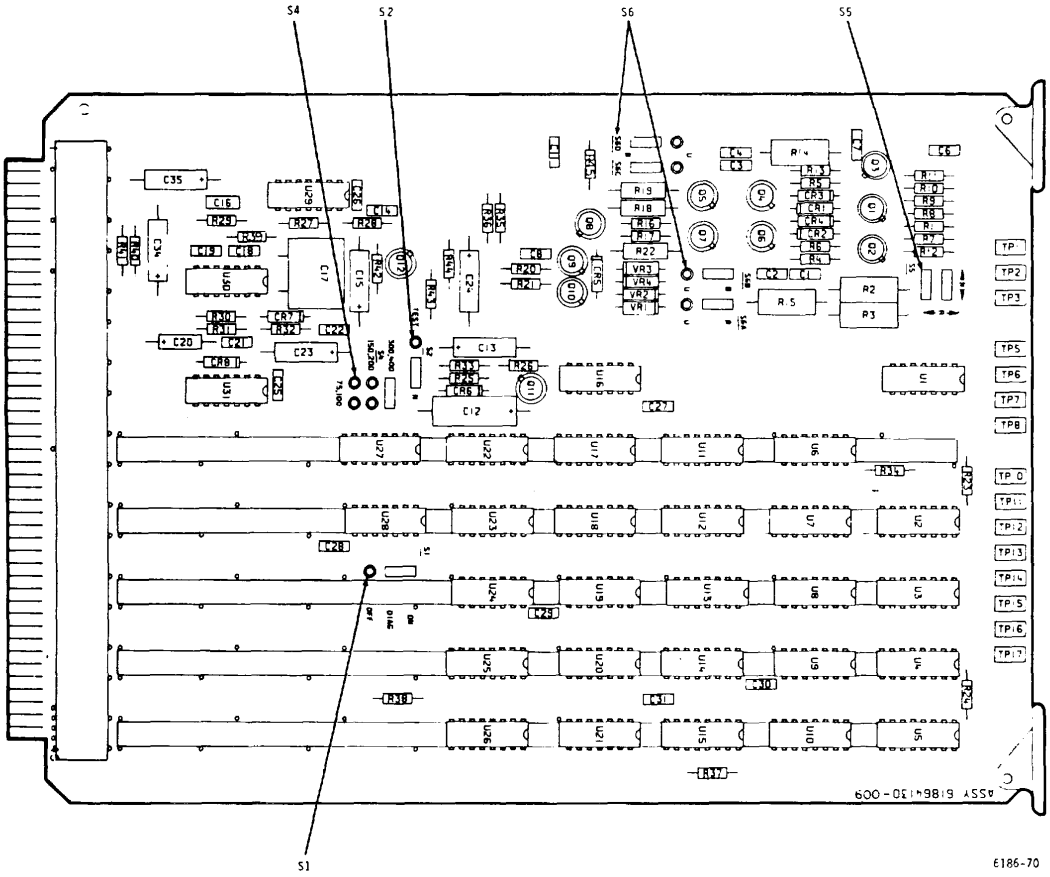


Figure 3-19. TD Card - Switch Location Diagram

NOTE

Setting S1 to the OFF position inhibits the display of errors detected by the TD diagnostic circuits.

2. Set S2 to the N (normal) position.

3. Refer to the DATA 0 N or R block on the worksheet, and set S5 to the indicated N (normal) or R (reversed) position.

4. Refer to the INTERFACE BAL, U75, or U6K block on the worksheet. If the INTERFACE BAL block is marked, set S6A, S6B, S6C, and S6D to the B position. If the INTERFACE U75 or U6K is marked, set the switches to the U position.

5. Multiply the number of ports (K) assigned to the channel on sheet

3 and the port rate (Rp) listed on sheet 4 of the worksheet. Divide the product (KRp) by 3, and set S4 on the TD card to the range that includes the computed KRp/3 value. This completes the TD card setup process.

NOTE

The computed KRp/3 value must exactly match one of the six ranges listed on switch S4. If a match is not obtained, a check of the computation is suggested. A correct computation not yielding a match with one of the S4 ranges indicates incorrect configuration data on the worksheet.

6. Install the TD card in its appropriate slot (1 through 15) in the DEMULTIPLEXER row.

3-84. DEMULTIPLEXER COMMON ELECTRONICS SETUP PROCEDURES.

3-85. The information required for configuring the cards comprising the common electronics section of the demultiplexer is contained on sheet 4 of the configuration worksheets (figure 3-11). Based on this information, paragraphs 3-86 through 3-90 prescribe the procedures to be used in the setup process.

3-86. OEG CARD (P/N 61864020). The demultiplexer and multiplexer OEG cards are identical, and are located in slot 19 of the MULTIPLEXER and DEMULTIPLEXER rows. Procedures for setting up the demultiplexer OEG card are the same as those prescribed in paragraph 3-75 for the multiplexer OEG card.

3-87. SEQ CARD (P/N 61864040), The demultiplexer seq card in slot 21 of the DEMULTIPLEXER row is identical to that used in the multiplexer. Procedures to set up this card are identical to those prescribed in paragraph 3-76, with the following exceptions: (1) worksheet information pertinent to the demultiplexer seq card is contained on sheet 4 of the configuration worksheets; and (2) the demultiplexer seq card is installed in slot 21 of the DEMULTIPLEXER row.

3-88. GC/DM CARD (P/N 61864030). The demultiplexer GC/DM card is identical to that used in the multiplexer. Ensure that a GC/DM card is installed in slot 20 of the DEMULTIPLEXER row. No setup procedures are required for this card.

3-89. FS CARD (P/N 61864110). The FS card is located in slot 16 of the DEMULTIPLEXER row. Set up the FS card as follows (refer to figure 3-20 for all switch locations):

1. Refer to sheet 4 of the configuration worksheets and note the DATA Ø N or R block. Set S1 to the indicated N (normal) or R (reversed) position.

2. Refer to the TIMING Ø N or R block on the worksheet, and set S2 to the indicated N (normal) or R (reversed) position.

3. Set S3A and S3B to the NORM position.

4. Refer to the INTFC 75 or 6K block on the worksheet, and set S4 and S5 to the indicated 75 or 6K position. install the FS card in slot 16 of the DEMULTIPLEXER row.

3-90. ERD CARD (P/N 61864120). The ERD card is located in slot 17 of the DEMULTIPLEXER row, To set up the ERD card, refer to the ERROR RATE THRESHOLD block on sheet 4 of the configuration worksheets, and set S1 (figure 3-21) to the indicated position. Install the ERD card in slot 17 of the DEMULTIPLEXER row.

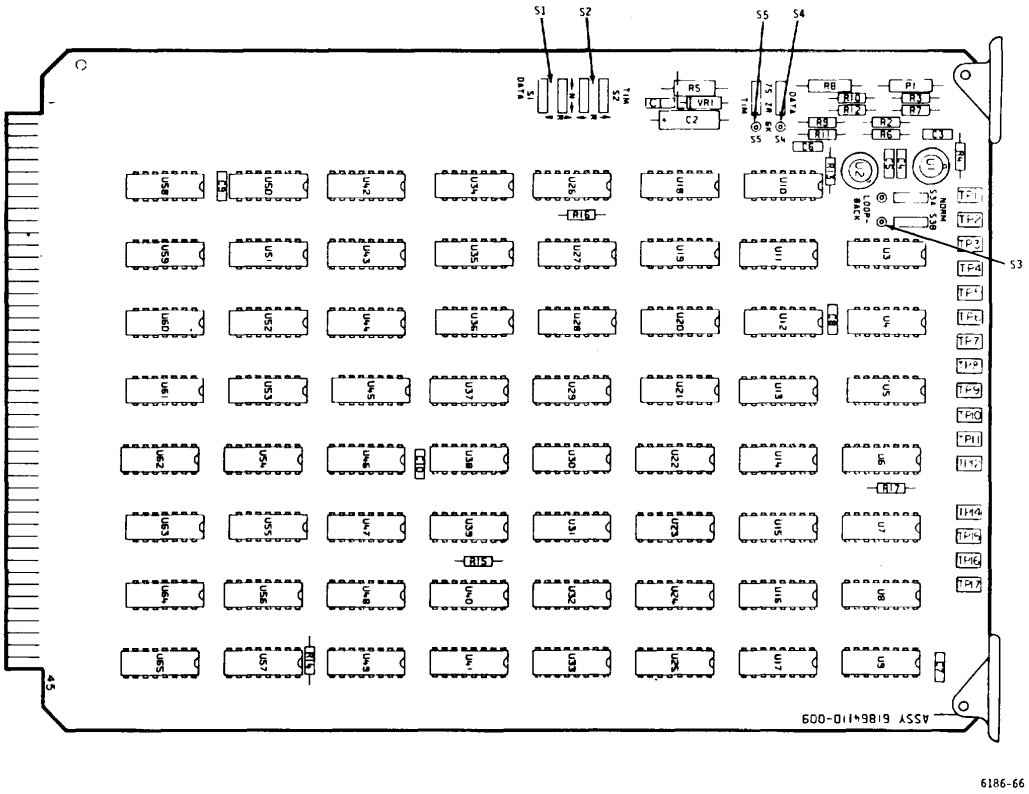


Figure 3-20. FS Card - Switch Location Diagram

3-91. DISPLAY CARD (P/N 61864050) SETUP PROCEDURES.

3-92. The display card is located in slot 22 of the MULTIPLEXER row. Set up the display card as follows:

1. If both the multiplexer and demultiplexer portions of the multiplexer set are being used, i.e., overall configuration is duplex (paragraph 3-7), set S1 (figure 3-22) to the NORM position.

2. If either the multiplexer or the demultiplexer portion of the multiplexer set is not being used, set S1 to the MUX OFF or DEMUX OFF position as applicable. This will inhibit diagnostic error indications from the portions of the multiplexer set not being used. Install the display card in slot 22 of the DEMULTIPLEXER row.

3-93. THERMAL ALARM OPTIONS.

3-94.The multiplexer set has alarm circuits that activate when the operating temperature within the set exceeds specified limits. Upon activation, the alarm circuits are set up to perform one of the two following optional functions: (1) light the front panel TEMPERATURE indicator, cause a remote alarm indication to appear at connector

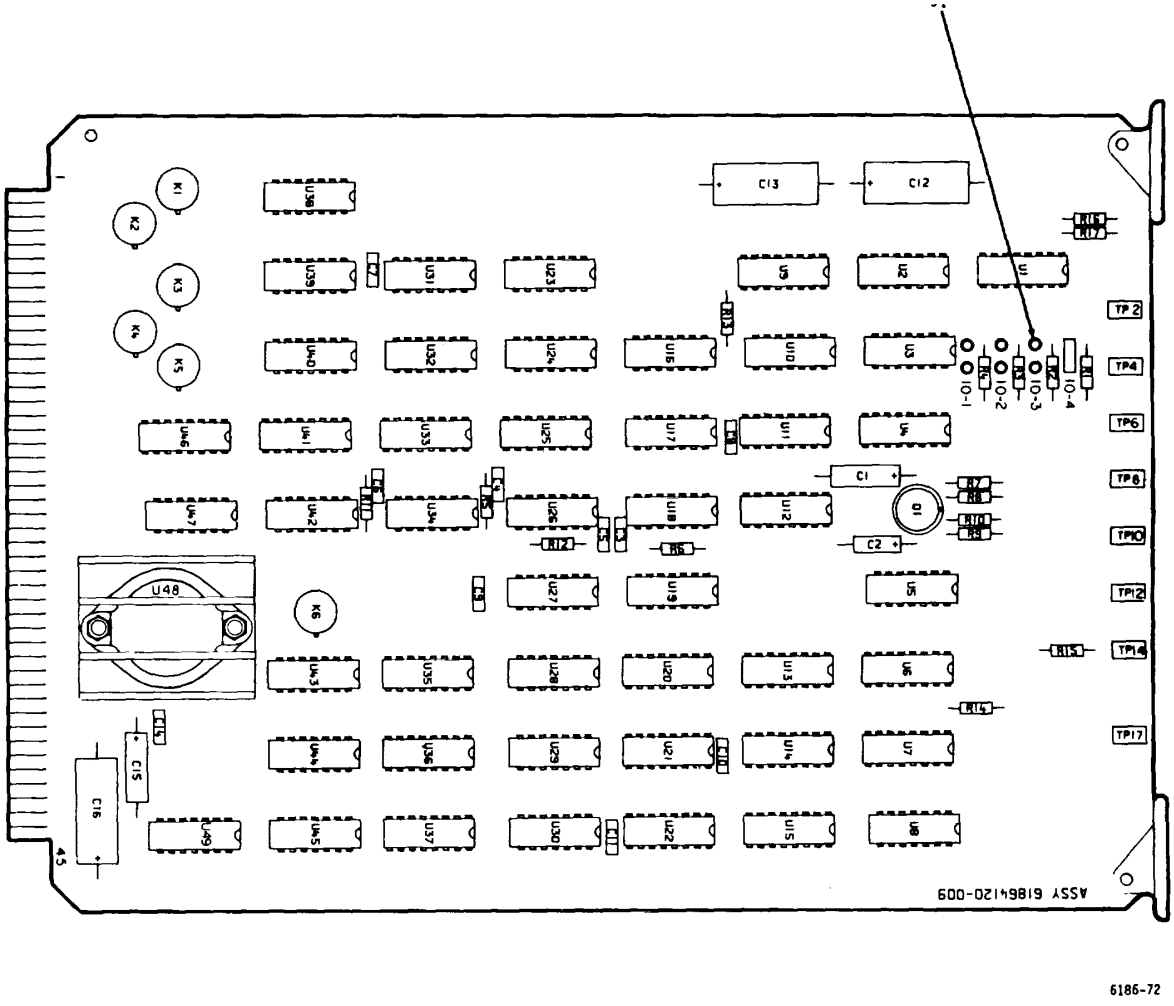


Figure 3-21.ERD Card - Switch Location Diagram

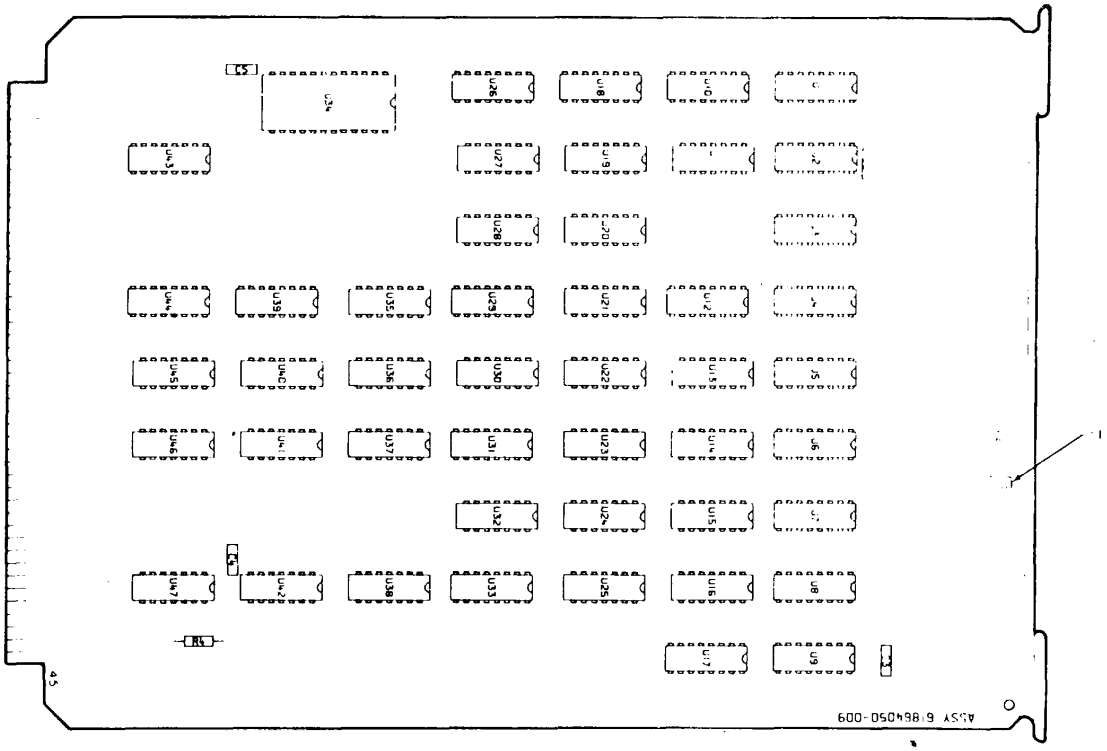


Figure 3-22. Display Card - Switch Location Diagram

J66, and cause the multiplexer set power supply to automatically shut down; and (2) light the front panel TEMPERATURE indicator and cause a remote alarm indication to appear at connector J66.

3-95. In option 1, the multiplexer set ceases to process input/output data until the cause of the overtemperature situation is corrected. The multiplexer set is initially manufactured with option 1 installed.

WARNING

Dangerous voltages are present within the front panel. Turn multiplexer power off and disconnect power cord from power source before removing front panel assembly.

3-96. If option 2 is desired, remove power, remove the front panel assembly (paragraph 6-23), and carefully remove the bare wire jumper soldered between terminals E24 and E25 of front panel board A2A1 (P/N 61861028) (refer to figure 3-23 for terminal locations). Option 1 can be reinstalled by soldering a jumper between terminals E24 and E25.

3-96.1. REMOTE ALARM OPTIONS

3.96.2. There are seven remote alarm signals routed to the REMOTE ALARM connector on the rear panel. The remote alarm signals that are applied to the REMOTE ALARM connector are initiated by the multiplexer set diagnostic circuits. The diagnostic circuits automatically monitor the equipment for faulty system data inputs and multiplexer set equipment malfunctions. Each of the remote alarm signals is associated with a pair of outputs (C1 and C2) that are held in an open-circuit condition in a no-error condition. When a fault is detected, the associated pair of outputs is closed in the multiplexer set to produce a closed-loop output condition. The seven remote alarm signals and their associated output pin locations on the REMOTE ALARM connector are listed below. Connector kit assembly 61867000-009 or 6187000-019 contains the mating connector for the REMOTE ALARM connector.

Signal	Pin No.	Function
LOFAC1	J66A	System indicator - Pro
LOFAC2	J66B	duces fault indication during time that demultiplexer circuits are not synchronized with incoming data.
LOFBC1	J66-C	System indicator - Pro
LOFBC2	J66-D	duces a continuing fault indication once demultiplexer circuits are not synchronized with incoming data. Fault indication remains until DISPLAY RESET switch is pressed on multiplexer set.
LERRC1	J66-G	System indicator - Pro
LERRC2	J66-H	duces fault indication during time that bit error rate in a demultiplexer exceeds a preselected threshold.
OOTC1	J66-N	System indicator - Pro-
OOTC2	J66-P	duces fault indication when an out-of tolerance condition exists between the incoming data and one multiplexer input circuit.
FAILC1	J66-E	Multiplexer set indica-
FAILC2	J66-F	tor - Produces fault indication when a card malfunction in multiplexer set is detected.
PSFC1	J66-L	Multiplexer set indica-
PSFC2	J66-M	tor Produces fault indication when power supply malfunction in multiplexer set is detected.
TEMPC1	J66-J	Multiplexer set indica-
TEMPC2	366-K	tor Produces fault indication when internal operating temperature in multiplexer set exceeds 205°F (96°C).

3-97. MULTIPLEXER SET OPERATIONAL TESTS.

3-98. When a multiplexer set is reconfigured for a different system application, the performance standards prescribed in paragraph 6-38 will be performed. These procedures will also be performed when a multiplexer set is initially installed in a system to ensure that the equipment is operationally ready to perform its assigned tasks.

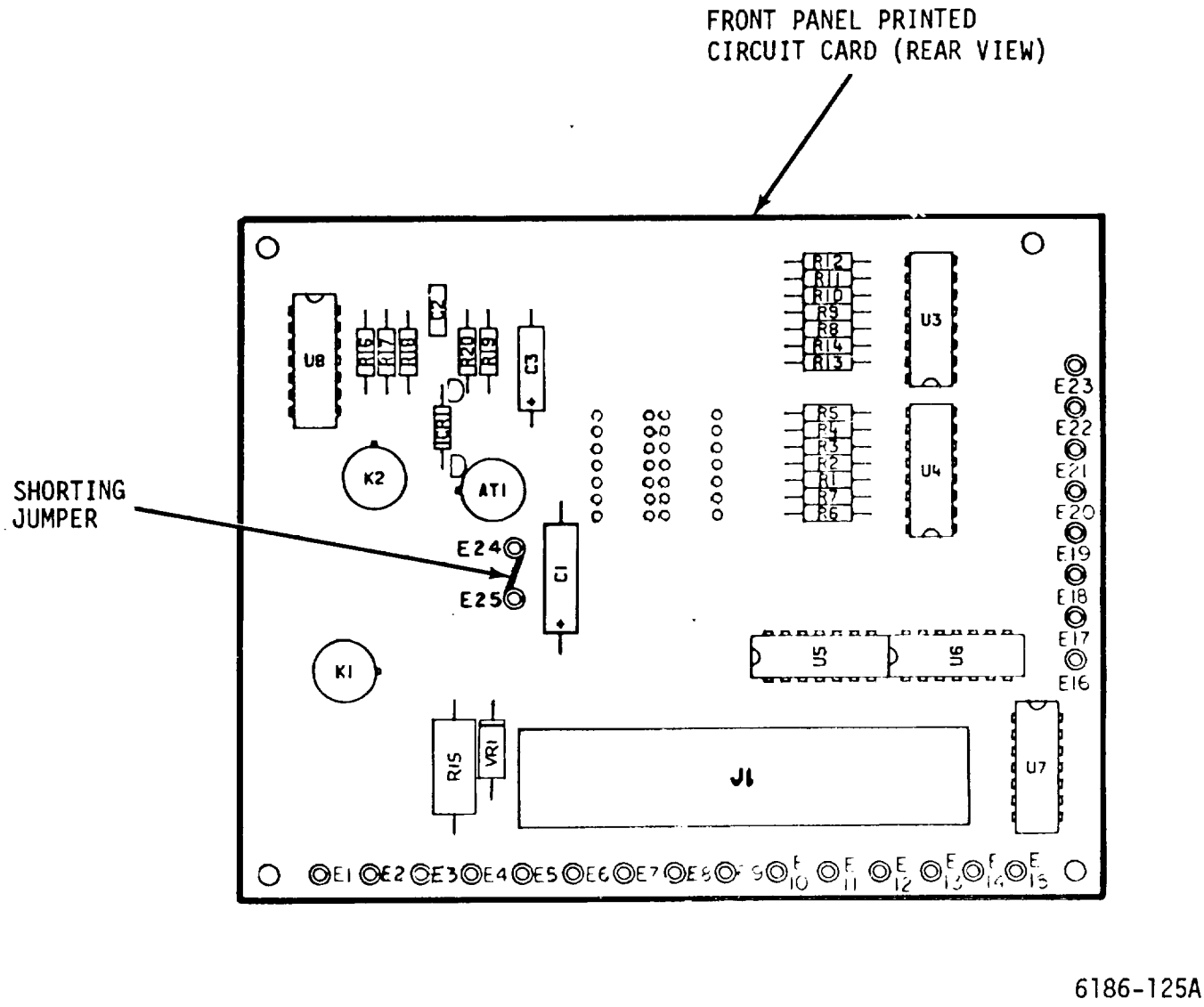


Figure 3-23. Front Panel Printed Circuit Card - Jumper Location Diagram

SECTION IV

PREPARATION FOR RESHIPMENT

3-99. GENERAL.

3-100. This section contains instructions for preparing the multiplexer set for shipment. The original shipping container, padding, and filler should be used for packing the multiplexer set for shipment.

3-101. PACKING PROCEDURES,

WARNING

The multiplexer set weighs 140 pounds. Use a mechanical lifting device whenever possible. To prevent injury to personnel, it is recommended that a minimum of four men be used when a multiplexer set is to be lifted manually.

1. Set POWER CONTROL switch to OFF.

NOTE

Perform the procedures in steps 2 through 10 when the multiplexer set is rack mounted and uses the extendable slides for support. Proceed to step 11 when the multiplexer set is secured to a rack only by its two rack-mounting flanges. When the multiplexer set is installed on a flat surface such as a bench or table, perform only steps 4, 5, 9, and 10 below.

2. Remove and retain 12 screws and washers securing two rack-mounting flanges to electronic equipment rack.

3. Carefully extend multiplexer set upon its mounting slides until slides lock in extended position.

4. Disconnect power cable from primary power source and from multiplexer set.

5. Disconnect remote alarms cable from multiplexer set, and disconnect all input/output data and timing signal cables.

6. Release the extender slide locks and carefully remove multiplexer set from rack. Place multiplexer set on a suitable work bench or surface.

7. Remove two outer extender slide sections secured to electronic equipment rack. Retain all mounting hardware.

8. Install two outer extender slide sections removed in step 7 on two inner slide sections mounted on multiplexer set.

9. Verify that all captive screws on front panel and top panel of multiplexer set are securely fastened.

NOTE

When original shipping container is not available, prepare multiplexer set for shipment in accordance with currently applicable packaging instructions for electronic equipment.

10. Place multiplexer set and power cable in shipping container and prepare equipment for shipment.

11. Disconnect power cable from primary power source and from multiplexer et.

12. Disconnect remote alarms cable from multiplexer set and disconnect all input/output data and timing signal cables from multiplexer set.

13. Support multiplexer set as necessary and remove 12 screws and washers securing two rack-mounting flanges to electronic equipment rack. Retain mounting hardware.

14. Carefully move multiplexer set from rack and place multiplexer set on a suitable work bench or surface.

15. Install pair of slide assemblies removed from multiplexer set at time of initial installation. Use seven screws on each slide assembly.

16. Verify that all captive screws on front panel and top panel of multiplexer set are securely fastened.

17. Place multiplexer set and power cable in shipping container and prepare equipment for shipment.

CHAPTER 4

OPERATION

4-1 INTRODUCTION.

4-2. When the multiplexer set is configured as prescribed in section I of chapter 3, the functional operation of the multiplexer is fully automatic. The operator requirements for operating the equipment are limited to the application of operating power. Once the equipment is in operation, operator duties consist of visual checks of the automatic diagnostic error displays and the performance of periodic maintenance tests.

4-3. CONTROLS AND INDICATORS.

4-4. All controls and indicators are mounted on the front panel of the multiplexer set. The controls and indicators are shown in figure 4-1. The controls and indicators, together with their functional descriptions, are listed in table 4-1.

4-5. OPERATING INSTRUCTIONS.

4-6. Paragraphs 4-7 through 4-10 contain the operating procedures for the multiplexer set; no unusual or special operating procedures are required. The lamp test and self-test procedures in paragraphs 4-8 and 4-9 can be performed on an operational multiplexer set without disrupting the functional operation of the equipment.

4-7. STARTING PROCEDURES.

1. Ensure that POWER CONTROL circuit breaker is pressed to its on position.

2. Set POWER CONTROL switch to ON. Observe that POWER CONTROL ON indicator is lighted. Other indicators may also be lighted.

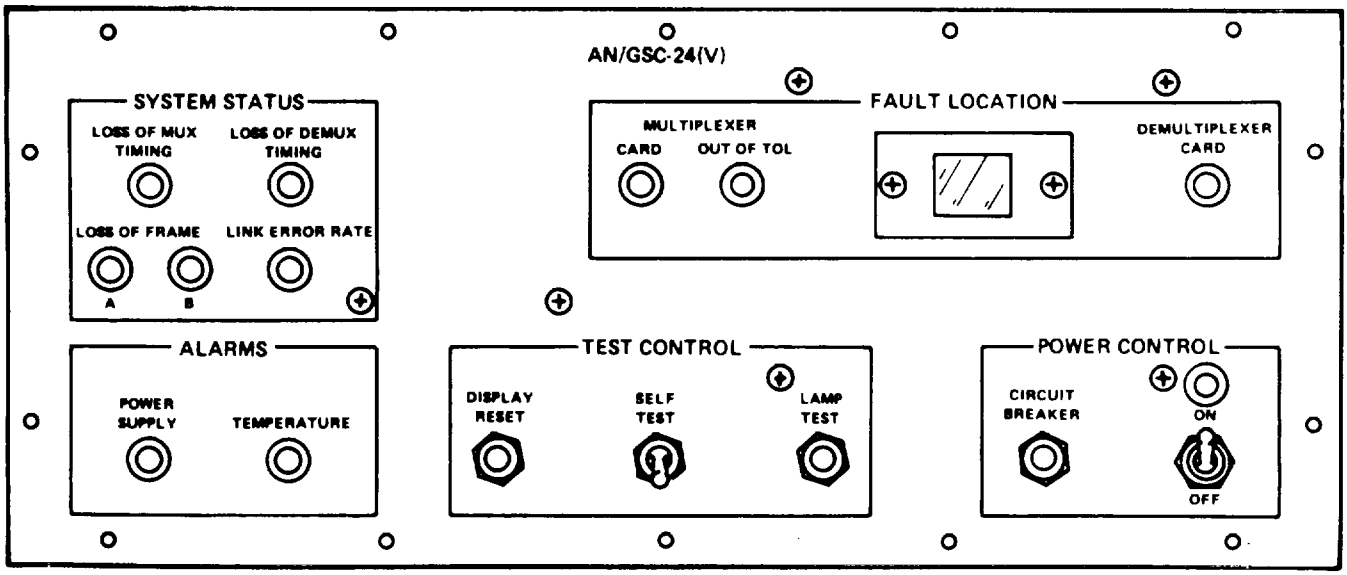


Figure 4-1. Front Panel Controls and Indicators

Table 4-1. Multiplexer Set Controls and Indicators

Controls/Indicators	Function
POWER CONTROL switch	Applies multiplexer set operating power.
POWER CONTROL ON indicator	Lights when operating power is applied.
POWER CONTROL circuit breaker overload occurs.	Provides equipment protection when electrical
SYSTEM STATUS group	
LOSS OF MUX TIMING indicator	Lights when source of multiplexer reference timing is removed. Remains lighted until reset.
LOSS OF DEMUX TIMING indicator	Lights when source of demultiplexer input timing is removed. Remains lighted until reset.
LOSS OF FRAME A indicator	Lights only when demultiplexer is not synchronized with transmitting multiplexer.
LOSS OF FRAME B indicator	Also lights when demultiplexer is not synchronized with transmitting multiplexer, but remains lighted until reset.
LINK ERROR RATE indicator	Lights when bit error rate applied to demultiplexer exceeds a predetermined threshold.
ALARMS group	
POWER SUPPLY indicator	Lights when a power supply malfunction is detected.
TEMPERATURE indicator	Lights when internal operating temperature exceeds 205°F (96°C).
TEST CONTROL group	
LAMP TEST switch	When pressed, causes a test of all indicators except POWER CONTROL ON indicator (paragraph 4-8).
SELF TEST switch	When set to on (up) position, initiates a test of built-in diagnostic circuits (paragraph 4-9).

Table 4-1. Multiplexer Set Controls and Indicators (Cont)

Controls/Indicators	Function
TEST CONTROL group (Cont)	
DISPLAY RESET switch	When pressed, extinguishes all lighted indicators except POWER CONTROL ON indicator.
FAULT LOCATION group	
MULTIPLEXER CARD indicator	Lights when a multiplexer card malfunction is detected. Remains lighted until reset.
MULTIPLEXER OUT OF TOL indicator	Lights when an out-of-tolerance condition is detected on one or more input channels.
DEMULTIPLEXER CARD indicator	Lights when a demultiplexer card malfunction is detected. Remains lighted until reset.
FAULT LOCATION numerical display	Functions are as follows: a) When MULTIPLEXER CARD or DEMULTIPLEXER CARD indicator is lighted, displays numerical location of malfunctioning card. b) When MULTIPLEXER OUT OF TOL indicator is lighted, displays number of channel that is out of tolerance. When two or more channels are out of tolerate at the same time, displays number of these channels sequentially. c) When SELF TEST switch is in on (up) position and no malfunction exists, displays 00. When SELF TEST switch is in on (up) position and a malfunction exists, displays numerical location of card whose diagnostic circuits are malfunctioning.

NOTE

The time required for the multiplexer set to stabilize when the POWER CONTROL switch is set to the ON position may take several minutes. Therefore, false error indications may occur when step 3 is performed before the multiplexer set has stabilized.

3 Press and release DISPLAY RESET switch. Observe that all indicators except POWER CONTROL ON indicator are out. When one or more indicators, other than POWER CONTROL ON indicator, are lighted, wait 60 seconds and repeat this step.

4-8. LAMP TEST PROCEDURES.

1. Press and hold LAMP TEST switch. Observe that all indicators are lighted. FAULT LOCATION numerical display is 88.

2. Release LAMP TEST switch. Observe that all indicators except POWER CONTROL ON indicator are out. FAULT LOCATION numerical display is out.

4-9. SELF-TEST PROCEDURES.

NOTE

For multiplexer output rates (R_o above 10 kbps, the time required for a final display of the self-test results is approximately 10 seconds. The time required for output rates less than 10 kbps is estimated by using the expression: time (in seconds) = 90,000/Ro The time required for a final display of the self-test results is approximately 10 minutes for an $_{Ro}$ o f155 bps.

1. Set SELF TEST switch to on (up) position.

2. Wait for completion of the self-test function within the multiplexer set and then observe that all indicators are lighted and FAULT LOCATION numerical display is 00.

3. Set SELF TEST switch to off (down) position. Observe that all indicators except POWER CONTROL ON indicator are out.

4-10. STOPPING PROCEDURES.

1. Set POWER CONTROL switch to OFF.

2. Observe that all indicators are out.

4-11. EMERGENCY STOPPING PROCEDURES.

1. Set POWER CONTROL switch to OFF.

2. Observe that all indicators are out.

CHAPTER 5

THEORY OF OPERATION

5-1. INTRODUCTION.

5-2. This chapter contains the principles of operation for the circuits in the multiplexer set. The chapter is divided into five sections. Section I contains discussions of the output data message format and basic equipment concepts used in the multiplexer set. The overall block diagram discussions for the multiplexer, demultiplexer, and diagnostic functions are in section II. Section III contains the block diagram discussions and detailed theory of operation for the printed circuit cards in the multiplexer function. The block diagram discussions and detailed theory of operation for the printed circuit cards in the demultiplexer function are in section IV. Section V contains the block diagram discussions and detailed theory of operation for the power supply.

5-3. The reference designations for major circuit components, such as U1, Q5, etc, appear in the functional blocks in the block diagrams for the printed circuit cards and power supply to assist in relating the block diagram functional descriptions to the associated detailed theory of operation discussions. The detailed theory of operation discussions, in turn, reference the circuit reference designations as they appear on the associated logic diagrams or schematics in the circuit diagrams manual. The use of logic symbols in the block diagrams is limited to simplified functional applications that are best illustrated by the use of logic symbols. Complete logic circuits are not shown in the block diagrams.

5-4. In the detailed circuit discussions, certain conventions are used to describe and define logic elements. These conventions are described by the following examples.

Example	Description
U1, U2, Q5, etc.	The reference designations used in this manual are the same as those that appear on schematics and logic diagrams, and show physical locations on equipment assembly drawings.
U1-6, U2-4, etc.	Many microcircuit packages in this equipment contain multiple circuits: four AND gates, two shift registers, etc. Therefore, when one or more circuits within one package need to be identified, one of the input or output pins associated with the specific circuit being discussed is added to the reference designation for identification. Normally, an output pin is used to identify a particular circuit.
MGCXX, DGCXX, MMFCX, DMFCX-	All functional signals in the equipment are assigned names. Initial letter M indicates a multiplexer signal; initial letter D indicates a demultiplexer signal. X or XX identifies a particular signal within a signal family; for example, MGCXX consists of 15 signals; MGCO1 through MGC15. The bar signal "-" after a signal name indicates that the signal is low in its true state.

SECTION I

MESSAGE FORMAT AND BASIC EQUIPMENT CONCEPTS

5-5. GENERAL.

Paragraphs 5-6 through 5-18 contain a description of the message format used in the transmission of digital data from the multiplexer in a multiplexer set to the demultiplexer in a far-end multiplexer set. Basic equipment concepts are described in paragraphs 5-19 through 5-67 to introduce maintenance personnel to the unique equipment functions that are performed in the multiplexer set.

5-6. MESSAGE FORMAT.

5-7. OVERALL MESSAGE FORMAT.

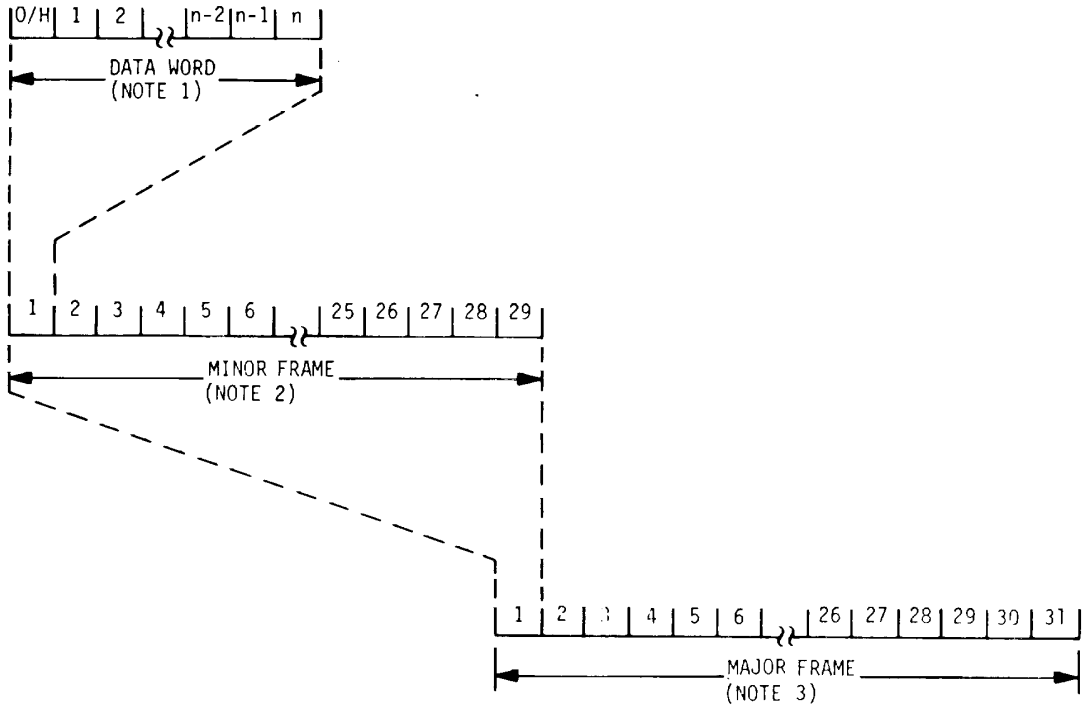
5-8. Data leaving the multiplexer are arranged in a predetermined format as shown in figure 5-1. The message format contains data bits sampled from the multiplexer's channel data inputs interleaved with overhead data bits generated within the multiplexer. Overhead data are inserted for two purposes: to provide a framing or synchronization pattern for use by the receiving demultiplexer, and to inform the demultiplexer of stuffing actions taken by the multiplexer as part of its input rate buffering process. For purposes of enabling proper demultiplexer operation in a high bit error environment, data bits comprising a complete overhead message are evenly inserted over the span of numerous channel data messages, as described in paragraph 5-14.

5-9. The largest organized grouping in the output message format is the major frame. The significance of this grouping is that in addition to sampled channel data, it contains 31 complete overhead messages. Each overhead message consists of a framing pattern and stuffing information pertaining to one of the multiplexer's 31 ports. A complete overhead message in each minor frame is designated as an overhead word. The overhead message content is discussed in greater detail in paragraph 5-14.

5-10 A minor frame contains 29 data words and one complete 29-bit overhead word, and is the second largest organized grouping in the output message format. One bit of the overhead word is located in the first bit position of each of the 29 data words comprising the minor frame. Thus, it can be seen that overhead words appear in the output message format at a rate one twenty-ninth that of data words.

5-11. Each data word contains a sampled channel data bit for each port being used in the multiplexer. As previously noted, an overhead data bit occupies the first data word bit position. The total number of bits contained in a data word is variable, depending upon the number of multiplexer ports in use. Each multiplexer configuration must use a minimum of 15 ports; therefore, the minimum data word length is 16 bits (overhead + 15 channel data bits). The word length can range up to 32 bits (overhead + 31 channel data bits when all 31 ports are in use.

5-12. In summary, a major frame is comprised of 31 minor frames, with each minor frame containing one overhead word. Each 29-bit overhead word consists of a demultiplexer framing pattern and stuffing information pertaining to one of the multiplexer's 31 ports. One overhead bit is located in the first bit position of the 29 data words comprising the minor frame. Remaining data word bit positions, varying in number between 15 and 31, contain a sampled channel data bit for each multiplexer port in use.



NOTES:

1. EACH DATA WORD CONTAINS ONE OVERHEAD (O/H) BIT PLUS ONE DATA BIT FOR EACH USED PORT. TOTAL NUMBER OF WORD BITS FOR A GIVEN CONFIGURATION IS BETWEEN 16 and 32.

2. EACH MINOR FRAME CONTAINS 29 DATA WORDS. AN O/H BIT FROM EACH DATA WORD MAKES UP ONE 29-BIT O/H WORD PER MINOR FRAME.

3. EACH MAJOR FRAME CONTAINS 31 MINOR FRAMES.

6186-54

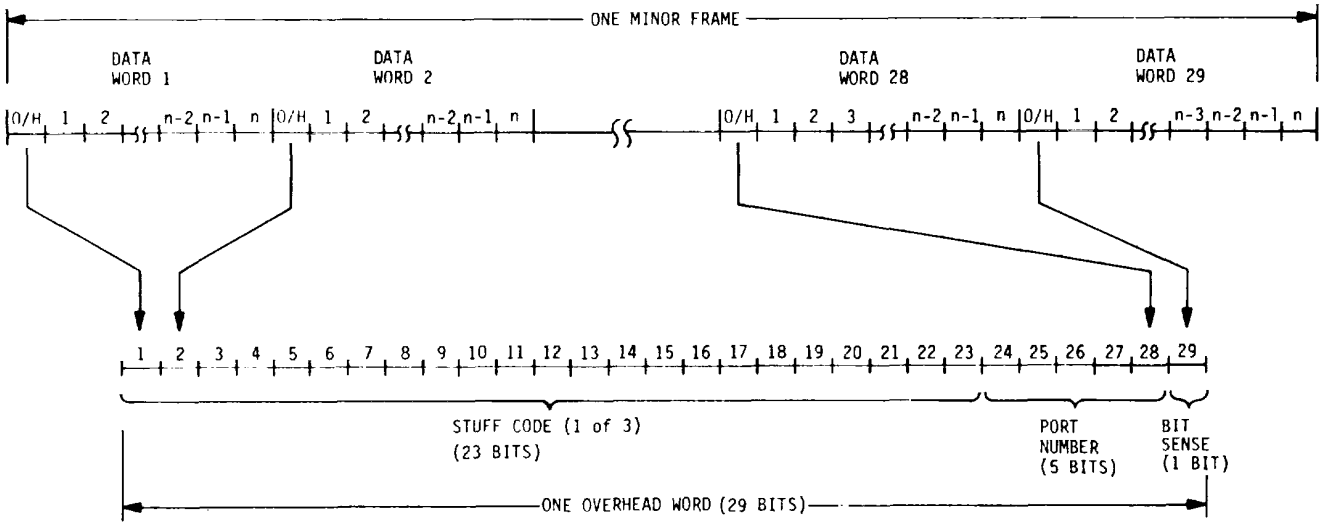
Figure 5-1. Output Message Format

5-13. OVERHEAD MESSAGE FORMAT.

5-14. As noted in the message format discussion in paragraph 5-7, overhead data are inserted in the multiplexer output data stream. The overhead data consist of a framing or synchronization pattern for the receiving demultiplexer, and information regarding stuffing actions performed as part of the multiplexer's input rate buffering process. The latter information enables the demultiplexer to properly perform its destuffing and smoothing operations. A complete overhead message is contained in each minor frame of the multiplexer's output message. The overhead message consists of a 29-bit word, with one bit located in the first bit position of each of the 29 data words comprising the minor frame. Figure 5-2 illustrates the manner in which the overhead word is interleaved into the multiplexer's output. The figure shows that the overhead word conveys three types of information: a 23-bit stuff code, a 5-bit port number, and a sense bit.

5-15. The 23-bit stuff code is one of three different forms, indicating positive, negative, or no-action stuffing operations performed by the multiplexer. Frame synchronization circuits in the demultiplexer are designed to detect and initially synchronize with any one of the three 23-bit stuff codes. Other circuits in the demultiplexer, operating on the basis of the particular stuff code (one of three) detected, control the demultiplexer destuffing and smoothing functions. Thus the 23-bit stuff code serves a dual purpose: it enables initial demultiplexer frame synchronization and determines the type of destuffing and smoothing operation the demultiplexer is to perform.

5-16. To enable the demultiplexer to fully synchronize with the transmitting multiplexer and properly perform its



NOTE: VALUE OF n IN DATA WORD IS BETWEEN 15 and 31.

Figure 5-2. Overhead Message Format

subsequent destuffing and smoothing operations, it is necessary to identify the multiplexer port with which the 23 bit stuff code is associated. The 5-bit port number information is inserted in bit positions 24 through 28 of the overhead word. Upon decoding by the demultiplexer, the port number permits proper presetting of demultiplexer minor frame and word counters. Having detected and decoded the first 28 bits of the overhead word, the demultiplexer is fully synchronized with the transmitting multiplexer and is informed of the type of destuffing it must perform and the port to which the destuffing operation applies.

5-17 When performing a positive stuffing operation (indicated by the first 23 bits of the overhead word), the multiplexer issues an extra gated clock to the port identified in overhead bit positions 24 through 28. The clock forces a data bit from the elastic data storage register located on the channel card with which the indicated port is associated. Since this data bit is actually one bit of channel data, its sense (1 or 0) must be conveyed to the demultiplexer for use in subsequent destuffing operations. Sense of this data bit is inserted into bit position 29 of the multiplexer's overhead word. Because no action and negative stuffing operations performed by the multiplexer do not force a data bit from a multiplexer channel card storage register, sense of overhead bit 29 is of no significance to the demultiplexer when the two stuffing codes are received.

5-18. In summary, a 29-bit overhead word is interleaved into each minor frame transmitted by the multiplexer. The first 23 bits of the word enable initial frame synchronization of the receiving demultiplexer and inform the demultiplexer of the type of stuffing action (positive, negative, or no-action) taken by the multiplexer. The next five overhead bits (24-28) identify the port to which the 23-bit stuffing code applies, and also enable presetting of demultiplexer minor frame and word counters. The 29th overhead bit conveys the sense of the data bit read from a channel card's data storage register when a positive stuffing operation has been performed by the multiplexer.

5-19. MULTIPLEXER BASIC CONCEPTS.

5-20. INTRODUCTION.

5-21. Like most time division multiplexers, the AN/GSC-24(V) design is structured about the use of ports for the combining of applied channel inputs into a single interleaved serial output data stream. Simply stated, a port is an interval of time during which data from a particular channel are allowed into the output stream. The rate at which the porting occurs is termed the port rate (R_p); once established for a given multiplexer set configuration, the port rate remains constant for all ports in use.

5-22 To enable the multiplexer to simultaneously accept input channels of different (mixed) rates, multiple ports are assigned to a single input channel. This arrangement is termed port strapping. The total number of ports assigned to a particular channel may vary between 1 and 25, and the variable is designated as K. The total number of ports assigned to all input channels of a given configuration is simply the sum of all individual channel K values, and is designated as N.

5-23. In addition to the total number of ports assigned to channels in a particular configuration (N), one additional port is always used within the multiplexer for the insertion of overhead data into the output bit stream. Generated internal to the multiplexer, the overhead data include a synchronization pattern for use by the receiving

demultiplexer, and information describing the stuffing actions taken by the multiplexer in the processing of asynchronous channel inputs. Thus the total number of ports, including overhead, used in any given configuration may be expressed as N+1.

5-24. The multiplexer's output rate (R) is the product of the total number of ports used (N+1), and the port rate (R_p), or $R_o = (R_p)$ (N+1).

5-25. Data applied to a multiplexer's input channels may take several forms: digital data with associated timing, voice, and digital data without timing. Within prescribed limits, inputs may be asynchronous with the multiplexer's reference timing source and with each other. Using a variety of input channel card types, all data are converted to a digital form and are subsequently processed as synchronous signals under control of the internally generated multiplexer clock.

5-26. Generally, a digital input channel rate (R_c) will be nominally equal to the product of port rate (R_p) and the number of ports (K) assigned to that channel. In other words, $R_c = KR_p$. For cases where $R_c \neq$ KRp, the multiplexer is capable of performing a rate conversion process termed coarse rate conversion. This entails the use of a KRp that is greater than the applied $_{Rc,}$ and a predetermined sequence of internal timing adjustments. The degree of rate conversion that may be performed is defined by the expression:

$$0.96 \geq K\left(1 - \frac{R_c}{KR_p}\right)$$

The most important benefit resulting from the multiplexer's coarse rate conversion capability is that it enables simultaneous processing of digital channel input rates from mixed rate families. A voice channel is processed in the equipment, using a KR_p of 19.2 kbps or greater

5-27. EQUIPMENT APPLICATION.

Figure 5-3 depicts the use of several multiplexers in a typical system application. In the example shown, numerous lower rate channel inputs are multiplexed in successive steps into a single high-speed output, which is then applied to a communications link. The actual link may take any of several forms, including radio, microwave, or land line. The inputting of one multiplexer with the output of another is commonly known as tandeming, and the overall result is a hierarchy comprised of an output multiplexer being fed by the outputs of other multiplexers operating at successively lower rates.

5-28. Figure 5-3 illustrates the outputs from 20 third level multiplexers No. 3-1 through 3-20 being applied to two second level multiplexers No. 2-1 and 2-2. The outputs from these two multiplexers, plus two independent digital inputs of 2.304 Mbps each, are the inputs to first level multiplexer No. 1. The multiplexed 7.168 Mbs output from multiplexer No. 1 is routed to a communications link for transmission to far-end demultiplexing equipments.

5-29. Multiplexers No. 3-1 through 3-5 each process a combination of voice and digital data inputs using a port rate (R_p) of 9.6 kbps and a total (N+1) of 30 ports. Output rate (R_o) is 288 kbps (9.6 x 30 = 288). Using a port rate of 2.4 kbps and a total of 20 ports each, multiplexers No. 3-6 through 3-20 process a mix of digital inputs and yield an output rate of 48 kbps. Note that the data rate applied to channel 5 of multiplexers No. 3-6 through 3-20 is 2.3 kbps. This rate takes the form Rc< KR . Using the expression

$$0.96 \geq K\left(1 - \frac{R_c}{KR_p}\right)$$

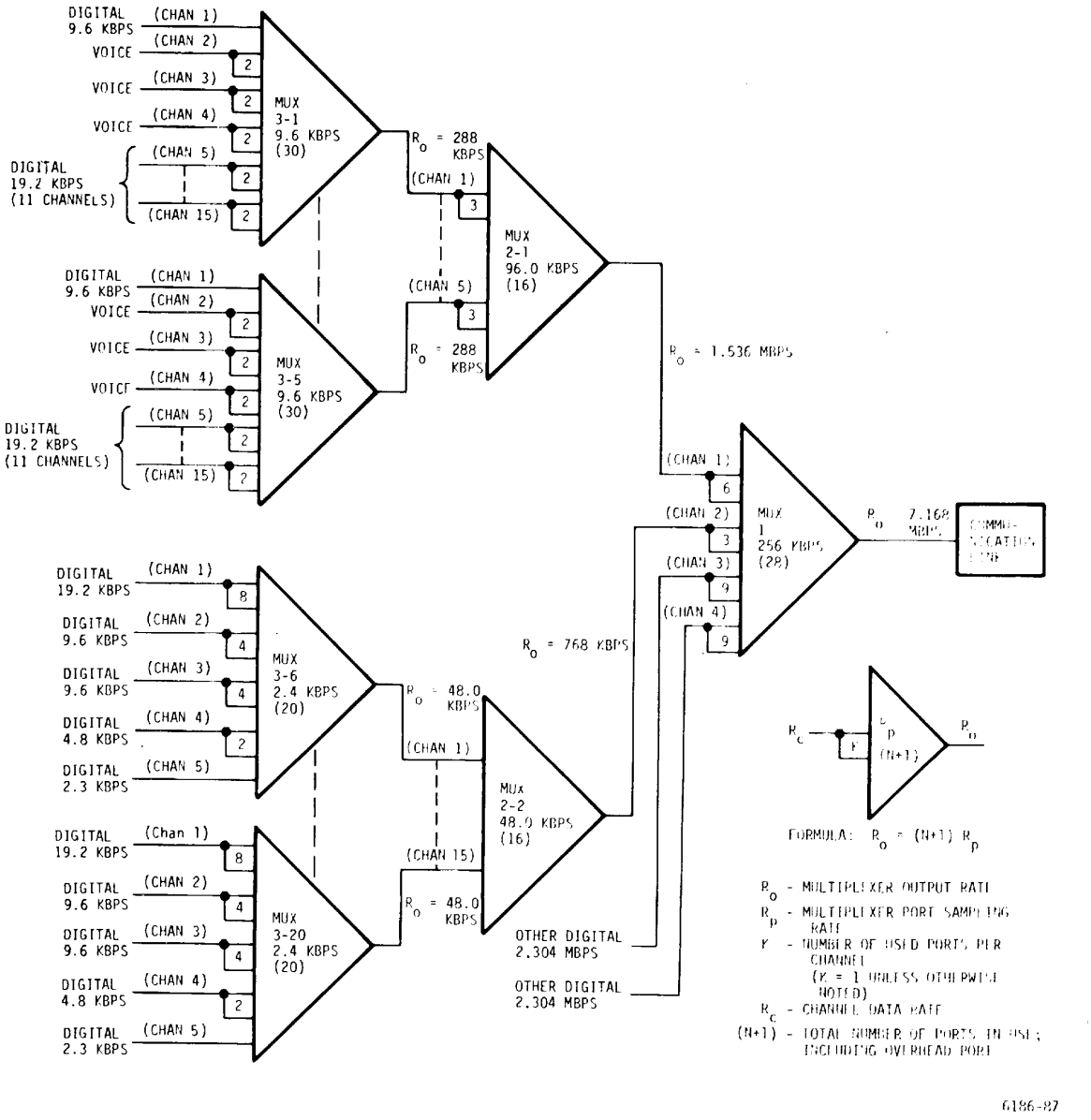


Figure 5-3. Typical Multiplexer Application

these inputs are coarse rate converted within the multiplexer, and subsequently processed as rates of the KR form. The outputs of multiplexers No.P3-1 through 3-20 are time division interleaved data streams carrying the information from a total of 150 input channels [(5 x 15) + (15 x 5)] = 150. After being processed by multiplexers No. 2-1, 2-2, and 1, the combined 150 channels, together with the independent 2.304Mbps channels applied to multiplexer No. 1, appear on a single line that is routed to the communications link. This example shows that the AN/GSC-24(V) multiplexer is an extremely flexible equipment that is capable of combining numerous individual data channels of mixed rates and forms into a single data stream.

5-30. PROCESSING OF ASYNCHRONOUS INPUTS

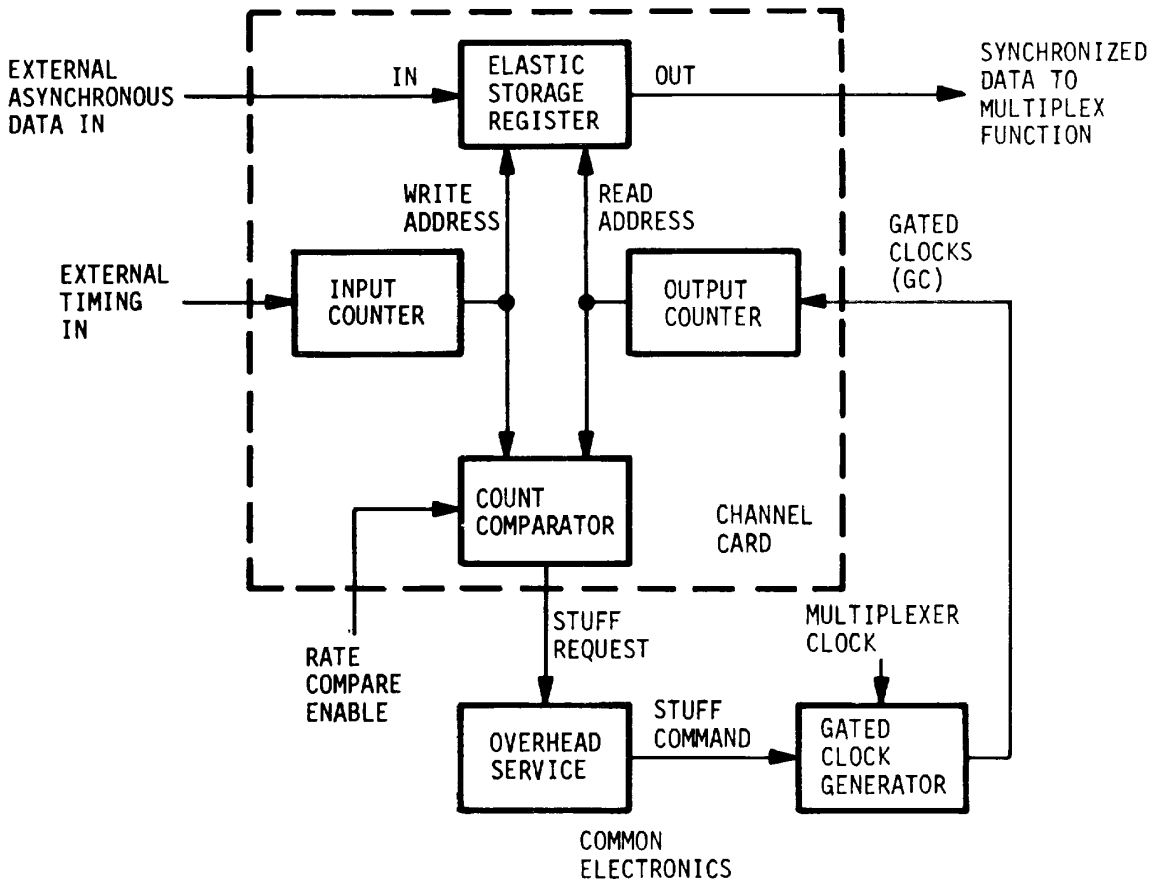
5-31. One primary feature of the multiplexer is its ability to accept and process channel data inputs that are not synchronized with internal multiplexer timing references or with other channel data inputs. Such processing is made possible by the use of a variety of channel cards, each designed to handle a given form of channel data input. The output of each channel card, regardless of type, is a digital representation of the data input applied to the card. Furthermore, the output is synchronized with internal multiplexer timing references and is subsequently processed as a synchronous signal. Channel cards thus provide form conversion and rate or time buffering functions, and present all channel data inputs to the multiplexer common electronics section in a digital synchronized form.

5-32. Figure 5-4 is a simplified block diagram of a typical channel rate buffering arrangement. Both channel card and common electronics elements are used in the rate buffering process. A digital input signal, with associated timing, is applied to the channel card. The input is asynchronous to internal multiplexer timing references. An input counter, clocked by the input timing signal, enables storage of input data bits in successive cells of an elastic storage register. The register is designed to enable simultaneous data storage and retrieval (write and read) under control of independently clocked counters. However, write and read of the same storage cell at the same time is not permitted, so that the input (write) and output (read) counters are nominally maintained at a predetermined offset.

5-33. Data stored in the elastic storage register under control of the input counter are read from the elastic storage register under control of an output counter. The output counter is operated by a gated clock signal derived from the internal multiplexer reference timing source, and is therefore synchronized with other events occurring within the multiplexer common electronics section. The result is a single data storage buffer operated under control of two independently clocked (asynchronous) counters. Since the output counter is clocked by a multiplexer timing source that is considered to be the reference for all multiplexer set internal timing, the result is an asynchronous-to-synchronous conversion of channel data and timing.

5-34. The preceding discussion assumes that the input and output counters addressing the elastic storage register are operated by clock signals of different phases but having the same rate. However, since clocking of the counter is performed by the use of independently generated timing sources, minor differences in clock rates are also encountered.

5-35. Within prescribed limits, the multiplexer is capable of compensating for input counter-to-output counter rate



6186-55

Figure 5-4. Channel Data Asynchronous-to-Synchronous Conversion Functional Block Diagram

variations. Compensation is accomplished by a stuffing process, which is discussed in detail in paragraph 5-48. Since the stuffing operation is actually accomplished by the channel card buffering function described in paragraph 5-32, a preliminary discussion is in order. Referring to figure 5-4, it can be seen that the outputs of the channel card input and output counters are routed to a counter comparator. Under control of a rate compare enable signal generated by the common electronics section, the comparator determines if the pre-established offset between the counters has increased or decreased or remains unchanged since the previous rate comparison was performed. The results of the determination are passed to the common electronics section in the form of a stuff request.

5-36 The overhead servicing portion of the common electronics section receives the request, and at a predetermined time in the overall multiplexer operating

sequence, issues a stuff command to the common electronics gated clock generator. In response to the stuff command, the gated clock generator appropriately adjusts the number of gated clocks sent to the channel's output counter during a predetermined interval. The adjustment causes the output counter again to become offset from the input counter by the established nominal value. For example, if the output counter is determined to be operating slower than the input counter, a gated clock is added. Conversely, a gated clock is deleted when it is necessary to slow the counter. The overall process of gated clock addition/deletion, the sequence in which the operation is performed, and the process by which the operation is reversed at the demultiplexer output is termed overhead servicing. The overhead service function is described in paragraph 5-48.

5-37. The basic input rate buffering, asynchronous-to-synchronous conversion process discussed above is performed by the RCB card, and is applicable to multiplexer channels being inputted with digital data and associated timing. While most channel inputs are in this form, voice and digital data without associated timing are also accepted as channel inputs by the multiplexer. Voice inputs are processed by a VE card. The VE card performs analog-to-digital conversion of the voice signal and provides the common electronics section with a digitally encoded representation of the voice input. The timing used in the encoding process is the gated clock signal. Since the gated clock signal is derived from and is therefore synchronous with the multiplexer reference timing source, the output of the VE card is in the required synchronous digital form.

5-38. Digital data inputs applied to the multiplexer without associated timing are processed by the TE/TR channel card. The TE/TR card operates in one of two modes: transition encoder or timing recovery. Both modes provide the incoming data stream with an associated timing signal. with timing thus supplied, the TE/TR card then uses the previously discussed rate buffering, asynchronous-to-synchronous conversion process to supply the multiplexer common electronics section with synchronous digital data.

5-39. In the TE mode, sense transitions (low to high or high to low) occurring in the input data stream are detected and encoded for subsequent processing. Under control of an independently generated multiplexer timing signal, each detected transition is encoded into a 3-bit data word. The timing signal, which occurs at a rate at least three times that of the nominal input data bit rate, also clocks the input counter of the rate buffering portion of the TE/TR card. As previously discussed, the output of the rate buffering function is synchronous with other timing signals in the multiplexer common electronics section.

5-40. In the TR mode, the TE/TR card accepts a data input without associated timing and provides a timing signal for use in the subsequent rate buffering operation. Timing provided by the TR function is derived from an independent high frequency clock generator on the TE/TR card. Divided to the nominal bit rate of the channel's input data stream, the timing is automatically phase adjusted to coincide with data transitions occurring at this rate. The input data stream, accompanied by its recovered timing, is then routed to the rate buffering function on the card, leaving the card in a digital form that is synchronous with the timing signals in the multiplexer's common electronics section.

5-41. As described in paragraphs 5-31 through 5-40, four methods can be used

in a multiplexer for processing of channel inputs not synchronized with internal multiplexer timing signals. Regardless of their input form (digital with timing, voice, or digital without timing), all channel data inputs are processed by the appropriate channel card type, so that the output from each channel card is in a digital form that is synchronous with the timing of the multiplexer's common electronics section.

5-42. CHANNEL DATA GATING FUNCTION.

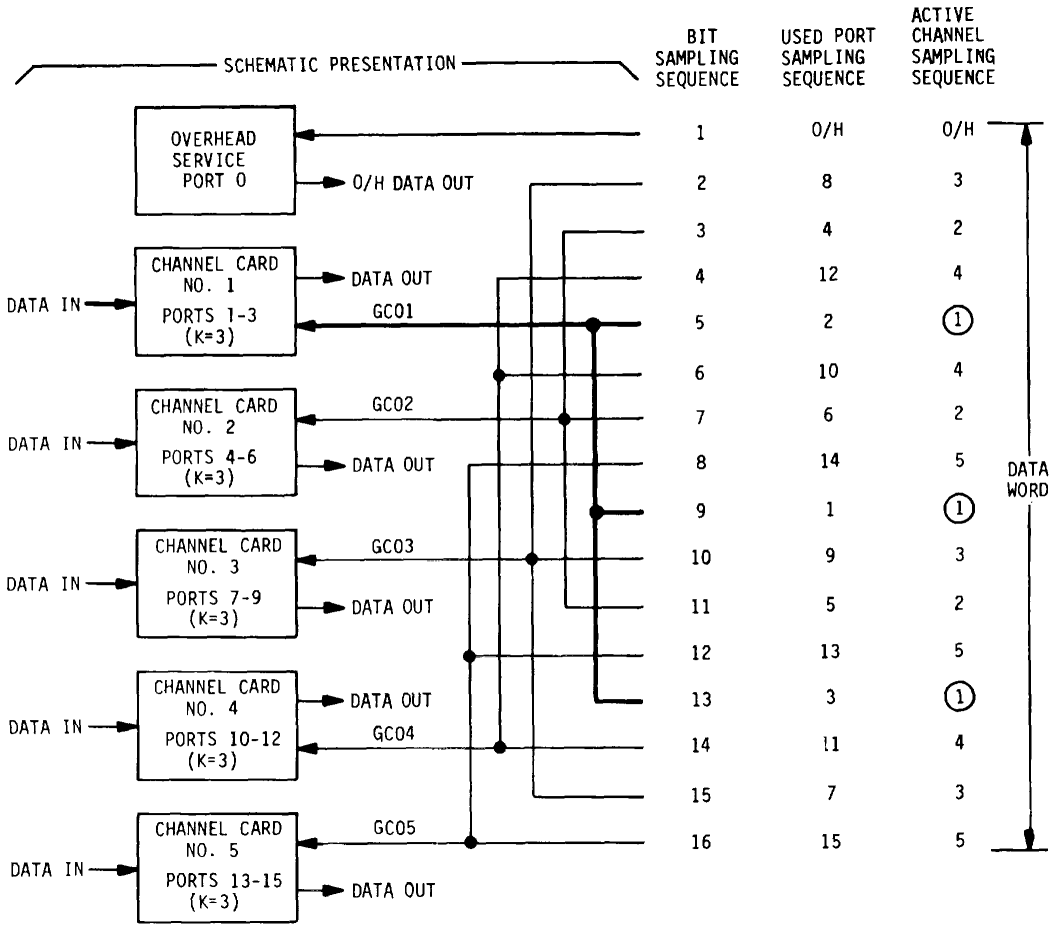
5-43. Each active digital channel in a multiplexer is configured so that, over a given period of time, the bit rate at which the data bits are read out of a channel card is equal to the channel data bit rate at which the data bits are written into the channel card from an external source. Since the data inputs are asynchronous to the multiplexer internal timing functions, data cannot be gated in and out of a channel card in real time on a bit-for-bit basis.

5-44. As described in paragraph 5-30, the data applied to a channel card are converted to a synchronous form. The data bits are clocked out of the channel card by gated clock signals on a bit-by-bit basis: one data bit for each gated clock signal applied to the channel card. Each gated clock signal generated in the common electronics is equivalent to one bit time in the multiplexer output data stream. Also, the number of gated clock signals applied to all channel cards, plus the overhead service bits, is equal to the number of data bits in the multiplexer output data stream over a given period of time.

5-45. The number of ports required to service a given data channel is based on the formula $R_c = KR$ as described in paragraphs 5-23 through 5-26. The rate at which gated clock signals are applied to a given active channel is KR For example, a data channel with a Bit rate (R_c) of 288 kbps requires the use of three used ports (K) when gated clock signals occur at a port sampling rate (R_p) of 96 kbps.

5-46. During each data word period, each used port in the multiplexer normally receives one gated clock signal. Therefore, if a channel has four used ports, that channel normally receives four gated clock signals during a word period. The gated clock signals applied to one multiport channel are not applied sequentially or in a group, but rather are applied in a near-homogeneous sequence as shown in figure 5-5. In figure 5-5, under the "ACTIVE CHANNEL SAMPLING SEQUENCE" column, each entry indicates the channel card that receives one gated clock during the bit time (per word time) listed under the "BIT SAMPLING SEQUENCE" column. Note that channel No. 1 has three used ports and receives a gated clock signal during bits 5, 9, and 13 of the bit sampling sequence A waveform representation for this condition is shown in A, B, and C in figure 5-6. The other four channels shown in figure 5-5 also have three used ports that receive three gated clock signals per bit sampling sequence as indicated in the "ACTIVE CHANNEL SAMPLING SEQUENCE" column.

5-47. The near-homogeneous port sampling sequence shown in figure 5-5 is not random, but is developed by reversing the 5-digit binary numbers that represent bit sampling sequence counts of 1 to 16. Examples of reversing the binary counts are listed below. For a given configuration, the number of ports used is a selected number between 15 and 31. When the port addressed by a reversed binary count is greater than the number of used ports in the configuration, that specific address is automatically bypassed and the next applicable port count is generated without any delay. The following example assumes that the system used has 15 used ports. The use of reverse binary

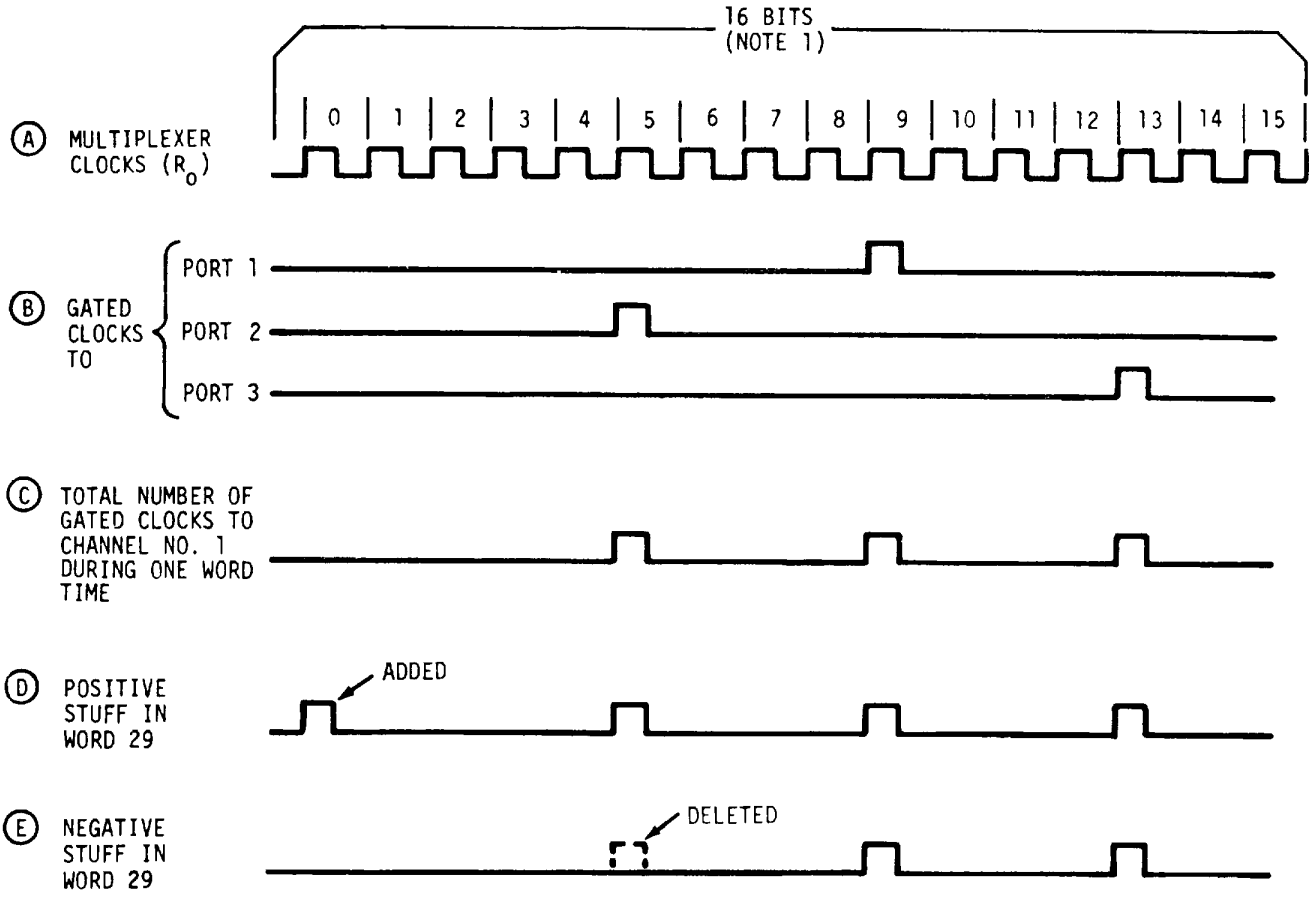


NOTES:

1. TYPICAL CONFIGURATION: DATA WORD CONTAINS 16 DATA BITS (ONE O/H BIT PLUS ONE BIT PER PORT).
2. INDICATES THREE USED PORTS REQUIRED TO SERVICE ONE CHANNEL.
3. O SHOWS HOMOGENEOUS SAMPLING SEQUENCE FOR CHANNEL CARD NO. 1 WITH USED PORTS 1, 2, AND 3.

6186-61

Figure 5-5. Example of Homogeneous Sampling Sequence



NOTES:

1. THESE 16 BITS REPRESENT ONE WORD IN A MULTIPLEXER CONFIGURATION SERVING 15 USED PORTS (1 OVERHEAD PORT + 15 USED PORTS).

2. WAVEFORMS (B) AND (C) REPRESENT CHANNEL NO. 1 CONFIGURED FOR THREE USED PORTS.

3. WAVEFORMS (D) AND (E) (REPRESENT OVERHEAD FUNCTION PERFORMED ON CHANNEL NO. 1 DURING WORD 29 .

6189-60A

Figure 5-6. Gated Clocks - Waveform Diagram

Decimal Count	Binary Count	Reversed Binary Count	Resultant Decimal Count	Used Port Sequence	Associated Channel Sequence
1	00001	10000	16	Bypass	
2	00010	01000	8	8	3
3	00011	11000	24	Bypass	
4	00100	00100	4	4	2
5	00101	10100	20	Bypass	
6	00110	01100	12	12	4

weighting to achieve near-homogeneous gating simplifies the logic implementation required for extracting data from the channel cards. This is further described in the theory of operation for the sequencer card (paragraph 5-265).

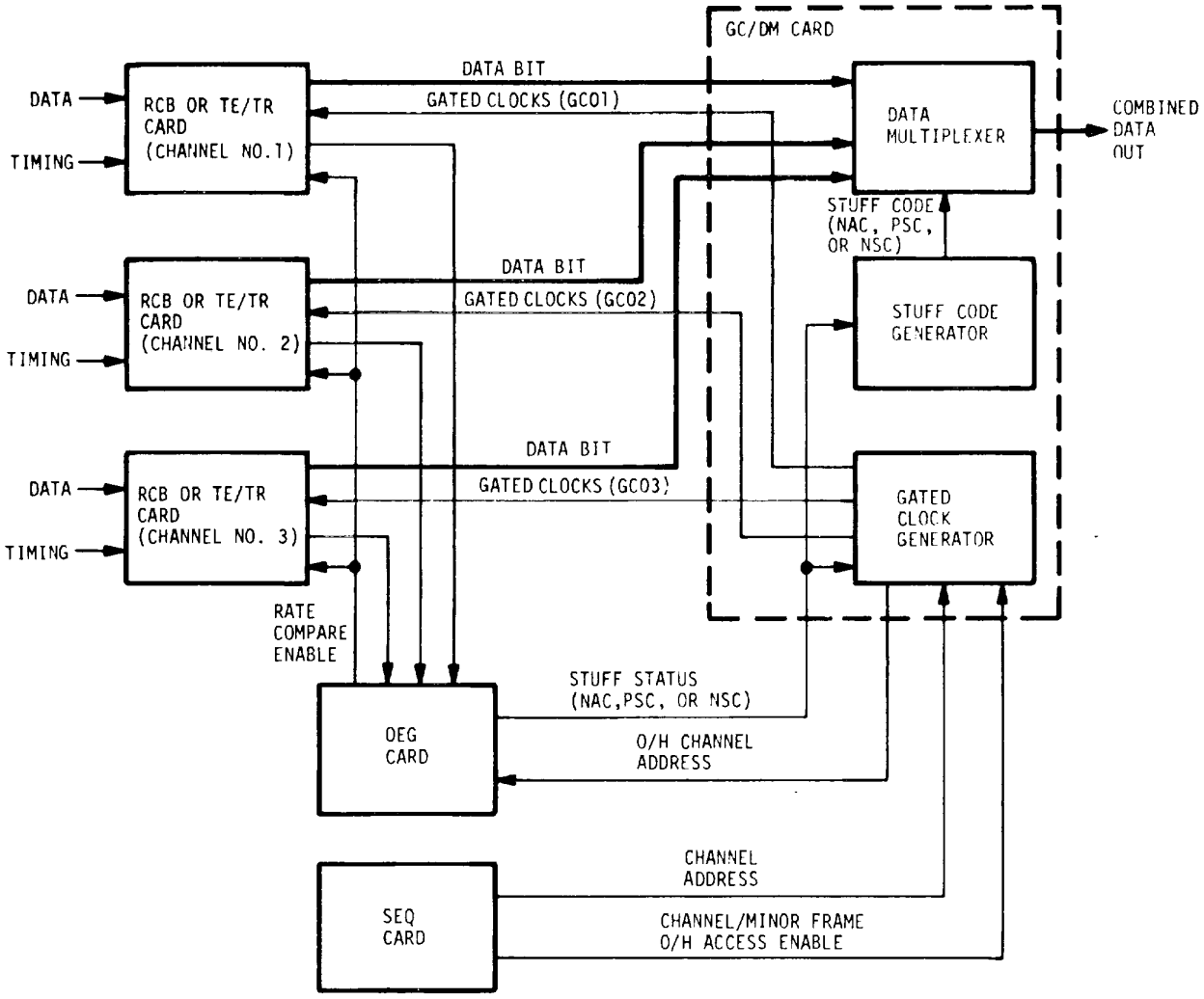
5-48. OVERHEAD SERVICE FUNCTION.

5-49. It is possible that the applied channel data rate could vary with respect to the multiplexer timing rate since the incoming data are asynchronous to the multiplexer set. As described in paragraphs 5-30 through 5-35, the multiplexer channel cards can detect differences in the input and output rates and cause corrective action when the differences are less than $\pm$250 ppm. The differences between the input and output data bit rates are compensated by the use of an overhead service function. Using overhead servicing, the multiplex function has the ability to add or delete gated clock signals sent to the channel card as necessary to maintain bit count integrity.

5-50. Figure 5-7 is a simplified block diagram of the printed circuit card assemblies involved in the overhead service function. Basically, figure 5-7 is an expanded version of figure 5-4 with greater emphasis on the common electronics functions. The overhead service' function is initially activated when a rate compare signal is applied to each channel card from the OEG card. In turn, each channel card responds with one of three requests back to the OEG card: no action, positive stuff, or negative stuff. In this discussion, assume that channel card No. 1 requests no action, channel card No. 2 requests a positive stuff, and channel card No. 3 requests a negative stuff

5-51. A no-action request from channel card No. 1 indicates that the rate at which data are being written into the channel card is the same as the rate at which data are being read out. When the GC/DM gated clock generator card transmits channel No. 1 address to the OEG card, the no-action request signal is applied back to the GC/DM card. As a result, the gated clock generator continues to apply normal gated clock signals GCO1 to channel card No. 1.

5-52. A positive stuff request from channel No. 2 indicates that the rate at which data are being written into the channel card is greater than the rate at which data are being read out. When the gated clock generator on the GC/DM card transmits channel No. 2 address to the OEG card, the positive stuff request signal is applied back to the GC/DM card. As a result, one extra gated clock signal GC02 is generated during word 29 in one preselected minor frame. A channel card is eligible to receive overhead service once in each major frame period during a specific



6186-58

Figure 5-7. Multiplexer Overhead Service - Simplified Block Diagram

minor frame for each used port assigned to the channel. For example, if channel No. 2 has three used ports, up to three extra gated clocks can be received during a major frame period. Each extra gated clock occurs during one specific minor frame period.

5-53. A negative stuff request from channel No. 3 indicates that the rate at which data are being written into the channel card is less than the rate at which data are being read out. When the gated clock generator on the GC/DM card transmits channel No. 3

address to the OEG card, the negative stuff request signal is applied back to the GC/DM card. As a result, one normal gated clock signal GC03 is deleted during word 29 in one preselected minor frame.

5-54. Each additional gated clock signal generated as a result of a positive stuff request occurs during bit 0 in a given word as shown in D of figure 5-6. Each gated clock that is deleted as a result of a negative stuff request occurs in the first bit time assigned to the given channel as shown in E of figure 5-6. In a no-action condition, the channel continues to receive one gated clock in each word period for each used port assigned to the channel.

5-55. DEMULTIPLEXER BASIC CONCEPTS

5-56. Two functions are considered unique to the AN/GSC-24(V) demultiplexer. One is the frame synchronization function, which enables the demultiplexer to acquire and maintain frame synchronization with the transmitting multiplexer. Such synchronization is accomplished in relatively severe error environments. The second function is commonly termed smoothing, and is associated with the demultiplexer's ability to compensate for stuffing operations performed by the multiplexer without inducing unacceptable perturbations in the demultiplexer channel timing outputs. The frame synchronization and smoothing functions are conceptually introduced in paragraphs 5-57 through 5-67.

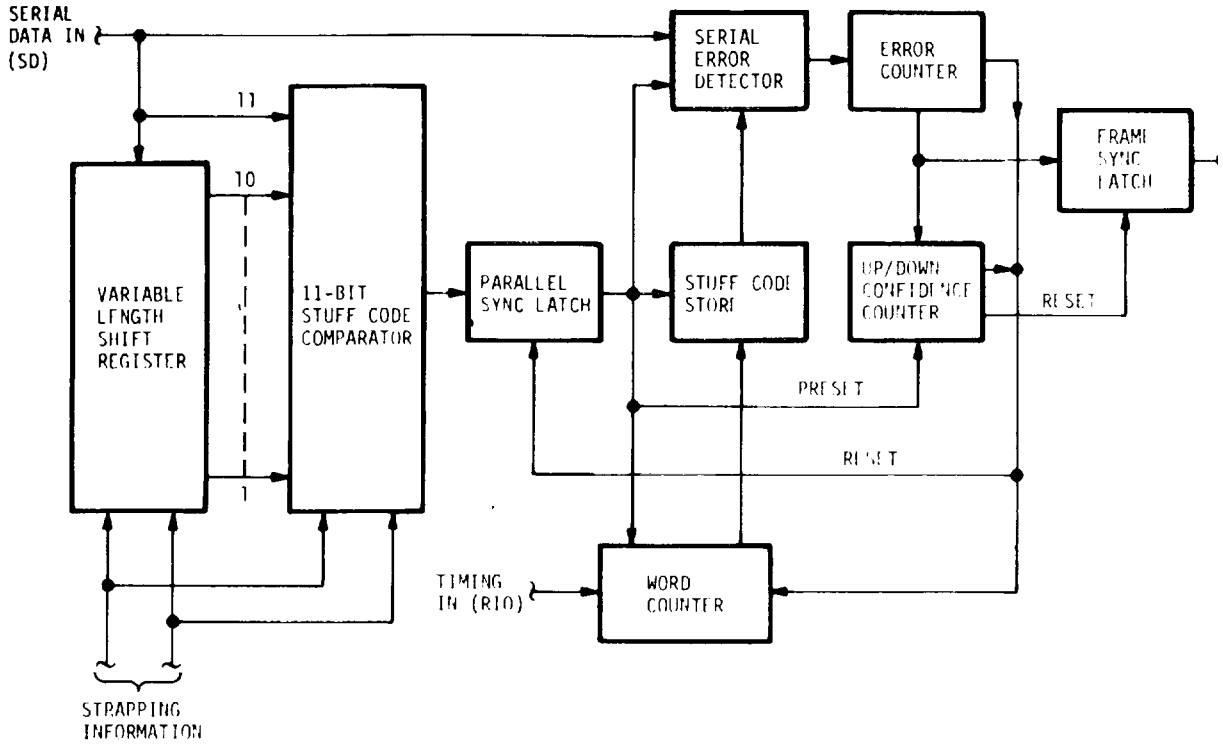
5-57. FRAME SYNCHRONIZATION FUNCTION.

5-58. The demultiplexer uses a frame synchronization technique that enables acquisition and maintenance of frame synchronization in the presence of errors in the received synchronization pattern. Such an arrangement ensures a high degree of bit count integrity in situations where the multiplexer-to demultiplexer transmission link may be subject to data errors induced by atmospheric fading, lightning hits, or other such phenomena.

5-59. Frame acquisition and maintenance by the demultiplexer is accomplished by the use of the 23-bit stuff code pattern inserted in the overhead word of the multiplexer's output (paragraph 5-13). As discussed in paragraph 5-13, each minor frame transmitted by the multiplexer contains one of three stuffing codes in the first 23 bit positions of the 29-bit overhead word. The demultiplexer is designed to recognize any of the three codes and to synchronize its timing circuits with the received code. Within prescribed limits, received codes may contain errors not present when the code was transmitted by the multiplexer.

5-60. The demultiplexer frame synchronization circuits operate in two modes: frame acquisition and frame maintenance. When the demultiplexer first receives data from the transmitting multiplexer, the frame acquisition mode is automatically selected. Once initial frame acquisition is accomplished within prescribed error limitations, the frame synchronization circuits switch to a frame maintenance mode. The circuits remain in this mode until the number of received errors exceeds a second set of prescribed limits or until the demultiplexer data input is otherwise interrupted. Figure 5-8 depicts a simplified block diagram of the demultiplexer frame synchronization function.

5-61. In the frame acquisition mode, serial data entering the demultiplexer are routed to a variable length shift register (VLSR) whose length is controlled by port strapping assignments in the demultiplexer common electronics section. The varying of shift register length is set to correspond to the variable length data word transmitted by



6186-85

Figure 5-8. Frame Synchronization Function - Simplified Block Diagram

the multiplexer (paragraph 5-11). An 11-bit stuff code comparator performs a broadside or parallel search for an exact match between the data flowing through the VLSR and one of three stuff codes contained in the comparator. When one of the three codes is detected without errors, the stuff code comparator sets a parallel sync latch. This latch, in turn, presets the demultiplexer word counter and an up/ down confidence counter, and enables a serial error detector. The word counter is preset to 12, since the next received multiplexer word is 12. The confidence counter is set to a count of 5. Once parallel sync is established without detected errors in the first 11 bits of the received framing code, the next 12 bits (11 + 12 = 23 total stuff code bits) of received overhead data are compared serially by the serial error detector. To enable comparison, the stuff code store provides the remaining 12 bits of the appropriate one of the three known code possibilities under control of the word counter. Each error detected during the serial comparison is counted by an error counter whose output is routed to the up/down confidence counter. If the number of errors detected during the serial code comparison is two or less, the frame sync latch is set and the frame synchronization circuits automatically switch to a frame maintenance mode. If more than two errors are detected, the word counter and parallel sync latch are reset and the frame acquisition cycle is initiated again.

5-62. Frame maintenance is accomplished by a serial 23-bit comparison of the received overhead stuffing codes and known codes provided by the stuff.

code store. In the frame maintenance mode, each 23-bit pattern containing seven or less errors causes the up/down confidence counter to be incremented by one count, and the frame sync latch to remain set. Each received code containing more than seven errors causes the up/down confidence counter to be decremented by one count. If several successive codes containing more than seven errors are detected, the confidence counter is decremented to 0 and the frame sync latch is reset to a loss-of-frame condition. In such an event, the frame acquisition mode is again automatically initiated.

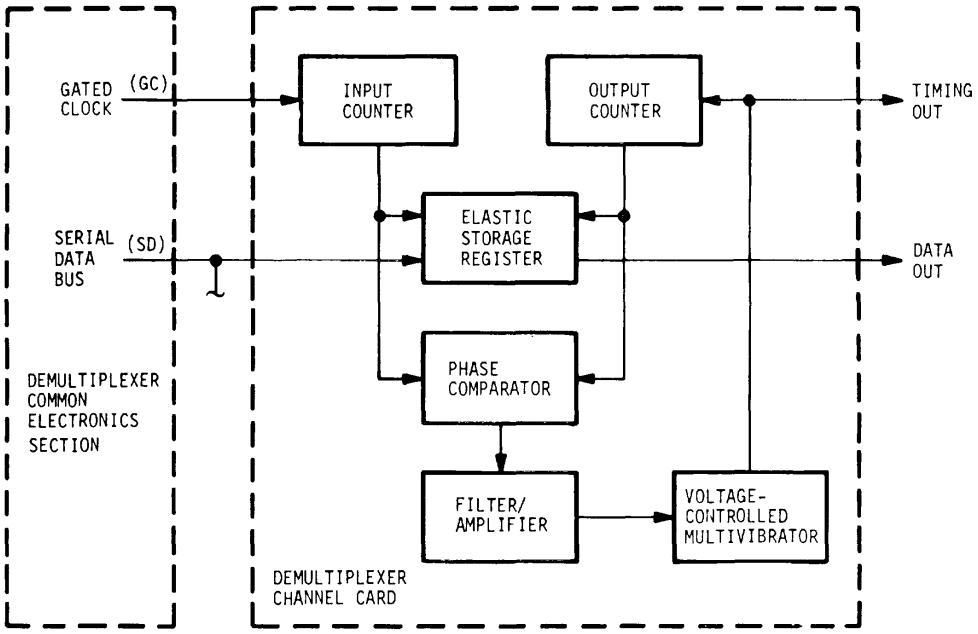
5-63. Based upon the above discussion, it can be established that the demultiplexer frame synchronization function operates in two automatically selected modes: acquisition and maintenance. Frame acquisition is accomplished by a combined parallel and serial search for one of the three overhead stuffing codes transmitted by the multiplexer. Frame maintenance is achieved by a 23 bit serial search for one of the three possible codes. In either the acquisition or maintenance mode, a prescribed number of detected code errors may be present without causing disruption of the overall frame synchronization process. Further discussion of the frame synchronization function is presented in paragraphs 5-108 and 5-472.

5-64. SMOOTHING FUNCTION.

5-65. When outputting data other than voice, channel cards in the demultiplexer perform a synchronous-to-asynchronous buffering process that is the inverse of the stuffing operation performed in the multiplexer. The demultiplexer destuffing process results in reinsertion of those rate variations that were present at the transmitting multiplexer's channel inputs.

5-66. A smoothing function is also accomplished by an analog phase-locked loop arrangement as depicted in simplified form in figure 5-9. Under control of a gated clock (GC) signal generated within the demultiplexer common electronics section, data bits associated with a given channel are read from the serial data bus into the channel card elastic storage register. The GC signal exactly matches the GC signal applied to the transmitting multiplexer channel card, and therefore may have individual clocks added or deleted as necessary to accommodate channel rate variations applied to the multiplexer's channel input. Data in the demultiplexer channel card's elastic storage register are read out under control of a clock provided by a voltage-controlled multivibrator (VCM). Located on the channel card, the VCM is configured to operate independent of the GC at the channel's nominal output data rate, and also provides the channel's output timing signal.

5-67. Since there are variations in the rate of the GC timing signal, the VCM and GC signals are phase locked to prevent underflow or overflow of the elastic storage register. A phase comparator determines when a predetermined offset between the channel card's input and output counters increases or decreases beyond acceptable limits. When an unacceptable offset is detected, the phase comparator yields a corresponding error signal that is routed, via a filter/amplifier network, to the frequency control input of the VCM. Thus, when the input counter is determined to be operating faster than the output counter, the resultant error signal causes an increase in the VCM output frequency. In turn, when the input counter is determined to be operating slower than the output counter, the resultant error signal causes a decrease in the VCM output frequency. The net effect is that the input counter and output counter timing sources are phase locked. Circuits within the filter/amplifier network are



6186-86

Figure 5-9. Smoothing Function - Simplified Block Diagram

designed to integrate the error signal output of the phase comparator. Therefore, a detected input/output counter offset is corrected over numerous periods of the VCM output rather than instantaneously. The correction process over an extended time interval assures a smooth variation in the channel's output timing signal and provides the basis for the term smoothing. A more detailed discussion of the smoothing function is presented in paragraph

SECTION II

MULTIPLEXER, DEMULTIPLEXER, AND OVERALL DIAGNOSTICS FUNCTIONAL BLOCK DIAGRAM DISCUSSIONS

5-68. This section contains separate functional block diagram discussions for the multiplexer, demultiplexer, and overall diagnostics. The overall diagnostics functional block diagram discussion includes the diagnostic circuits associated with the multiplexer, demultiplexer, and power supply. The block diagram discussions of the circuits on the front panel are also incorporated into the overall diagnostics circuit discussion.

5-69. OVERALL MULTIPLEXER FUNCTIONAL BLOCK DIAGRAM DISCUSSION.

5-70. GENERAL. A multiplexer configuration uses between 1 and 15 channel option cards to receive up to 15 channels of asynchronous digital data and/ or voice data from associated communications links. The three types of channel cards that can be used to receive data in a multiplexer configuration are shown in figure FO-1. The block diagram also shows the four common cards in a multiplexer configuration that generate the timing and control signals that perform the time-division multiplex and overhead service functions for the incoming channel data.

5-71. RATE COMPARISON BUFFER (RCB) CARD.

5-72. The RCB card receives asynchronous data that are clocked into a temporary storage register by its own associated timing signals. At a later time, data are clocked out of the storage register and are routed to the GC/DM card by signals that are synchronous with the multiplexer timing function. The write and read functions for the storage register are independent of each other; the only restriction is that data written into a given address cannot be simultaneously read out of the address.

5-73. As shown in figure FO-1, digital data signals DIXX are applied to a data receiver on the RCB card. The data receiver conditions the data into TTL levels compatible with the logic circuits in the multiplexer. The associated timing signals are applied to a timing receiver that conditions the signals into TTL levels. The conditioned timing signals are routed to increment the write address counter. The write address counter, in turn, generates sequential write addresses that clock the conditioned data into the data elastic storage register. The read address counter is sequentially incremented by gated clock signals (MGCO1) that are applied at a port rate (R_p) nominally the same as the incoming data rate. The read address counter is offset from the write address counter so that the read address selected at any given time is always delayed from the write address. The data are therefore not simultaneously read in and out of the register for a given address. The data read out of the register are applied to the data output buffer. The data are clocked through the buffer to the GC/DM card by multiplexer clock signal MRI01-.

5-74. The rate compare and stuff request circuits on the RCB card are part of the multiplexer overhead service function to compensate for changes in the incoming bit rate. The rate compare circuits detect any variation between the incoming bit rate and the

precision multiplexer channel sampling rate (KRp) applied to the channel. During word 24, the rate comparison function is initiated by word 24 bit 0 signal MW2401 from the OEG card. At this time, the rate compare circuits effectively subtract the count in the write address from the count in the read address. In normal operation, there is a predetermined difference count between the two addresses. When the difference count from a rate compare is the predetermined figure, a no action request is generated. When the incoming bit rate increases, the difference count indicates that the write address is greater than the read address. At this time, a positive stuff request is generated and applied to the OEG card. As a result, an additional gated clock pulse applied to the RCB card effectively helps the read address counter to catch up. When the difference count indicates that the incoming bit rate has decreased, the write address is less than the read address and a negative stuff request is generated. The result is that one normal gated clock pulse to the RCB card is deleted, which effectively slows down the channel sampling rate of the read address counter. The stuffing action for either the positive or negative stuff condition continues as long as the rate compare circuits determine that the incoming bit rate and the channel sampling rate are not nominally the same. Each used port assigned to a given channel is eligible to receive overhead servicing during one minor frame in each minor frame period.

5-75. Initially, when an RCB card is configured for a data channel and the applied data rate to the card is the same (within $\pm$250 ppm) as the channel sampling rate applied to the card, the RCB/URC switch on the card is set to the RCB position. With the switch in the RCB position, the circuits on the card function as described above. When the channel sampling rate for a channel not be configured to be within $\pm$250 ppm of the incoming data rate, a channel sampling rate that is higher than the incoming data rate is selected. In this configuration, the RCB/URC switch on the card is set to the URC position to place the coarse rate conversion circuits in series with the applied gated clocks. The coarse rate conversion circuits are configured to delete a predetermined number of gated clock signals and effectively lower the channel sampling rate to within +250 ppm of the incoming data rate. The word 24 signal MW24N1, end-of-scan signal MEOS3NX, and minor frame terminal count signal MMFC31 are timing signals that control the selection of the individual gated clock pulses that are deleted, inhibit the coarse rate conversion circuits during word 29 when overhead servicing is performed, and preset the circuits after each major frame period. The coarse rate conversion circuits are independent of the positive and negative stuff function performed in the rate conversion buffer circuits as described in paragraph 5-74. Fixed amounts of gated clock pulses are deleted by the coarse rate conversion circuits during each major frame period.

5-76. TRANSITION ENCODER/TIMING RECOVERY (TE/TR) CARD.

5-77 The TE/TR card processes digital data that are applied to the multiplexer without timing. The circuits on the card are divided into three functional circuits: the transition encoder circuits that receive and process digital data whose bit rate is 400 bps or less; the timing recovery circuits that receive and process digital data whose bit rate is 75, 100, 150, 300, 600, 1200, 4800, or 9600 bps; and the rate comparison buffer (RCB) circuits that receive the data from the transition encoder or the timing recovery circuits and resynchronize the data bits with the multiplexer timing as described in the RCB card discussion.

5-78. The timing recovery (TR) circuits generate the timing signals that are synchronized with the incoming asynchronous digital data. As described in the RCB card discussion, the timing signals are necessary to clock the incoming data pulses into the RCB circuits. The data receiver in the timing recovery circuits conditions the applied digital data (DIXX) into TTL levels that are compatible with the logic circuits on the card. The data pulses are applied to a transition detector circuit and to the RCB circuits. The transition detector circuit applies a reset signal to the timing generator circuit each time a pulse transition occurs. The timing generator circuit, in turn, receives a continuous timing output from the timing oscillator. The timing signals are divided down to produce the selected timing output rate that is the same as the incoming data bit rate. By resetting the timing generator circuits each time a positive-going or negative-going pulse transition occurs, the continuous TR timing signals to the RCB circuits are effectively held in synchronization with the conditioned data pulses applied to the RCB circuits.

5-79. The transition encoder circuits generate the timing signals that are synchronized with the incoming asynchronous digital data. The data receiver in the transition encoder circuits conditions the applied digital data and applies the conditioned pulses to the 3-bit transition encoder circuits. Each time a positive-going or negative-going transition of a data pulse occurs, the 3-bit transition encoder circuits generate a 3-bit digital code that is synchronous with the TE timing pulses being applied to the RCB circuits. The 3-bit code identifies the following: that a transition has occurred; the position of the transition as related to the first half or the second half of the timing signal at the time of transition; and that the pulse transition is a positive-going or a negative-going transition. The timing signals from the timing generator to the RCB circuits are developed from the T4800 or the T3600 (Hz) timing signals from the RT card. The selected timing rate is either 225, 300, 450, 600, 900, or 1200 Hz, corresponding to the input rate ranges of 75, 100, 150, 200, 300 or 400 bps, respectively. The timing signals also synchronize the 3bit code output from the encoder so that the 3-bit data codes and the TE timing signals applied to the RCB circuits are synchronous

5-80. The TE/TR switches on the card are set to apply the data and associated timing signals from the TE or TR circuits to the RCB circuits. The RCB circuits process the incoming data to be synchronous with the multiplexer timing functions as described for the RCB card. The RCB circuits on the TE/ TR card do not have the coarse rate conversion circuits associated with the RCB card. The data output (MDT002) is clocked to the GC/DM card by system clock signal MRI02-. The positive and negative stuff request signals (MPST02 and MNST02) are applied to the OEG card.

5-81. VOICE ENCODER (VE) CARD.

5-82. The VE card receives one voice channel and converts the incoming analog signals into synchronous digital data that can be combined with other data channels in the GC/DM card. The VE card processes signals in the range of 150 to 3500 Hz. The voice signals are applied to a voltage comparator circuit that compares the incoming analog signals with a reconstructed analog signal voltage from the D/A conversion circuits. In real time, the reconstructed analog signals should be almost identical to the incoming analog signals to the card. The difference voltage developed in the voltage comparator circuit is applied as an error voltage to the digital sample and control circuits.

5-83. In normal operation, an analog error voltage, which continually varies in amplitude and polarity, is generated from the voltage comparator. The error voltage is translated into digital data in the digital sample and control circuits. The digital data from the digital sample and control circuits are applied to the data output buffer and to the D/A conversion circuits. The data from the data output buffer are clocked to the GC/DM card by multiplexer clock signal MRI02-.

5-84. The digital data applied to the D/A conversion circuits are converted from digital to analog voltages that are representative of the incoming voice signals. The reconstructed signal voltages from the D/A conversion circuits are identical to the voltage waveforms that will be decoded in the far-end demultiplexer. A slope control signal from the digital sample and control circuits effectively speeds up the D/A conversion circuits to track and convert the higher frequency and/or higher amplitude segments of the voice signals with a minimum amount of distortion.

5-85. SEQUENCER (SEQ) CARD.

5-86. The seq card generates the channel address, end-of-scan, and overhead MMF=PS signals that are applied to the GC/DM card for timing purposes. The PORT STRAPPING switches on the card are manually set to select up to 15 active channels and up to 31 used ports. The PORTS IN USE switches on the card are set to indicate the maximum number of used ports in a given system configuration. End-of-scan timing signals are generated on the card and applied to the GC/DM card and the OEG card.

5-87. The channel address generation circuits on the seq card generate 4-bit binary channel address signals MCHAD1 through MCHAD8. These signals, which are generated at the system clock rate (MRIO), are routed to the GC/DM card. Each 4-bit channel address applied to the GC/DM card causes one gated clock signal to be generated to the channel card contained in the channel address.

5-88. The end-of-scan generator circuits generate end-of-scan signal MEOS, which is applied to the OEG card when the port count in the sequencer timing circuits is equal to the maximum number of used ports selected by the PORTS IN USE switches. End-of-scan signals MEOS2B and MEOS2B- are derived from signal MEOS and applied to the GC/DM card. The end-of-scan signals effectively represent one word period.

5-89. The overhead port sequence selector circuit produces minor frame equals port sequence signal MMF=PS, which is applied to the GC/DM card. The signal is generated during each minor frame period that is eligible to provide overhead service to an assigned used port.

5-90. OVERHEAD ENABLE GENERATOR (OEG) CARD.

5-91. The OEG card generates negative and positive stuff request signals, as well as timing signals used by other cards in the multiplexer. Negative and positive stuff request signals MPSTOX and MNSTOX are applied to the OEG card from the active channels that use the RCB card or the TE/TR channel card. Each channel card input to the OEG card is interrogated for a stuff request as selected by the overhead address count signals MOHO through MOH3. The overhead count address signals are applied to the address select inputs on the stuff request multiplexers. When the selected channel has a positive or negative stuff request, a positive stuff request signal MPSA- or a negative stuff request signal MNSA- is applied back to the GC/DM card.

5-92. The word 24 generation circuits generate word 24 bit 0 signal MW240X and word 24 signal MW24NX when the word count in signals WCO through WC4 from the GC/DM card contains a count of 24 and multiplexer clock signal MRIO occurs. The word 24 signals are applied to the channel cards to initiate the overhead service function as described in the RCB card discussion. The end-of-scan generation circuits produce end-of-scan signal EOS2 to the word 24 generation circuits when end of-scan signal MEOS is applied from the seq card. At the same time, the circuits also generate end-of-scan signal MEOS3NX that is applied to the RCB cards in the multiplexer.

5-93. The system clock distribution circuits receive system clock signal from the RT card and, in turn, generate the multiplexer clock signals MRIO1- through MRI08-. These signals are distributed to the channel cards as timing signals. System clock signal MRIO that is applied to the GC/DM card is identical to system clock signals MRIO1- through MRI08-.

5-94. GATED CLOCK/DATA MUX (GC/DM) CARD.

5-95. The GC/DM card receives and combines the channel data from the active channel cards into one serial data stream that is applied to the RT card. Control and timing signals used in the multiplexer function are also generated on the card as described below.

5-96. The word generation circuits generate word count signals WCO through WC4 to provide 5-bit sequential word counts 1 through 29. The signals are applied to the stuff code generation circuits. Word count signals WCO, WC1, and WC2 are applied to the overhead data multiplexer, and word count signals WCO, WC1, WC2, and WC4 are applied to the OEG card. The circuits also generate word 27 signal W27, word 28 signal MW28, and words 24 through 29 signal MWC2429 that are used for timing purposes on the card. Word 28 signal MW28 is routed to the seq card as a control signal.

5-97. The stuff code generation circuits generate three different 23-bit stuff command codes: the positive stuff code (PSC), the negative stuff code (NSC), and the no action code (NAC). All three codes are generated at the same time, during word counts 1 through 23, and are applied to the overhead data multiplexer.

5-98. The minor frame generation circuits produce minor frame count signals MMFCO through MMFC4 that sequentially count minor frames 1 through 31. These signals are applied to the overhead data multiplexer and to the seq card. During minor frame count 31, minor frame terminal count signal MMFC31 is generated and applied to the channel cards that use the RCB card. Signal MMFC31 represents one major frame period. The minor frame count is advanced one count each time end-of-scan signal MEOS2B- from the seq card and word 29 signal W29 from the word generation circuits occur.

5-99. The gated clock generation circuits generate gated clock signals (MGCO1 through MGC15) as required to service the active channel cards. One gated clock signal is generated for each active channel. For example, a multiplexer with 10 active channels uses gated clock signals MGCO1 (channel 1) through MGC10 (channel 10). Each gated clock signal applied to an active channel gates one channel data bit to the output data multiplexer on the card. At the same time that a gated clock signal is generated, 4-bit binary channel address signals GCAD1 through GCAD8, which contain the same address as the active channel being

serviced, are generated and applied to the select inputs on the output data multiplexer. Each used port in an active channel in the multiplexer receives one gated clock signal that gates one data bit to the GC/DM card during each word time; the exception is during word 29 when overhead servicing is performed. When positive stuff enable signal MPSE is applied to the circuits during word 29, one additional gated clock signal is generated to the active channel selected for overhead servicing. In turn, when negative stuff enable signal MNSE is applied, one gated clock signal, which is normally applied to the selected active channel, is deleted as part of the overhead service function.

5-100. The overhead data multiplexer combines the overhead data inputs for a given port selected for overhead servicing into a serial format. The serial overhead data are clocked into the output data multiplexer during bit 0 of each data word period. Words 24 through 29 signal MWC2429-enables minor frame count signals MMFCO through MMFC4 to be applied, one bit at a time, to the overhead data multiplexer. Word count signals WCO, WC1, and WC2 sequentially clock the five minor word count signals into the output data multiplexer. The appropriate 23-bit stuff code clocked into the overhead data multiplexer during words 1 through 23 is selected by positive stuff request signal MPSA or negative stuff request signal MNSA from the OEG card. The absence of both signals from the OEG card enables the no-action code. When signal MPSA is applied to the multiplexer, positive stuff enable signal MPSE is generated and applied to the gated clock generation circuits. When signal MNSA is applied to the multiplexer, a negative stuff enable signal is generated and applied to the gated clock generation circuits. The output from the overhead data multiplexer is the serial 29-bit overhead message that is applied to the output data multiplexer during bit 0 of words 1 through 29.

5-101. The output data multiplexer interleaves, one bit at a time, the data inputs from each of the active channels and the overhead data input from the overhead data multiplexer. The high-speed serial data stream (MSD) from the multiplexer is applied to the RT card. The 4-bit binary channel address signals GCAD1 through GCAD8 select the appropriate overhead or data channel input to the multiplexer at the system clock rate MRIO. The channel address applied to the multiplexer is the same channel address in the gated clock signal that is generated at any given time. For example, channel 2 is receiving a gated clock signal MGC02 at the same time that the channel address signal for channel 1 is applied to the multiplexer. The high-speed serial data stream is clocked out of the multiplexer by system clock signal MRIO.

5-102. REFERENCE TIMER (RT) CARD.

5-103. The RT card produces system clock signal $_{Ro}$ and timing signals T3600 and T4800 used in the multiplexer cards. The high-speed serial data stream (MSD) from the GC/DM card is conditioned in the RT card and is then applied, with associated timing signals, to the rear panel, where the signals are fed into a balanced or unbalanced cable system.

5-104. The high-speed serial digital data stream from the GC/DM card is clocked into the output data line driver by system timing signal $_{Ro.}$ The digital data are conditioned into digital signals that can be applied to a balanced line or an unbalanced line input. In a balanced line configuration, the output data signals are transmitted as complementary serial data out signals SDATO and SDATO-. In the unbalanced line configuration, signal SDATO-is terminated (grounded). System

timing signal $_{Ro}$ and multiplexer timing out signals TIMOUT and TIMOUT- are generated by the output timing line driver. These timing signals are derived from an external timing reference source that is applied through the EXT position of the EXT/INT switch, or from a precision master oscillator on the RT card through the INT position of the EXT/INT switch. In a balanced line configuration, the timing signals are transmitted as complementary signals TIMOUT and TIMOUT-. In the unbalanced configuration, signal TIMOUT- is terminated (grounded). The output timing line driver also generates system clock signal R_o that is identical to the TIMOUT signal. Signal is applied to the OEG card.

5-105. The timing recovery (TR) timing generation circuits produce precision 3600-Hz and 4800-Hz timing signals that are applied as timing signals T3600 and T4800 to the TE/TR cards in the multiplexer.

5-106. OVERALL DEMULTIPLEXER FUNCTIONAL BLOCK DIAGRAM DISCUSSION.

5-107. GENERAL. A demultiplexer configuration uses between one and 15 channel option cards to process up to 15 channels of asynchronous digital data (with or without timing) and/or voice data outputs to associated communications links. The four types of output channel cards that can be used in the demultiplexer are the SB, NBSB, TD, and VD cards. Five common cards used in the demultiplexer generate the timing and control signals for demultiplexing the applied high-speed serial data stream from the far-end multiplexer. The OEG, GC/DM, seq, FS, and ERD cards are the common cards in the demultiplexer. The overall demultiplexer block diagram is shown in figure FO-2.

5-108. FRAME SYNC (FS) CARD.

5-109. The FS card buffers the incoming high-speed digital data and distributes the incoming data to all the channel cards in the demultiplexer. A frame synchronization function and an overhead decode function are also performed on the FS card. The frame synchronization function synchronizes the demultiplexer timing generation circuits to the timing associated with the incoming data. The overhead decode function decodes one of the three stuff codes that are in the overhead message during each minor frame period.

5-110. The incoming high-speed digital data stream (DATA) is applied to the data receiver circuits where the data are conditioned into the TTL levels that are compatible with the logic circuits in the demultiplexer. The data for the data receiver are applied to the channel data output shift register, parallel sync acquisition circuits, and serial sync and sync maintenance circuits. The data are clocked through the channel data output shift register by system input clock signals RIO from the timing receiver circuits. The shift register output is inhibited by the absence of frame sync signal DFS from the serial sync and sync, maintenance circuits when frame synchronization is lost. In normal operation, demultiplexer input data signals (DTIX-) clocked through the shift register are routed to each channel card in the demultiplexer,

5-111. The parallel sync acquisition circuits establish the initial synchronization of the demultiplexer timing with she incoming data timing. The circuits search the applied data for the first 11 bits of the overhead message located in bit 0 of the first 11 words. Since the first 23 bits of the

overhead message contain one of the three fixed stuff command codes, the first 11 bits are predictable and can be identified. When the first 11 bits of one of the three stuff command codes is identified, demultiplexer frame sync signal DSYNC- is generated and applied as an enable signal to the serial sync and sync maintenance circuits. Signal DSYNC- is also applied to the seq card to synchronize the channel address generation circuits with the incoming data timing. The serial sync and sync maintenance circuits then monitor overhead bits 12 through 23 in the overhead message during the same minor frame in which bits 1 through 11 were identified. When overhead bits 12 through 23 are successfully identified as part of a given stuff command code, frame synchronization is effectively completed. At the time that signal DSYNC is applied, the serial sync and sync maintenance circuits produce demultiplexer word counter preset signal DWPR that is applied to the GC/DM card to synchronize the gated clock generation circuits with the incoming data timing.

5-112. Once frame synchronization is established, demultiplexer frame sync signal DFS is generated and applied as an enable signal to the channel data output shift register and to the error rate detector circuits on the ERD card. Signal DFS is also applied to the parallel sync acquisition circuits as an inhibit signal that prevents the circuits from being enabled again until frame synchronization is lost. After initial frame synchronization, the serial sync and sync maintenance circuits continue to check that one of the three stuff code patterns generated (during words 1 through 23) by the stuff code generation circuits on the GC/DM card is the same as the stuff code pattern contained in the incoming data overhead message format. When the incoming pattern does not match one of the three patterns from the GC/DM card, an out-of-synchronization state is identified and signal DFS is removed. This causes the channel data output shift register on the FS card and the error rate detector circuits on the ERD card to be inhibited. At the same time, removal of signal DFS also enables the parallel sync acquisition circuits to start another initial frame synchronization search. Assuming that the equipment and incoming signals are not in a permanent error condition, signal DFS will again be generated and maintained as long as a synchronous timing condition is present. The serial sync and sync maintenance circuits also generate demultiplexer overhead data signals DOD- (bit 0 of each word) that are applied to the ERD card. As part of the sync maintenance function, the incoming stuff command code is decoded, and negative stuff enable signal DNSE or positive stuff enable signal DPSE is produced. The absence of both signals during a minor frame period indicates the presence of the no-action condition. These signals are applied to the GC/DM and ERD cards to initiate the appropriate stuffing action. Word 29 signal DW29 and end-of-scan signals DEOS2 and DEOS2- are applied as part of the demultiplexer timing function.

5-113. SEQUENCER (SEQ) CARD.

5-114. The seq card generates the channel address, end-of-scan, and overhead DMF=PS signals that are applied to the GC/DM card for timing purposes. The PORT STRAPPING and PORTS IN USE switches on the card are set to the same switching configuration as that used on the seq card in the far-end multiplexer. End-of-scan timing signals generated on the seq card are also applied to the ERD and OEG cards.

5-115. The channel address generation circuits on the seq card generate 4-bit binary channel address signals DCHAD1 through DCHAD8. These signals, which are generated at the system clock rate

(DRIO), are routed to the GC/DM card. Each 4-bit channel address applied to the GC/DM card causes one gated clock signal to be generated to the channel card identified in the channel address. The end-of-scan generation circuits generate complementary end-of-scan signals DEOS and DEOS- that are applied to the OEG and ERD cards. The signals are generated when the port count in the sequencer timing circuits is equal to the maximum number of used ports selected by the five PORTS IN USE switches. Complementary end-of-scan signals DEOS2 and DEOS2- are derived from signal DEOS and the signals are applied to the FS card. In turn, complementary end-of-scan signals DEOS2B and DEOS2B- are also derived from signal DEOS. These two signals are routed to the OEG, GC/DM, and ERD cards. The overhead port sequence selector circuit produces minor frame equals port sequence signal DMF=PS during each minor frame period that is eligible to provide overhead service to an assigned used port. The signal is applied as an enable signal to the GC/DM card during word 29 to allow a positive or negative stuff to be performed. The five minor frame count signals, DMFCO through DMFC4, that are applied to the circuit from the ERD card contain the minor frame number of a given minor frame being received in the demultiplexer at any given time.

5-116. OVERHEAD ENABLE GENERATOR (OEG) CARD.

5-117. The OEG card generates timing signals that are used in the demultiplexer function. The word 24 generation circuits generate word 24 signal DW24NX when the word count in word count signals DWCO through DWC4 from the GC/DM card is count 23, and end-of-scan signal EOS is applied from the end-of-scan generation circuits. Signal DW24NX is routed to the CRC circuits on the SB card(s) as a timing signal.

5-118. The system clock distribution circuits generate system clock signals DRIO from system clock signal RI from the FS card. Signals DRIO are routed as timing signals to the seq and GC/DM cards. The end-of-scan 7eneration circuits produce end-of-scan signal DEOS3NX when word 29 signal DW29 from the GC/DM card and end-of-scan signal DEOS from the seq card are applied. Signal DEOS3NX is routed as a timing signal to the CRC circuit on the SB card(s).

5-119. GATED CLOCK/DATA MUX (GC/DM) CARD.

5-120. The GC/DM card generates the gated clock signals that are applied to the channel cards in the demultiplexer. The card also generates the three stuff command codes and timing signals that are applied to the common cards in the demultiplexer as described in the following paragraphs. The gated clock generation circuits produce gated clock signals (DGCO1 through DGC15) as required to service the active channel cards. Each active channel card has a designated gated clock signal. For example, channel card No. 1 receives signal GCO1 each time a gated clock is designated to the channel card. Positive stuff enable signal DPSE applied to the circuits during word 29 causes one additional gated clock signal to be generated to a selected channel card as part of the overhead service function. In turn, negative stuff enable signal DNSE results in deletion of one gated clock signal during word 29 to the selected channel card. Minor frame equals port sequence signal DMF=PS applied to the circuits is an enable signal that allows a positive or negative overhead service to be performed during word 29 of a given minor frame period. Signal DMF=PS is not generated during minor frame periods that are not eligible to provide overhead servicing.

5-121. The stuff code generation circuits produce the three stuff command codes that are applied to the FS card as part of the frame synchronization function. End-of-scan signal DEOS2Bfrom the seq card is a timing input to the circuits. During bit 0 of each word, one bit from each of the three stuff command codes is applied to the FS card. When the demultiplexer has frame synchronization, one of the three bits applied to the FS card will compare with the equivalent bit in the incoming overhead message format during words 1 through 23.

5-122. The word generation circuits produce word count signals DWCO through DWC4 to provide 5-bit sequential word counts 1 through 29 to the OEG card. Word signals DW28 and DW29 are also produced by the circuits. Word signals DW28 and DW29- are applied as timing signals to the ERD card and the FS card. Word signal DW29 is applied to the OEG card.

5-123. ERROR RATE DETECTOR (ERD) CARD.

5-124. The ERD card generates a timing signal and monitors the incoming serial data stream for errors to establish confidence in the BCI of the incoming data. The minor frame generation circuits produce minor frame count signals DMFCO through DMFC4 that are applied to the seq card. The minor frame identified in the signals is the same minor frame that is identified in the incoming overhead message format at any given time. Timing signals DW28, DW29-, and DEOS- are used in the generation of the minor frame count signals. Demultiplexer overhead data signals DOD-, which contain the minor frame count for the minor frame in a given overhead message during a minor frame period, are used to synchronize the minor frame generation circuits.

5-125. The error rate detector circuits receive nine bit error counts from the FS card: three that are associated with the positive stuff command codes; three that are associated with the negative stuff command codes; and three that are associated with the no-action command code. During word 28, only one set of error counts is monitored by the circuits. The set of three error counts monitored is selected by positive and negative stuff command code signals DNSE and DPSE from the FS card. When signal DNSE is applied, the error rate detector circuits monitor the three bit error counts associated with the negative stuff command codes. The positive stuff command codes are monitored when signal DPSE is applied to the circuits. When both signals (DPSE and DNSE) are absent during a given minor frame period, the three bit error counts associated with the no-action command codes are monitored. When the number of errors identified in the error counts exceeds a predetermined threshold count within a given period of time, link error rate signal LLER is generated. Signal LLER causes the LINK ERROR RATE indicator on the front panel to light. When the number of errors detected within a given period of time decreases to a value that is less than the predetermined threshold count, signal LLER is removed and the indicator goes out.

5-126. SMOOTHING BUFFER (SB) CARD.

5-127. The SB card receives the high speed serial data in the form of synchronous data (DTIX-) from the FS card. The SB card function is basically the complement of the RCB card function performed in the far-end multiplexer. Each SB card demultiplexes one channel of data out of the high-speed serial data stream and converts the data into the original asynchronous data format (with timing) that was applied to the far-end multiplexer. This card also demultiplexes data originally processed into the far-end multiplexer by

a TE/TR card that was configured for the TE function. The original timing associated with the data processed by an RCB card is also reconstructed in the SB card.

5-128. The incoming data (DTIX-) are clocked through the data input buffer and are written into the data elastic storage register. The data input buffer, write address counter, and data elastic storage register are clocked by gated clock signals DGCO1 from the GC/DM card. The gated clock signals are applied directly to the buffer, the counter, and the storage register when the SB/URD switch is in the SB position. When the switch is in the URD position, the gated clock signals are effectively applied through the coarse rate conversion (CRC) circuits to the buffer, the counter, and the storage register. The function performed by the CRC circuits is the same as that performed by the CRC circuits in the RCB card used in the multiplexer. The write address counter is sequentially incremented by each gated clock pulse applied to it. The rate at which the write address counter is incremented is, in effect, the nominal bit rate at which the data will be processed out of the channel card. The write addresses from the write address counter enable the data bits to be written into the data elastic storage register. The read addresses that clock the data out of the data elastic storage register are generated by the read address counter. The read address counter, in turn, is incremented by the read clock pulses applied from the analog phase-locked loop (APLL) circuit.

5-129. The APLL circuit generates the read clock pulses that increment the read address counter. The read address counter, in turn, produces the read address signals that read the data bits out of the data elastic storage register. Tie APLL circuit contains a phase-locked loop configuration that effectively causes the read address count from the read address counter to track the write address count from the write address counter on a bit-for-bit basis, while maintaining a difference count of eight between the two addresses. The APLL circuit also performs a smoothing function to compensate for any abrupt changes in the data bit rate caused by the overhead stuffing function. The output clock signals from the APLL circuit are identical to the read clock signals. The output clock signals clock the data bits through the data output buffer to the data output drivers. The output clock signals also clock the timing output drivers to produce the complementary demultiplexer timing out signals TOXX and TOXX-. The data bits applied to the data output drivers are conditioned and processed into complementary demultiplexer channel data output signals DOXX and DOXX-.

5-130. NARROW BAND SMOOTHING BUFFER (NBSB) CARD.

5-131. The NBSB card is identical to the SB card described in paragraphs 5-126 through 5-129. The APLL circuit on the NBSB card is physically different, but performs the same functions as those described for the APLL circuit on the SB card. The APLL circuit on the NBSB card is configured to provide a greater smoothing action that occurs over a longer period of time as described in the detailed theory of operation for the NBSB card. The NBSB card has a narrower range of frequencies that it can process as compared to the SB card.

5-132. TRANSITION DECODER (TD) CARD.

5-133. The TD card receives the high-speed serial data in the form of synchronous data (DTIX-) from the FS card. The TD card function is basically the complement of the TE card function performed on the TE/TR card in the multiplexer. Functionally, the TD card demultiplexes one channel of data out

of the high-speed serial data stream and converts the data into the original asynchronous data format (without timing) that was applied to the far-end multiplexer.

5-134. The write and read function for writing and reading data bits into and out of the data elastic storage register is the same as that described for the SB card. The data out of the register are arranged in a series of 3bit transition codes. These codes are applied to the transition decoder, which produces one pulse transition for each 3-bit code applied to it. The result is a series of reconstructed data pulses that are clocked through the data output buffer to the data output drivers. The pulses applied to the data output drivers are conditioned and processed into complementary demultiplexer channel data output signals DOXX and DOXX-.

5-135. VOICE DECODER (VD) CARD.

5-136. The VD card receives the high-speed serial data in the form of synchronous data (DTIX-) from the FS card. The VD card function is basically the complement of the VE card function in the multiplexer. Functionally, the VD card demultiplexes one channel of digitized voice data out of the high-speed serial data stream, converts these data into analog signals, and filters the reconstructed analog signals into the original voice waveforms applied to the far-end multiplexer input channel.

5-137. The incoming digital data bits are applied through a shift register to the digital-to-analog (D/A) conversion circuits. The analog signals from the D/A conversion circuits are applied through a bandpass filter circuit to the output amplifier-drivers. The signals are amplified through the output amplifier-drivers to produce data output signals DOXX and DOXX-

5-138. OVERALL DIAGNOSTIC FUNCTIONAL BLOCK DIAGRAM.

5-139. GENERAL.

5-140. The diagnostic circuits in the multiplexer set monitor the equipment for error conditions. When an error is detected, a visual display on the front panel indicates the existence and source of the malfunction. On the front panel, the malfunction source is identified as either a faulty input signal to the multiplexer set or as a failed subassembly within the equipment. The diagnostic circuits also generate electrical error signals (remote alarms) representative of the front panel indications. The remote alarm signals are routed to one multipin connector on the rear panel, where the signals can be remoted to other equipment.

5-141. Each plug-in card type in the multiplexer set contains diagnostic error detection circuits that continually generate one or more error or no-error status signals to the display card. The display card, in turn, generates signals that enable the indicators on the front panel when an error condition is detected. An error status signal from the diagnostic circuit in the power supply is routed directly to a diagnostic circuit on the front panel. The remote alarm signals are generated by the display card, the ERD card, and the front panel.

5-142. The functional diagnostic circuits on the display card contain priority encoding circuits that establish an order of priority when more than one error condition is simultaneously applied to the display card. It is possible that some of the circuits being monitored in the multiplexer set may produce a false error condition as a result of faulty signal inputs from the true error source.

Therefore, the priority encoding circuits are configured to select the probable error source and inhibit the other error conditions that may be generated. The priority assigned to each of the diagnostic error inputs to the display card is described in the display card discussion in paragraph 5-568.

5-143. The overall diagnostic functional block diagram discussion is divided into two paragraphs: paragraphs 5-144 through 5-153 contain a general block diagram discussion of the overall diagnostic circuit functions in the multiplexer set and paragraphs 5-154 through 5-163 contain a detailed block diagram discussion of the control and indicator functions on the front panel. The following discussions are associated with the overall diagnostic block diagram in figure 5-10

5-144. SYSTEM BLOCK DIAGRAM DISCUSSION

5-145. In the multiplexer function, two diagnostic error signals from each of the four common cards are applied to the display card. Each channel card in the configuration generates a diagnostic error status signal that is transmitted on the positive stuff request line (MPSTXX) to the OEG card during word 24. The OEG card, in turn, multiplexes the applied signals (MPSTXX) into one serial positive stuff acknowledge signal (MPSA) that is applied to the display card. On the display card, each of the signals that make up MIPSA is monitored for an error or no-error condition. Each RCB and TE/TR card in a configuration also generates diagnostic out-of-tolerance signal OOTXX that is applied to the display card. A VE card does not generate signal OOTXX-, but does generate a diagnostic error status in signal MPSTXX to the OEG card.

5-146. When multiplexer loss-of-timing signal MLOT- is applied from the RT card to the display card, signal LMTIM is generated and applied to the front panel to light the LOSS OF MUX TIMING indicator. Signal MLOT indicates that the system timing from an external source to the multiplexer set is faulty. Therefore, the signal does not represent a local card error and no card address is displayed on the FAULT LOCATION numerical display on the front panel.

5-147. When a diagnostic error signal MRT-, MLEOS-, MSEQ-, MDM-, MGC-, or MTMOG-, which represents a common card error condition, is generated and applied to the display card, mux card error signal LMCRD is generated and applied to the front panel to light the MULTIPLEXER CARD indicator. An error condition, representing a channel card, in signal MPSA also causes the MULTIPLEXER CARD indicator to light. The display card also generates the faulty card address associated with the diagnostic error signal. The card address consists of tens address signals TAO and TA1 that contain the tens digit 0, 1, or 2, and unit address signals UAO, UA1, UA2, and UA3 that contain the units digit that is between 0 aid 9 The signals are decoded on the front panel to produce the proper card location (between 1 and 22) displayed on the FAULT LOCATION numerical display. 5-148. When out-of-tolerance signal OOTXX from an RCB or a TE/TR channel card is in the error state, the display card generates signal IMOOT that lights the MULTIPLEXER OUT OF TOL indicator on the front panel. The card address associated with the applied signal is also generated and applied to the front panel from the display card to produce the appropriate card location on the FAULT LOCATION numerical display.

5-149. In the demultiplexer function, 11 diagnostic error signal inputs are generated from the common cards and applied to the display card. Card error signal DPSTXX from each channel card in

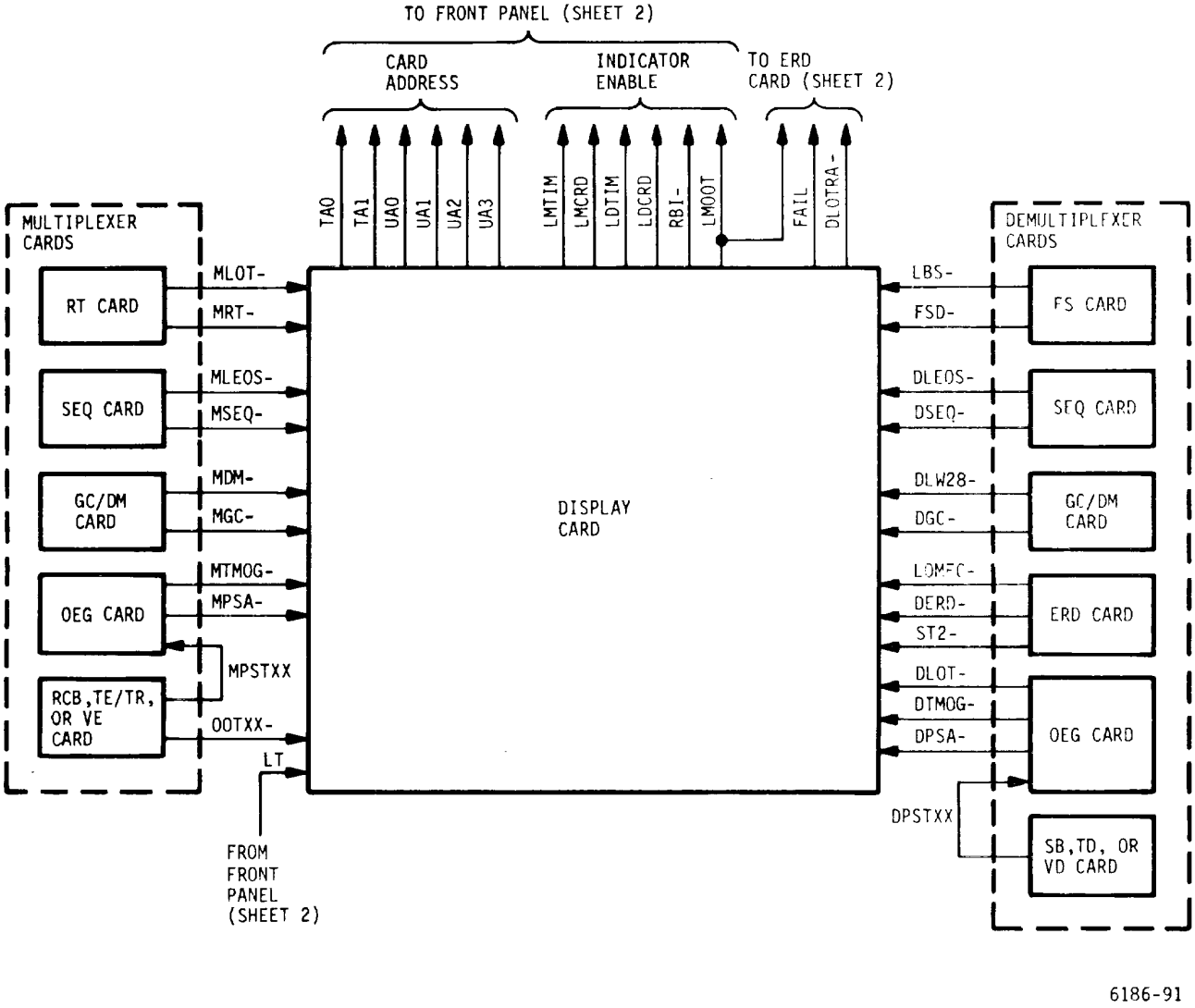


Figure 5-10. Diagnostic Overall System - Block Diagram (sheet 1 of 2)

the configuration is applied to the OEG card, which, in turn, multiplexes the error signals into one positive stuff error signal that is applied to the display card as signal DPSA-. 5-150. When demultiplexer loss-of-timing signal DLOT is generated from the OEG card to the display card, the display card, in turn, generates signal LDTIM that lights the LOSS OF DEMUX TIMING indicator on the front panel. Signal LDTIM indicates that the system timing from an external source to the demultiplexer is missing. The signal does not represent a local card error, and therefore no card address is displayed on the FAULT LOCATION numerical display on the front panel. 5-151. When diagnostic error signal LBS-, FSD-, DLEOS-, DSEQ-, DLW28-, DGC-, LOMFC-, DERD-, DTMOG-, or DPSA from one of the common cards indicates

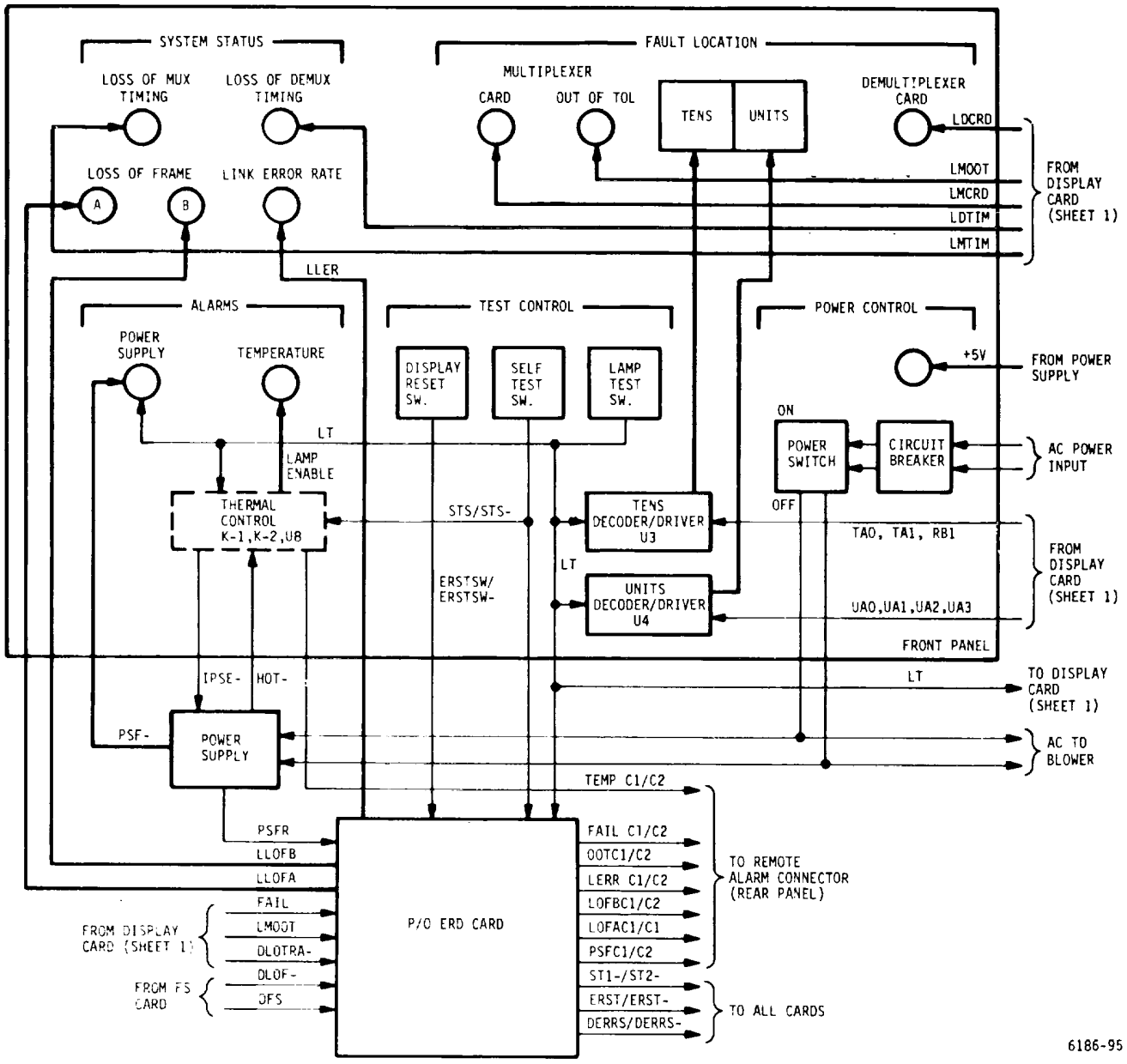


Figure 5-10. Diagnostic Overall System - Block Diagram (sheet 2 of 2)

an error condition, the display card generates demux card error signal LDCRD that lights the DEMULTIPLEXER CARD indicator on the front panel. The appropriate card address is generated on the display card and applied to the front panel to produce the card address in the FAULT LOCATION numerical display on the front panel.

5-152. Signals FAIL, DLOTRA-, and LMOOT are applied to the ERD card to develop three remote alarm signals as described in paragraph 5-163. Card failure signal FAIL is generated each time a faulty card condition in the multiplexer set is detected and a card address is applied to the front panel. Loss of timing remote alarm signal DLOTRA is generated each time signal DLOT indicates an error condition as described in paragraph 5-150. Mux out of tolerance signal LMOOT is generated from the display card as described in paragraph 5-148.

5-153. The diagnostic circuits on the ERD card generate six remote alarm signals that are routed to the remote alarm connector on the rear panel. Self-test signals ST1and ST2are applied to the cards in the multiplexer set, and signals LLOFA, LLOFB, and LLER are applied to the front panel. These signals are described as follows:

a. Self-test switch signal STS is applied to the ERD card when the SELF TEST switch on the front panel is set to the on (up) position. Signal STS enables the ERD card to generate identical self-test signals ST1and ST2that are applied to the cards in the multiplexer set.

b. Loss of frame A signal LLOFA is generated and applied to the front panel to light the LOSS OF FRAME A indicator when signal DFS is applied to the ERD card. Remote loss of Frame A signals LOFAC1/C2 are generated from the ERD card at this time.

c. LOSS OF FRAME B signal LLOFB is generated and applied to the front panel to light the LOSS OF FRAME B indicator when signal DLOF is applied to the ERD card. Remote LOSS OF FRAME B signals LOFBC1/C2 are generated from the ERD card at this time.

d. The diagnostic circuits on the ERD card generate link error rate signal LLER to light the LINK ERROR RATE indicator on the front panel when a link error condition is decoded in the ERD card. Remote link error rate signals LLERC1/C2 are generated from the ERD card at this time.

e. Remote out-of-tolerance signals OOTCl/C2 are generated when out-of tolerance signal MLOOT is applied to the ERD card from the display card. Card failure signals FAILCl/C2 are generated from the ERD card when the FAIL signal is applied from the display card.

f. Remote power supply fail signals PSFC1/C2 are generated from the ERD card when power supply error signal PSFR is applied from the power supply.

5-154. FRONT PANEL BLOCK DIAGRAM DISCUSSION.

5-155. The front panel diagnostic **in**dicators visually display the diagnostic error conditions detected in the multiplexer set. The diagnostic indicators are mounted on the front panel within three groups identified as follows: SYSTEM STATUS, FAULT LOCATION, and ALARMS. One of the SYSTEM STATUS indicators lights when one of the signal inputs to the multiplexer set is faulty. One of the FAULT LOCATION indicators lights and a card address is displayed when one of the cards in the multiplexer set is in an error condition. The POWER SUPPLY indicator in the ALARMS group lights when a power supply error condition is

detected. The TEMPERATURE indicator in the ALARMS group lights when an overtemperature condition is detected in the power supply. Three switches in the TEST CONTROL group and the POWER CONTROL switch are also mounted on the front panel.

5-156. When the POWER CONTROL switch is set to ON, ac power is applied to the power supply and to the blower fan in the multiplexer set. The POWER CONTROL ON indicator lights when the power supply is on. The incoming ac power is applied through a circuit breaker and the POWER CONTROL switch.

5-157. High-level signals LDCRD, LMOOT, LMCDR, LDTIM, and LMTIM are the enable signals from the display card that light the DEMULTIPLEXER CARD, MULTIPLEXER OUT OF TOL, MULTIPLEXER CARD, LOSS OF DEMUX TIMING, and LOSS OF MUX TIMING indicators on the front panel as shown in figure 5-10. The LOSS OF FRAME A and LOSS OF FRAME B indicators are enabled by signals LLOFA and LLOFB from the ERD card. The LINK ERROR RATE indicator is enabled by signal LLER from the ERD card. The error conditions that the indicators represent are listed in table 4-1.

5-158. The card location of a faulty card is presented on the FAULT LOCATION numerical display on the front panel. The card address for the faulty card is contained in signals TA0 and TA1 that contain the tens count 0, 1, or 2, and signals UAO, UA1, UA2, and UA3 that contain the units digit that is between 0 and 9. The incoming card address signals from the display card are applied to 7-segment decoder/driver logic circuits, which produce the outputs that enable the appropriate numerical readout from the units and tens numerical display.

5-159. Overtemperature signal HOT-generated and applied to the thermal control circuit on the front panel when an overheating condition occurs in the power supply. When the signal is applied to the thermal control circuit inhibit power supply signal IPSE is generated to turn off the power supply. At the same time, the thermal control circuit generates a lamp enable signal that lights the TEMPERATURE indicator on the front panel and generates remote temperature signals (TEMPC1/C2) that are applied to the rear panel.

5-160. When the LAMP TEST switch is pressed during normal operation, all the indicators on the front panel light. The lamp test function does not affect the operation of the functional circuits in the multiplexer set. When the LAMP TEST switch is pressed, lamp test signal LT is generated and the signal initiates the following functions:

a. The POWER SUPPLY indicator lights.

b. The thermal control circuit lights the TEMPERATURE indicator.

c. The two 7-segment decoder/ drivers enable the FAULT LOCATION numerical display to show 88.

d. The display card generates indicator enable signals that light the LOSS OF MUX TIMING, LOSS OF DEMUX TIMING, MULTIPLEXER CARD, MULTIPLEXER OUT OF TOL, and DEMULTIPLEXER CARD indicators.

e. The ERD card generates indicator enable signals that light the LOSS OF FRAME A, LOSS OF FRAME B, and LINK ERROR RATE indicators.

When the LAMP TEST switch is released, all indicators (except the POWER CONTROL ON indicator) return to their normal off state, assuming that the multiplexer set is in a no-error condition.

5-161. When the SELF TEST switch is set to the on (up) position, all the diagnostic circuits on the cards in the multiplexer set are placed in an error condition. The self-test function does not affect the normal operation of the functional circuits in the multiplexer set. Self-test switch signal STS is generated and applied to the thermal control circuit on the front panel and to the ERD card when the SELF TEST switch is set to the on (up) position. The thermal circuit, in turn, generates the lamp enable signal that lights the TEMPERATURE indicator. The ERD card generates self-test signals ST1and ST2that are applied to the cards in the multiplexer set to place their diagnostic circuits in an error condition. When all the diagnostic circuits are in the error condition, all indicators on the front panel should light. Should one of the diagnostic circuits being tested malfunction, the associated front panel indicator will be out to identify the faulty diagnostic circuit. Signal STS is applied to the ERD card when the SELF TEST switch is set to the off (down) position. The ERD card, in turn, generates error reset (mux) signals ERST and ERST-, and error reset (demux) signals DERRS and DERRS that reset the diagnostic circuits in the multiplexer set to their normal operating (no error) condition.

5-162. When the DISPLAY RESET switch is pressed, error reset switch signal ERSTSW is applied to the ERD card. The ERD card, in turn, generates error reset signals ERST, ERST-, DERRS, and DERRS that reset the diagnostic circuits in the multiplexer set to their normal operating (no error) condition. Assuming that the multiplexer set is in a no-error condition, all front panel indicators (except the POWER CONTROL ON indicator) should be out when the DISPLAY RESET switch is pressed and released.

5-163. The ERD card contains functional demultiplexer circuits as well as system diagnostic circuits as described in this paragraph. The ERD card generates six of the seven remote alarm signals that are applied to the rear panel, the three indicator enable signals that are applied to the front panel, and the self-test and reset signals that are applied to the diagnostic circuits in the multiplexer set. The signals applied to the ERD card in the diagnostic function, together with their associated output signal functions, are listed below and are shown on the block diagram in figure 5-10.

Input Signal	Source	Output Signal/Destination
FAIL	Display Card	Remote card failure signal FAILC1/C2 to rear panel
LMOOT	Display Card	Remote out of tolerance signal OOTC1/C2 to rear panel
LERR	Internal	Remote link error rate signal LERRC1/C2 to rear panel and link error rate signal LLER to front panel

Input Signal	Source	Output Signal/Destination
DLOF and DLOTRA-	FS card and display card	Remote loss of frame B signal LOFBC1/C2 to rear panel and loss of frame B signal LLOFB to front panel
DFS	FS card	Remote loss of frame A signal LOFAC1/C2 to rear panel and loss of frame A signal LLOFA to front panel
PSFR	Power supply	Remote power supply fail signal PSFC1/C2 to rear panel
STS	Front panel	Self-test signal ST1- or ST2- to all printed circuit cards (Self-test)
STS-	Front panel	Error reset signal ERST, ERST-, DERRS, or DERRS- to all printed circuit card
LT	Front panel	Signals LLER, LLOFB, and LLOFA to front panel (lamp test)

SECTION III

MULTIPLEXER CARDS FUNCTIONAL OPERATION

5-164. INTRODUCTION.

5-165. This section contains the block diagram and detailed circuit discussion for each of the card types used in the multiplexer. The detailed circuit discussion for each card follows the associated card-level block diagram discussion. The following cards are described in this section.

Channel Cards	Paragraph
RCB card	5-166
TE/TR card	5-203
VE card	5-245

Common Cards	Paragraph
Seq card	5-265
GC/DM card	5-306
OEG card	5-351
RT card	5-373

5-166. RATE COMPARISON BUFFER (RCB) CARD.

5-167. GENERAL. The RCB card is a channel option card that may be used to service one incoming channel of data that are applied with associated timing. The asynchronous digital data-inputs are processed into TTL levels,

synchronized to the multiplexer timing, and then, as synchronous data, are routed to the GC/DM card, where the digital data are multiplexed into the multiplexer output serial data stream. The block diagram discussions in paragraphs 5-168 through 5-189 are shown on figures 5-11 through 5-14. The detailed circuit discussions are based on the RCB card logic diagrams in the circuit diagrams manual.

5-168. BLOCK DIAGRAM DISCUSSION.

5-169. General. The RCB card can be operated in one of two modes. The mode of operation is selected by setting switch S3 to the URC or the RCB position. The mode of operation to which the card is programmed is determined by the relationship of the applied data bit rate as compared to the internal multiplexer timing rate in the formula $RC = KRp$

where

R_C= applied channel data rate (between 50 bps and 3 Mbps) within ±250 ppm of KRp

K = number of used ports strapped together to service an active channel

Rp = port rate at which each used port is sampled.

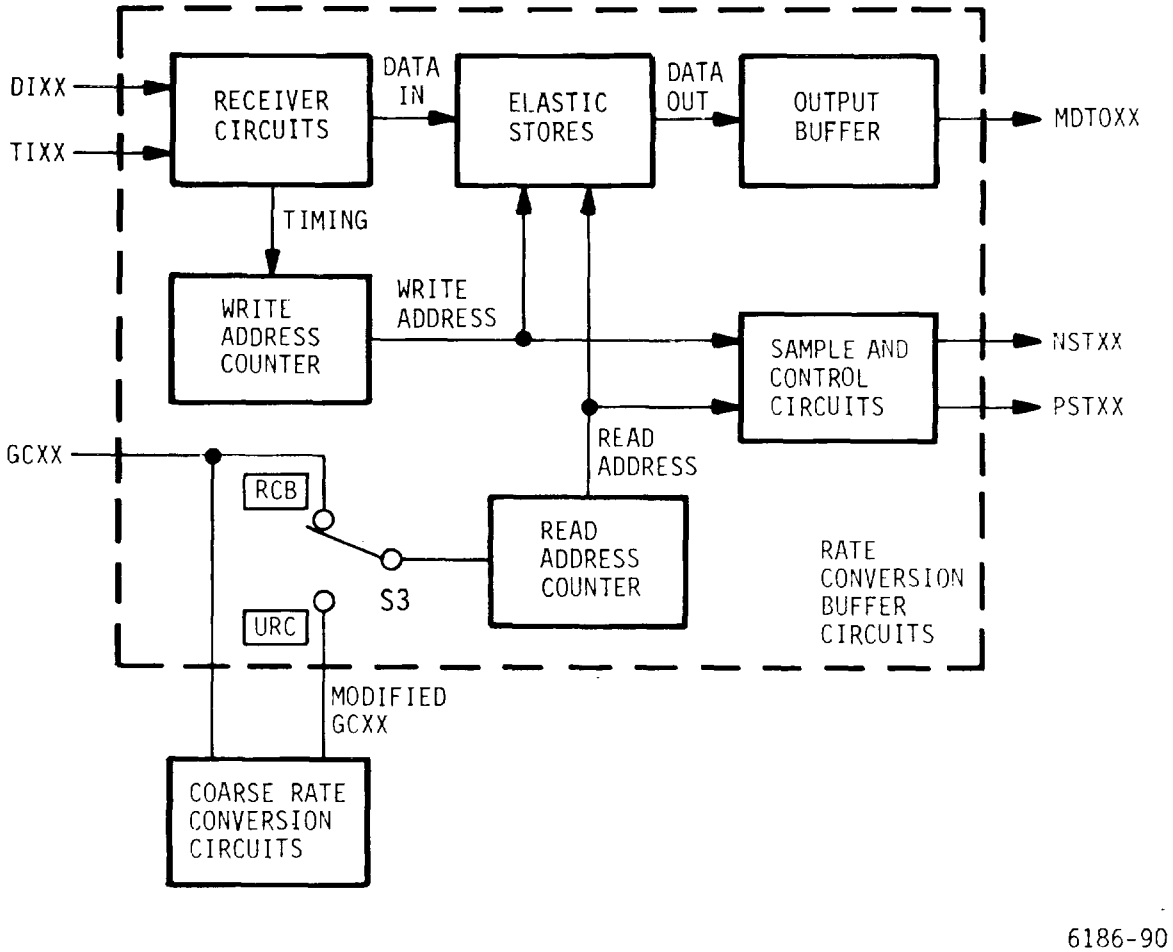


Figure 5-11. RCB Card - Simplified Block Diagram

When the input data rate meets the requirements of the formula, switch S3 is set to the RCB position and the circuits in the coarse rate conversion function are bypassed as shown in figure 5-11 and as described in paragraph 5-172. When the input data rate does not meet the requirements of the formula, switch S3 is set to the URC position. With S3 in the URC position, incoming gated clock signals GCXX are routed through the circuits in the coarse rate conversion function, where they are modified as described in paragraph 5-173.

5-170. Simplified Block Diagram Discussion (Figure 5-11).

5-171. The incoming data (DIXX) and the associated timing signals (TIXX) are applied to receiver circuits that process the digital data and timing to TTL levels that are compatible with the digital circuits on the RCB card. The conditioned timing pulses from the receiver circuits increment the write address counter, which, in turn, generates the write addresses for writing the conditioned data into the elastic stores. The data pulses read out of the elastic stores and applied to the output buffer are controlled by the read address counter, which is incremented by gated clocks (CGXX) from the GC/DM card. One gated clock is applied to the read address counter for each data bit applied to the RCB card to maintain bit integrity while the data are processed.

5-172. Switch S3 is set to the RCB position when the incoming data bit rate is within $\pm$250 ppm of KRp as explained above. In this configuration, the incoming gated clocks are applied directly to the read address counter. The number of gated clocks applied to the RCB card is controlled by the sample and control circuits that continually monitor the 4-bit address counts in the two address counters. When the sample and control circuits determine that the read address count leads or lags the write address count by more than the predetermined offset, a positive (PSTXX) or a negative (NSTXX) stuff command is generated and routed to the GC/DM card. The stuff command causes the GC/DM card to either add or delete gated clocks until the read address counter properly tracks the write address counter. When the two address counters are synchronized, a data bit is read out for each data bit that is written into the elastic storage. The stuffing of gated clocks (adding or deleting clocks) does not change the basic bit rate (KRp) at which the gated clocks are being generated. The addition or deletion of gated clocks is performed as a part of the multiplexer overhead service function.

5-173. Switch S3 is set to the URC position when the incoming data bit rate is greater than $\pm$250 ppm of KRp. In this configuration, the gated clocks from the GC/DM card are routed through the coarse rate conversion circuits and are then applied to the read address counter. A basic condition in this configuration is that the number of used ports strapped together and the port rate establish a KRp that is greater than the data bit rate being processed. In operation, the rate conversion functional circuits appear to convert the gated clock bit rate to the internal KRp sampling rate to obtain bit integrity between the asynchronous pulses applied to the elastic stores and the synchronous pulses out of the elastic stores. Actually, the coarse rate conversion is obtained by select deletion of individual gated clocks until the number of gated clocks is effectively lowered to produce the same number of clocks (KRp) that equal the incoming data bit rate (Rc). The modified gated clock bit rate from the coarse rate conversion circuits is applied to the read address counter. Any positive or negative stuff actions generated by the sample and control

circuits (fine rate adjustment) will cause the addition or deletion of gated clocks not controlled through the coarse rate conversion circuits.

5-174. Detailed Functional Block diagram Discussion (Figure 5-12).

5-175. Input-Output Data Buffer Function. The incoming channel data bits (DIXX) are applied to data receiver No. 1, where the data pulses are converted to TTL levels. The conditioned data pulses from data receiver No. 1 are applied to the data input buffer circuit. The incoming channel timing pulses (TIXX) are also converted to TTL levels. The conditioned timing pulses from timing receiver No. 1 are applied to the data input buffer, rate compare control, write address counter, initialization logic, and the diagnostic function.

5-176. The conditioned data pulses are clocked by the associated timing pulses through the data buffer and are applied serially to an elastic storage register. The elastic storage register is a

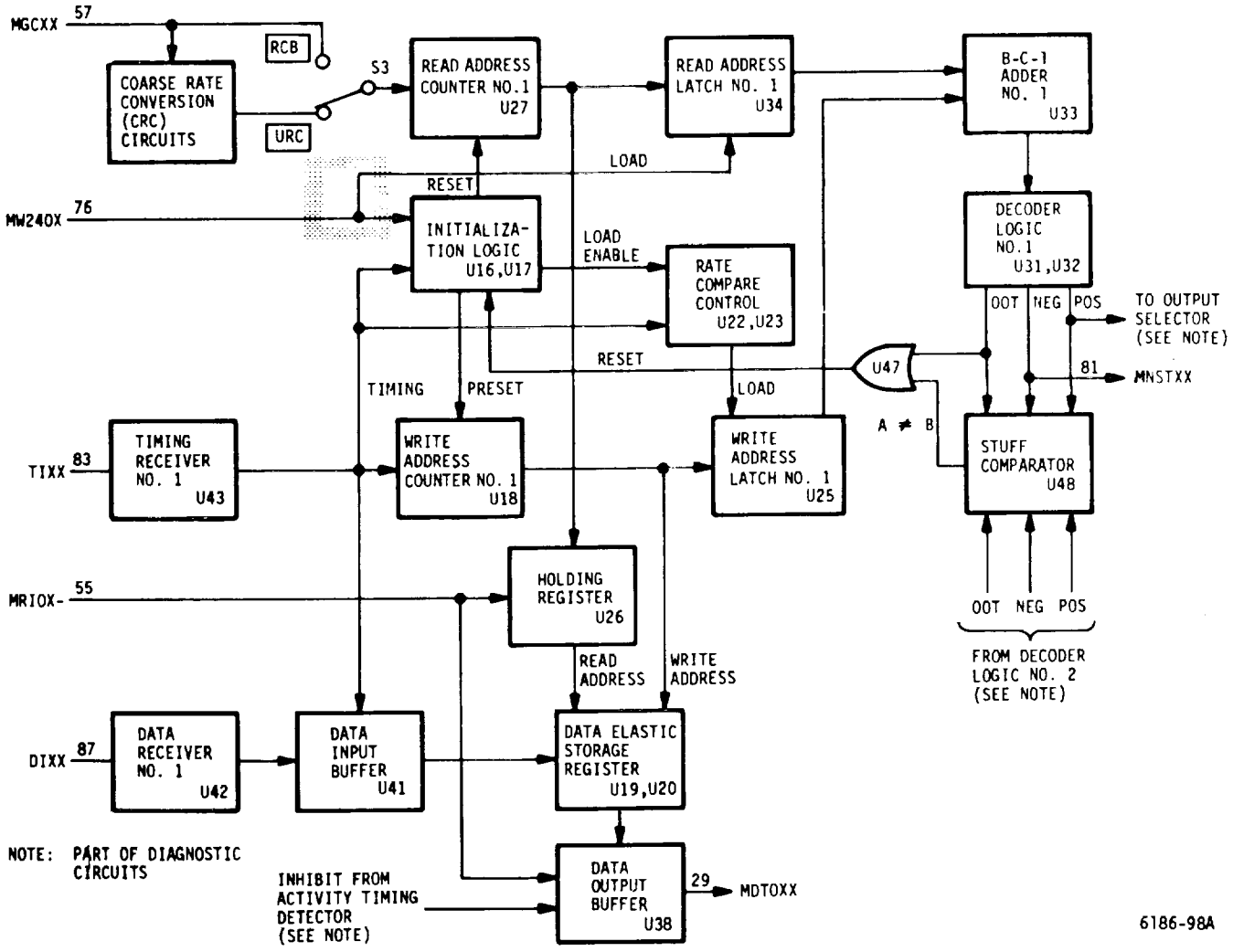


Figure 5-12. RCB Card-Block Diagram

16-port register that has the capability for data bits to be written into the register at the same time that stored data are read out (at a different address). The write address counter, which is sequentially incremented by the conditioned channel timing pulses, generates the 4-bit write addresses that are applied to the elastic storage register and the write address latch. The read address counter is sequentially incremented by the gated clock (GCXX) pulses applied through switch S3. Switch S3 selects the mode of operation as described in the simplified block diagram discussion. In the RCB position, the incoming gated clocks (GCXX) from the GC/DM card are routed directly to the read address counter. In the URC position, the gated clocks are routed through the coarse rate conversion circuits, where the gated clock bit rate is modified as described in the simplified block diagram discussion. The read address counter generates the read addresses that are applied to a holding register, and the read address latch. The read addresses are clocked out of the holding register to the elastic storage register by the multiplexer master clock signal MRIOX-. The serial data out of the elastic storage register are reclocked into the data output buffer by the system clock signal MRIOX-. The data in the buffer are sampled at a selected time by the GC/DM card.

5-177. Input-Output Data Rate Compare Function. The channel data and associated timing applied to the RCB card are asynchronous to the multiplexer timing and can vary $\pm$250 ppm from the multiplexer's nominal data rate. Any variation of the applied data rate with respect to the multiplexer's data rate is detected and compensation is initiated by this function. A rate compare is initiated when a read address is loaded into the read address latch by the load signal applied from the initialization logic to the latch during word 24 bit 0. At the same time, a load enable signal is applied from the initialization logic to the rate compare control. With the load enable signal applied, the control generates a load signal when the next timing signal from the timing receiver is applied. The load signal causes the write address latch to load in the write address from the write address counter. The load and load enable signals from the initialization circuit are inhibited if a reset signal is applied from OR gate U47. The addresses in the two latches are applied to the B-C-1 adder, where the write address count is subtracted from the read address count to provide a 4-bit count to the decoder logic. The decoder logic, in turn, decodes the adder output to determine if a stuffing action is required, an out-of-tolerance condition exists, or no action is required. The decoder logic is configured so that, during a rate compare, the offset between the write and read address is a predetermined count. Should the offset between the write address and the read address become greater than the predetermined count, a positive stuff (POS) command is decoded. If the offset between the write address and the read address is less than the predetermined count, a negative (NEG) stuff command is decoded. When the offset variation between the addresses is greater than the compensatory capability of the buffer function, an out-of-tolerance (OOT) command is decoded. When the read address is effectively tracking the write address (within tolerance), none of the three above commands are generated to indicate a no-action condition.

5-178. An out-of-tolerance (OOT) signal from the decoder logic generates a reset signal to the initialization circuit. When a reset signal is applied to the initialization circuit, the circuit generates a reset signal to the read address counter that resets the counter to a count of 0. The initialization logic also generates a preset

signal, two clock times later, to the write address counter that presets the counter to a count of 10. The preset and reset signals are generated from the initialization logic during word 24. The offset in count (normally a count of 8) between the two counters prevents them from generating identical read and write addresses to the elastic storage register at the same time. The OOT signal is also applied to the stuff comparator as described below.

5-179. A negative stuff (NEG) signal from the decoder logic is applied to the stuff comparator, and the signal is also routed as signal MNSTXX to the OEG card. The positive stuff (POS) signal from the decoder logic is also applied to the stuff comparator and is processed to the OEG card as described in the diagnostic function discussion.

5-180. The stuff comparator performs a comparison of the three outputs from the decoder logic circuits in the functional circuits with the three out puts from the decoder logic circuits in the diagnostic circuits. The three outputs from the diagnostic circuits should be duplicates of the three out puts in the functional circuit. Therefore, when the outputs do not compare, the A is not equal to B signal is applied from the stuff comparator to OR gate U47. OR gate U47, in turn, generates a reset signal to the initialization logic that resets the read and write address counters as previously described. The stuff comparator also performs diagnostic functions as described in the diagnostic circuits description.

5-181. The coarse rate conversion circuits (figure 5-13) produce modified gated clocks to the read address counter when switch S3 is set to the URC position. In normal operation, end-of-scan signal MEOS3NX increments the word counter to generate a 10-bit binary code that sequentially advances one count during each word until the end-of-scan signal in word 24 of minor frame count 31 occurs. At this time, the word counter preset control generates a preset signal that presets the word counter binary output to zero. End-of-scan signal MEOS3NX, together with word 24 MW24NX-, clocks a data bit into the 5-bit shift register so that an inhibit signal is clocked out from the register during word 29. The inhibit signal during word 29 inhibits the word counter and the gated clock control so that a gated clock cannot be deleted during word 29. Word 29 is used for the normal overhead service function. Each word count from the word counter is applied as the A input to the 10-bit comparator. Before the circuits are activated, 10 fill-bit strapping switches (O through 9) are strapped to a predetermined count that is related to the number of gated clocks to be deleted during a major frame. The 10-bit binary code from the strapping switches is applied as the B input to the 10-bit comparator. The 10-bit comparator continually compares the 10-bit binary code (A) from the word counter with the programmed 10-bit binary code applied from the fill-bit strapping switches. Each time that a binary code applied as the A input is greater than the programmed B input, the gated clock inhibit signal is generated and applied to the gated clock control logic. In a straight binary code comparison, the gated clocks to be deleted when A is greater than B would be grouped, thus causing deletion of an undesirable series of consecutive gated clocks. To prevent this condition, the outputs from the word counter are reversed so that the MSB of the counter is applied to the LSB of the A input to the 10-bit comparator. As a result, a homogeneous spread of the gated clock deletions is obtained by the reversed binary count function.

5-182. Detailed Diagnostic Block Diagram Discussion (Figure 5-14).

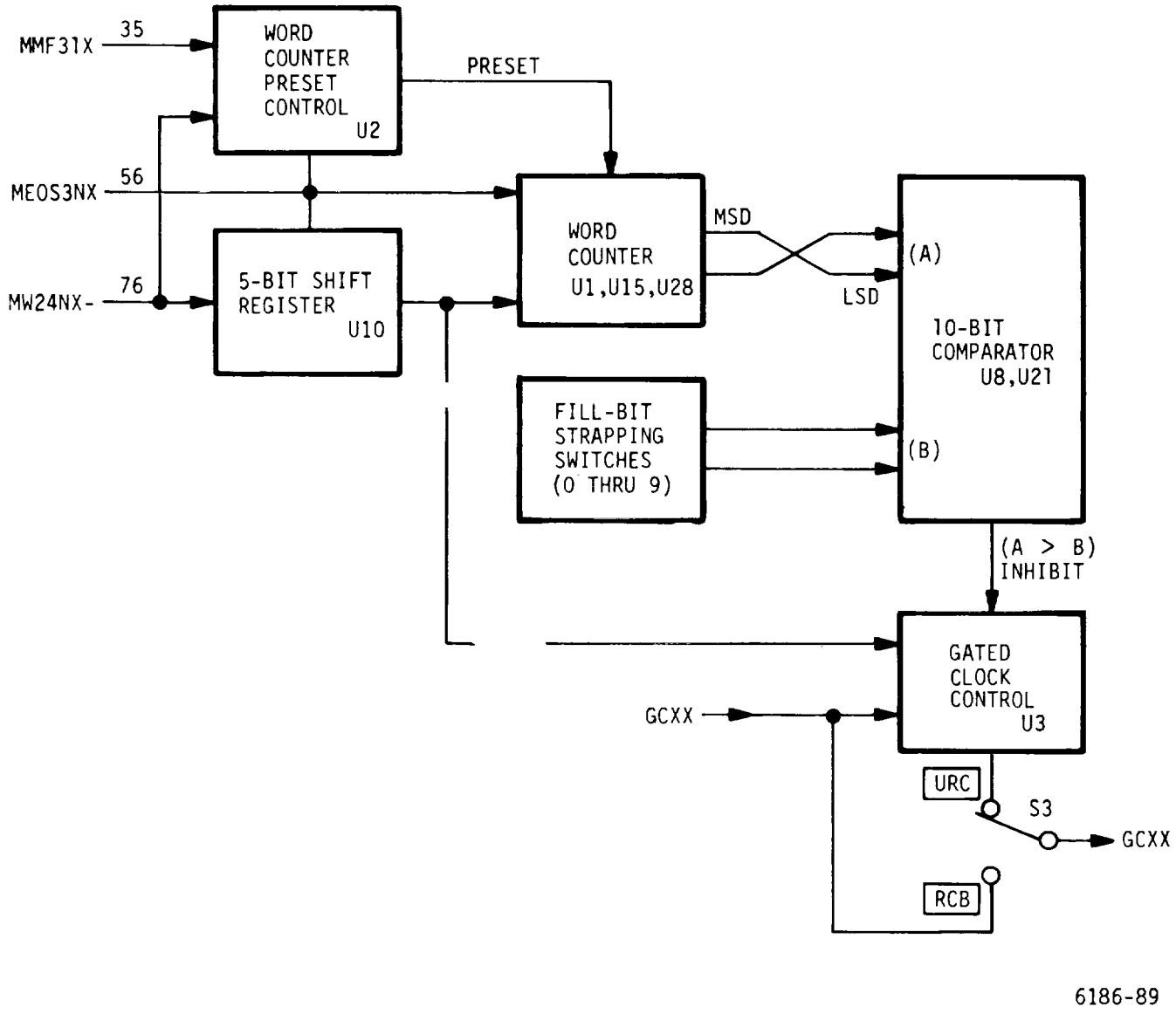


Figure 5-13. RCB Card, Coarse Rate Conversion Circuits - Block Diagram

5-183. The coarse rate activity detector is a retriggerable one-shot multivibrator that is held in conduction by bit count 512 from the word counter in the coarse rate conversion circuits. When bit count 512 is missing, the multivibrator's duty cycle expires and the coarse rate error signal is applied to the composite error detector.

5-184. The timing comparator compares the identical timing outputs of timing receiver No. 1 with those from timing receiver No. 2. When the timing signals are not the same, the output of the comparator sets the timing error latch, which, in turn, applies a timing error signal to the composite card error detector.

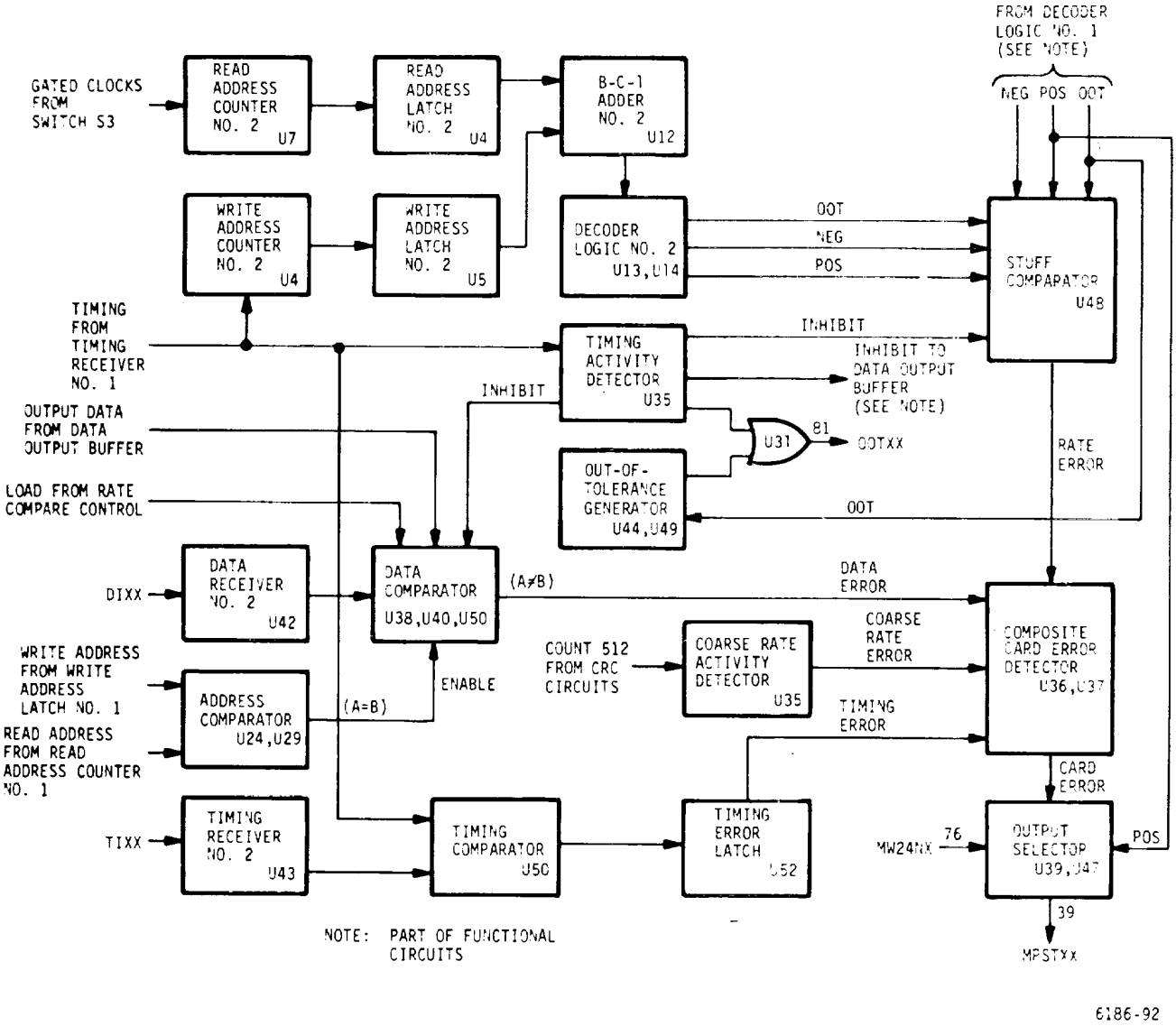


Figure 5-14. RCB Card, Diagnostic Circuits - Block Diagram

5-185. When the rate compare control circuits generate a load signal, the data bit (DIXX) from data receiver No. 2 is loaded in the data comparator, and the write address from the write address latch associated with the data bit is loaded into the address comparator. The address comparator samples the read address out of the read address counter. When the read address is the same as the write address stored in the comparator, an enable signal (A=B) is applied to the data comparator to enable the data compare function. The data bit stored in the data comparator is compared with the data bit in the data output buffer at this time. Since the read and write addresses are the same, the data bits being compared should also be

same. When the data bits are not the same, the data comparator generates the data error signal (A is not equal to B) to the composite card error detector circuit.

5-186. The timing activity detector, which is used to force the output data to all zeros when the incoming timing to the RCB card is lost, is a retriggerable one-shot multivibrator that is held in conduction by the timing signals from timing receiver No. 1. When the timing signals are missing, the multivibrator's duty cycle expires and the circuit forces the output data buffer to the zero state and also applies a high-level signal that is applied through OR gate U31 as out-of-tolerance signal OOTXX that is applied to the display card.

5-187. The out-of-tolerance generator applies a cycling out-of-tolerance signal OOTXX through OR gate U31 when the functional decoder logic circuit generates an out-of-tolerance signal. The out-of-tolerance signal from the generator is the product of a one-shot multivibrator that has a duty cycle of approximately 31 seconds.

5-188. The composite card error detector monitors the four error signals described above. When an error condition is detected, the circuit generates an error signal to the output selector.

5-189. The output selector applies the error signal from the composite error detector to the OEG card, or the selector applies positive stuff (POS) commands to the OEG card. The output selector is controlled by word 24 signal MW24MXfrom the OEG card. When signal MW24NX is applied, the selector samples the composite card error detector output and transmits signal MPSTXX when a card error is present. When signal MW24NXis not present, the selector samples the positive stuff (POS) output from decoder logic No. 1 and transmits signal MPSTXX when a stuff command is present.

5-190. DETAILED CIRCUIT DISCUSSION.

5-191. Input-Output Data Buffer Function. 5-192. The incoming channel data bits (DIXX) are applied to data receivers U42-1 and U42-8. The conditioned data pulses from data receiver No. 1 (U42-1) are applied through inverter U51 to data buffer U41. The incoming channel timing pulses (TIXX) are applied to timing receivers U43-1 and U43-8. The conditioned timing pulses from timing receiver No. 1 (U43-1) are applied through inverters U51-4 and U30-2 to increment write address counter U18. The same timing pulses that are applied through inverter U30-2 are also used to clock the data pulses through data buffer U41. The timing pulses from timing receiver No. 1 are also applied to AND gates U23-8 and U23-11 to clock the data from data buffer U41 into U19 or U20 of the data elastic storage register.

5-193. The write address counter (U18) is incremented by the same timing signal that is applied to data buffer U41. The low level MSB of the 4-bit write address from U18-11 is applied through inverter U30-12 to enable AND gate U23-8 for binary addresses 0 through 7. In turn, the high-level MSB of the 4-bit address from U18-11 enables AND gate U23-11 for binary counts 8 through 15. Therefore, the first eight bits of data clocked through data buffer U41 are stored in U20 and the next eight bits of data are stored in U19. Write address counter U18 continues to cycle until a preset signal from J-K flip-flop U16-7 in the initialization logic circuits presets its output to 1010.

5-194. The gated clocks (MGCXX) from the GC/DM card are applied through inverter U53-6 to AND gate U9. AND gate

U9 is held in an enabled state when switch S3 is strapped in the RCB configuration. When switch S3 is strapped in the URC configuration, AND gate U9 is enabled or inhibited by the output from AND gate U36 in the coarse rate conversion circuits. The gated clocks applied through AND gate U9 increment read address counter U27. The 4-bit address from U27 is applied to holding register U26. The register, in turn, applies a 3--bit address to the read address inputs of elastic storage registers U19 and U20. The data bits read out of U19 and U20 are each applied to dual AND-OR gate U39. Inverter U30-6 enables one AND gate of U39 so that data are read out of register U20 for bits 0 through 7 and are read out of register U19 for bits 8 through 15. Multiplexer system clock signal MRIOX clocks the address out of holding register U26 and through output data buffer U38-6 to the OEG card. For each data bit applied through data receiver U42-1, one equivalent data bit is clocked out of output data buffer U38-6.

5-195. Input-Output Data Rate Compare Function.

5-196. In the initialization circuit, J-K flip-flop U16-10 normally has a low-level signal applied to the J-K inputs so that AND gate U17-6 has an enable input and AND gate U17-8 has an inhibit input. This condition causes a rate compare function to be initiated when word 24 bit 0 (signal MW240X-) is applied through inverter Ull-8 to AND gate U17-6. The high level signal from Ull-8 is applied to read address latch U34 so that the output from read address counter U27 is latched in U34 at word 24 bit 0 (signal MW240X). The low-level signal from U17-6 sets latch U23-3 in the rate compare control circuit. The next timing signal (TIXX) applied through inverter U30-2 increments write address counter U18, clocks J-K flip-flop U22-9, and enables AND gate U13-4. The total effect is that write address latch U25 is enabled at word 24 bit 1. For example, at word 24 bit 0, if the read address counter output to the read address latch is 0000, the write address counter output should be 1000. Therefore, at word 24 bit 1, the read address latch remains at 0000 and the write address latch is enabled to accept the write address counter output of 1001. The Q outputs from read address latch U34 are applied to the B inputs of B-C-1 adder U33 and the Q (complementary) outputs from write address latch U25 are applied to the C inputs of the B-C-1 adder. Therefore, the B inputs to U33 are 0000 and the C inputs to U33 are 0110. The total implementation conforms to algorithm B-C-2. The 4-bit output from B-C-1 adder U33 is decoded by AND gates U31 and U32 to determine if the address relationships require a positive stuff, negative stuff, or an out-of-tolerance condition. A positive stuff condition is a high-level output from AND gate U32-11, a negative stuff condition is a high-level output from AND gate U32-3, and an out-of-tolerance condition is a high-level output from AND gate U31-10. The 4-bit binary codes generated by the B-C-1 adder, together with the resulting decodes, are listed below.

5-197. The three outputs from the decoder logic are applied to the stuff comparator U48 as part of the diagnostic function. A high-level positive stuff output from AND gate U32-11 is applied to one of the AND gates in AND-OR gate U39 and is transmitted as signal MPSTXX through the OR gate in U39 when word 24 signal MW24NX is also applied to the AND gate in U39. A high-level negative stuff output from AND gate U32-3 is applied through inverter U30-8 as signal MNSTXX-. Signal MNSTXX or MPSTXX is applied to the OEG card for processing when a stuff command is generated. High-level

Adder U33 Output E1	E2	E3	E4	Positive Stuff	Negative Stuff	Out of Tolerance
0	0	0	0	H	L	L
1	0	0	0	H	L	L
0	1	0	0	H Positive Stuff	L	L
1	1	0	0	H	L	L
0	0	1	0	H	L	L
1	0	1	0	H*	H*	L
0	1	1	0	H*	H*	L
1	1	1	0	H*	H*	L
0	0	0	1	L	H	L
1	0	0	1	L	H	L
0	1	0	1	L	H Negative Stuff	L
1	1	0	1	L	H	L
0	0	1	1	L	H	L
1	0	1	1	H	H	H
0	1	1	1	H	H	H OOT
1	1	1	1	H	H	H

* No action

out-of-tolerance signal OOT from U31-10 is applied through inverter U46-10 to OR gate U47-8 and to J-K flip-flop U49-7. The low-level output from OR gate U47-8 is applied as a reset signal to the initialization logic. J-K flip-flop U49-7, in turn, triggers one-shot multivibrator U44 into conduction to generate a low-level out-of-tolerance signal from OR gate U31-4.

5-I98. Coarse Rate Conversion Circuits. Flip-flop U2-10 in the word counter preset control toggles and a high input is applied to the J input of flip-flop U2-7 when word 24 signal MW24NXand end-of-scan signal MEOS3NX occur at the same time and minor frame terminal count signal MMF31Xis applied through inverter U53-10 to U2-10. When the next signal MEOS3NX occurs, the Q output from flip-flop U2-7 goes low and presets the outputs of word counter U1, U28, and U15 to zero. When the next signal MEOS3NX occurs, the Q output from U2-7 goes high and enables the

word counter to start counting at the beginning of the next major frame. The word counter is incremented one count each time signal MEOS3NX is generated and applied through inverters U53-2 and U53-4 to the CP inputs of U28, U1, and U15. Before the circuits are activated, 10 fill-bit strapping switches (0 through 9) are strapped to a predetermined count that determines the number of gated clock pulses to be deleted during each major frame period. The 10-bit binary code from the fill-bit switches is applied to the B inputs of 10-bit comparator U21, U8. The 10 outputs from the word counter are applied in reverse sequence to the A inputs of the 10-bit comparator. This reverse sequence is performed to obtain a near-homogeneous output from the 10-bit comparator. Each time the reversed binary numbers applied to the A inputs of the comparator are less than the programmed binary numbers applied to the B inputs, a gated clock inhibit signal is generated. Therefore, the gated clock inhibit signals from the comparator result in near-homogeneous low-level inhibit inputs to AND gate U9-11. The result is gated clock inhibit signals that occur (spread out) in a near-homogeneous sequence during each major frame period. Signals MW24NX and MEOS3NXtoggle flip-flop U3-10 to set a one in shift register U10 during word 25. This causes U10 to generate an inhibit signal during word 29 (count 5) that inhibits the word counter and AND gate U36-6, thus preventing generation of a gated clock inhibit signal from being applied to AND gate U9-11 during word 29. Activity detector U35-10 is held in conduction by count 512 from the word counter when $_{Ro}$ is greater than 2 kbps. When $_{Ro}$ is less than 2 kbps, signal MEOS3NX holds U35-10 in conduction. A missing input causes the duty cycle of U35-10 to expire and generate an error signal to OR gate U36-8.

5-199. Diagnostic Function.

5-200. Read and write address counters U4 and U7, read and write address latches U5 and U6, B-C-1 adder U12, and decoder logic U13 and U14 duplicate the rate compare functional circuits. The out-of-tolerance, positive stuff, and negative stuff signals from decoder logic U13, U14 are applied to stuff comparator U48. The output from U48 is normally a high level (A=B) signal that holds the output from J-K flip-flop U49-10 high. When the three outputs from decoder logic No. 1 and decoder logic No. 2 do not compare, the output from U48 goes low, resulting in a low-level error signal from U49-10 to OR gate U36-9 in the input circuit of the output selector circuit. An out-of-tolerance command from decoder logic No. 1 is also applied to the out-of-tolerance generator circuit consisting of J-K flip-flop U49-7 and one-shot multivibrator U44-6. The out-of-tolerance signal applied through inverter U46-10 causes U49-7 to go high and trigger U44 into conduction. Thus the low-level output (OOTXX-) from U31-4 is generated for approximately 31 seconds. The conditioned identical timing signals from timing receiver U43-8 are applied to exclusive OR gate U50-3 to exclusive OR gate U50-8. In normal operation, exclusive OR gate U50-8 generates a low-level output that is applied to inverter U46-8 and AND gate U47-6. When a malfunction occurs, the output of exclusive OR gate U50-8 goes high and enables AND gate U47-6, which, in turn, sets latch U52 that generates a low-level error signal to OR gate U36-13. The latch remains set until reset signal ERST is applied through inverters U51-8 and U51-10 to reset latch U52-6.

5-201. A diagnostic data compare function is initiated when AND gate U13-4

in the rate compare control circuit generates a load signal that is applied to write address latch U25 and to flip-flop U38 in the data compare logic. At the time that the load signal is generated, the data bit associated with the write address written into the write address latch is loaded into flip-flop U38. When the read address from the read address counter matches the write address in comparator U24, the A=B output from U24 is applied as an enable signal through J-K flip-flops U29-10, U41-10, and U40-10 to AND gate U47. At the time that AND gate U47 is enabled by flip-flop U40-10, the data bit in flip-flop U38-9 and the data bit in flip-flop U38-6 are applied to exclusive OR gate U50-11. The two data bits should be the same, therefore producing a low-level inhibit signal to AND gate U47-3. AND gate U47-3, in turn, applies a high-level signal to the K input of J-K flip-flop U40-6. J-K flip-flop U40-6, in turn, applies a high-level signal to OR gate U36-8. When there is a no compare from U50-11, a low-level signal is applied to U36-8.

5-202. Timing activity detector U35-6 is held in conduction by the timing signals (TIXX) from timing receiver No. 1. When the timing pulses are missing, the Q output from U35-6 goes low and inhibits the data bits out of flip-flop U38-6. The low-level output from U35-6 is applied through AND gate U45-3 to enable AND gate U45-11. AND gate U45-11, in turn, presets J-K flip-flop U49-10 to inhibit a low-level error signal, caused by an OOT condition, from being generated to OR gate U36-8 when stuff comparator U48 detects an error condition and tries to set flip-flop U49-10. The Q output from U35-7 is applied through OR gate U37-8 to inhibit the low-level error signal from J-K flip-flop U40-6 in the data compare function to OR gate U36-8. The high level signal from the Q output of U35-7 is also applied to OR gate U31-4 to generate an out-of-tolerance signal OOTXX to the display card. When switch S1 is in the URC position and switch position 9 of fill bit switch S2 is strapped in the 1 position (fill bit quantity is greater than 434 (refer to table 3-3)), AND gate U9-9 produces a low-level preset signal to J-K flip-flop U40-10 to inhibit the diagnostic data compare function. During self-test, the low output from AND gate U13-10 produces a low output to OR gate U37-8 that, in turn, causes J-K flip-flop U40-6 to produce an error signal.

5-203. TRANSITION ENCODER/TIMING RECOVERY (TE/TR) CARD.

5-204. GENERAL. The TE/TR card is one of the multiplexer channel cards that receives and processes incoming digital data that are applied without associated timing. The TE/TR card processes one of two types of incoming data: data with bit rates up to 400 bps using transition encoding, or data whose bit rate is 75, 150, 300, 600, 1200, 2400, 4800, or 9600 bps using timing recovery. In the following discussion, the circuits on the card are divided into three functions: timing recovery, transition encoder, and rate comparison buffer (RCB). Figure 5-15 is a simplified block diagram that shows the two operational configurations in which the three functions can be connected. The functional application of the card is selected by connecting the TE/TR strapping switches to the TE or the TR positions. Incoming data with bit rates up to 400 bps are processed by the circuits that make up the transition encoder and the RCB functions (switches strapped in the TE positions). The incoming data bit rate of 75, 150, 300, 600, 1200, 2400, 4800 or 9600 bps is processed by the circuits that make up the timing recovery and the RCB functions (switches strapped in the TR positions). The block diagram discussions are contained in paragraphs 5-205 through 5-229. Paragraphs 5-230 through 5-244 contain the detailed

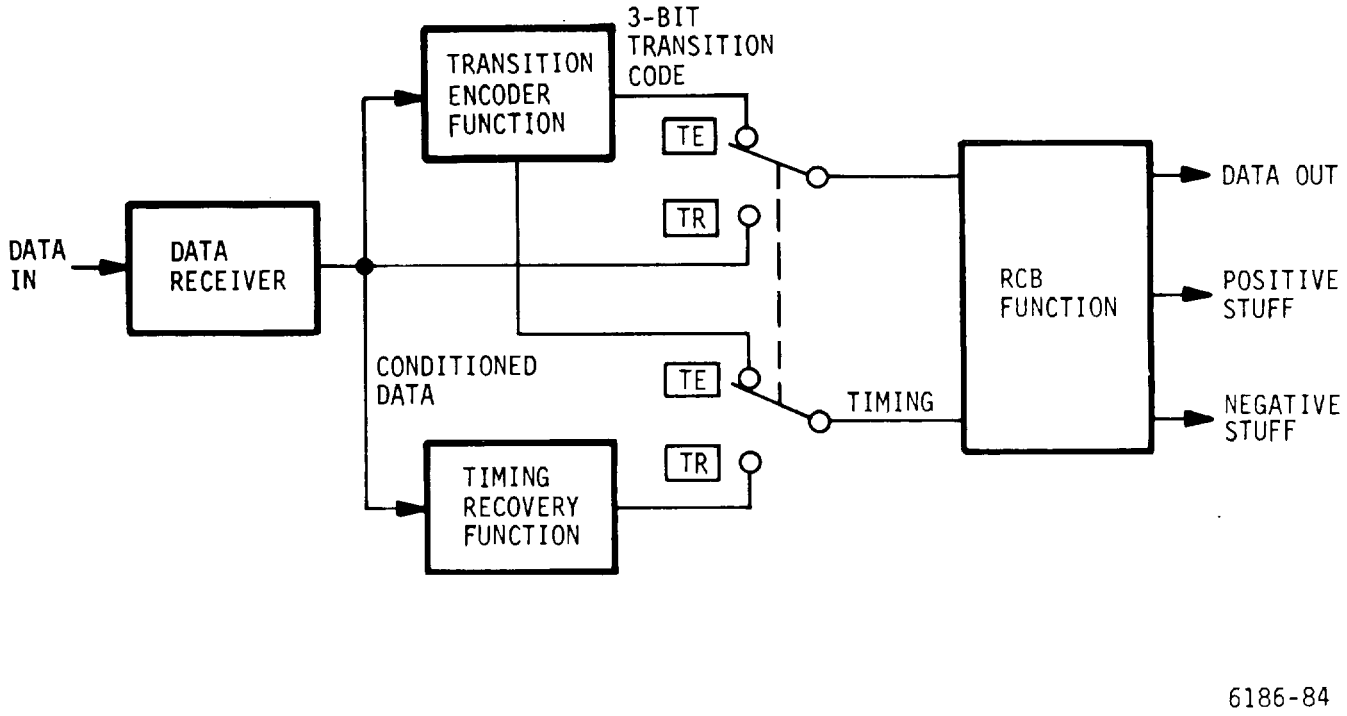


Figure 5-15. TE/TR Card - Simplified Block Diagram

theory of operation discussions based on the TE/TR card logic diagram contained in the circuit diagrams manual.

5-205. BLOCK DIAGRAM DISCUSSION.

5-206. Transition Encoder Function (Figure 5-16).

5-207. The transition encoder function receives the incoming data, without timing, that has a bit rate less than 400 bps. The data receiver circuits condition the incoming data pulses to TTL levels that are compatible with the digital circuits on the card. The transition encoder circuits then monitor for the positive-going and negative-going transitions of each incoming pulse. When a pulse transition is detected, a 3-bit transition code is generated and applied to the RCB function. The 3-bit transition code provides the following information: bit 1 indicates that a pulse transition has occurred, bit 2 identifies the transition as having occurred during the first half or the second half of an associated timing pulse, and bit 3 indicates that the pulse transition is a positive going or negative-going transition. The 3-bit code combinations are listed in table 5-1.

5-208. Initially, the TE range switch is set to the switch position that is equal to or higher than the incoming data bit rate. The switch selects one of the three bit rates from divide-by-N counter No. 1, or one of the three bit rates from divide-by-N counter No. 2 as shown in figure 5-16. Divide-by-N counter No. 1 receives the 3600-Hz timing from the reference timer card and divides the signals down to produce the 225-Hz, 450-Hz, and 900-Hz timing signals applied to the 75, 150, and 300-positions of the TE range switch. Divide-by-N counter No. 2 receives the 4800-Hz timing from the reference timer card and divides the

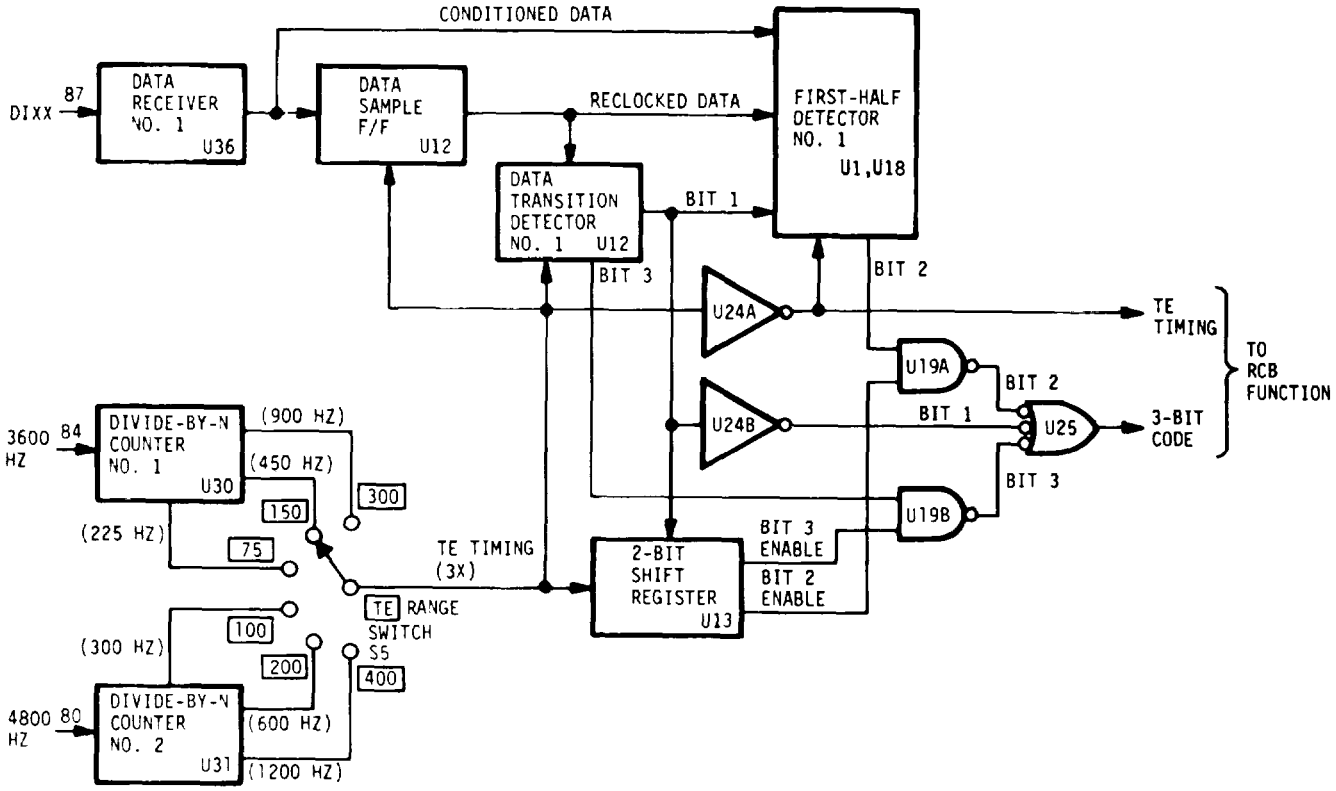


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Figure 5-16. TE/TR Card, Transition Encoder Circuits - Block Diagram

Table 5-1. 3-Bit Transition Codes

Code			Information
Bit 1	Bit 2	Bit 3	
1	1	1	Transition is positive going and occurs during first half of timing pulse.
1	1	0	Transition is negative going and occurs during first half of timing pulse
1	0	1	Transition is positive going and occurs during second half of timing pulse.
1	0	0	Transition is negative going and occurs during second half of timing pulse.

signals down to produce the 30-Hz, 600-Hz, and 1200-Hz timing signals applied to the 100, 200, and 400 positions of the TE range switch. The selected range, which is at least three times the bit rate of the data, is routed through the TE range switch and is applied to the data sample flip-flop, the data transition detector, the 2-bit shift register, and through inverter U24, to the first-half detector. The selected sampling data rate must be at least three times the input data rate, since one bit of data is coded into three bits.

5-209. The incoming data signals (DIXX) are conditioned in the data receiver and are then applied to the data sample flip-flop and the first- half detector. The data are clocked through the flip-flop by the selected TE timing signals applied through the TE range switch. The reclocked data are applied to the data transition detector and to the first-half detector. When a data transition is detected, the data transition detector generates bit 1 to signify the transition. The bit 1 pulse, synchronized with the TE timing signals, is applied through inverter U24 and OR gate U25 to the RCB function. The bit 1 signal is also applied to the first-half detector and to the 2-bit shift register. The data transition detector also determines if the transition is positive going or negative going., Bit 3 from the detector is a high-level signal when the transition is positive going or is a low-level signal when the transition is negative going. The bit 3 signal is applied to AND gate U19B.

5-210. The first-half detector determines when the data pulse transition occurs with respect to the TE timing signals. A transition of the data that occurs during the high-level portion of the timing signal is identified and coded as a first half transition. Conversely, a second half transition is defined as a transition that occurs during the low-level portion of the TE timing signal. Therefore, the first- half detector generates a high-level signal to AND gate U19A when a first- half transition occurs or a low-level signal to AND gate U19A when a second-half transition occurs.

5-211. The 2-bit shift register sequentially clocks out the enable 1 and enable 2 timing signals that are synchronized to the TE timing signals. The bit 2 enable signal from the shift register enables AND gate U19A so that bit 2 is sequentially clocked out of U19A to OR gate U25 by the next TE clock after bit 1 is clocked through OR gate U25. In turn, the bit 3 enable signal from the shift register enables AND gate U19B so that bit 3 data are sequentially clocked out of U19B to OR gate U25 by the next TE clock after bit 2 is clocked out. The 3-bit code from OR gate U25 and the TE clock signals through inverter U24A are applied to the RCB function.

5-212. Assuming that there are no further transitions of the incoming data over a given period of time, the output from OR gate U25 returns to a zero level after a 3-bit code has been generated for the last transition. The return-to-zero action is initiated when both inputs to exclusive OR gates U18-8 and U18-11 are either high or low, depending on the type of transition decoded.

5-213. Timing Recovery Function (Figure 5-17).

5-214. The timing recovery function provides synchronous timing pulses for the incoming data whose bit rate is 75, 150, 300, 600, 1200, 2400, 4800, or 9600 bps. The functional circuits maintain bit count integrity (provide the proper number of timing pulses) in excess of 100 data bits when there are no pulse transitions as a result of a continuous stream of l's or O's. The bit count integrity is based on the

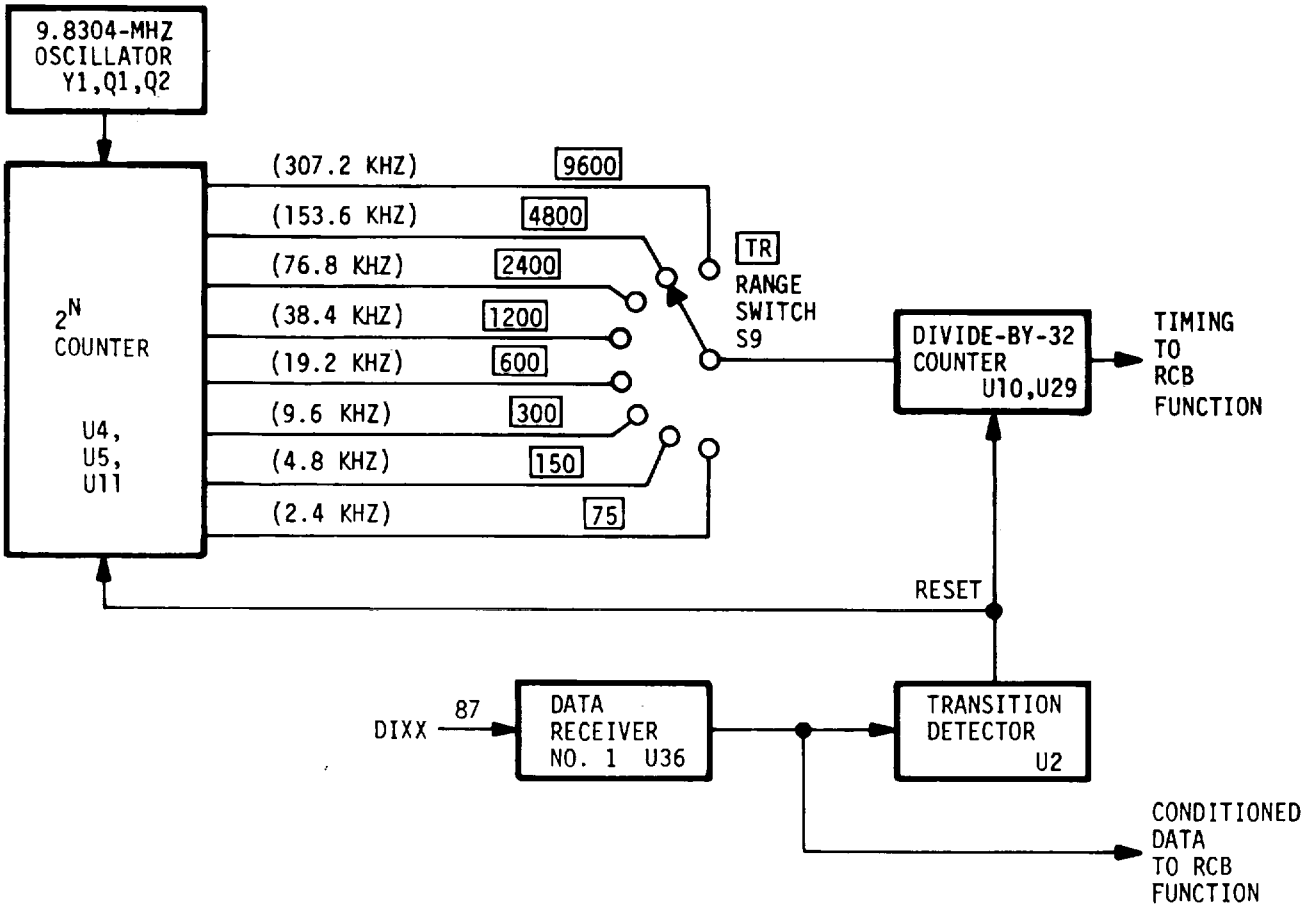

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Figure 5-17. TE/TR Card, Timing Recovery Circuits - Block Diagram

applied data bit rate variation being within ±250 ppm and the isochronous distortion of the data pulses being less than 40 percent. A decrease in data rate variation and/or isochronous distortion results in a corresponding increase in bit count integrity.

5-215. Initially, the TR range switch is set to the switch position that is equal to the incoming data bit rate. The switch selects one of the eight outputs from the 2^N counter as shown in figure 5-17. The eight outputs are developed by the counter performing a binary count down of the output from the 9.8304-MHz oscillator. The binary outputs from the 2^N counter are actually 32 times the bit rate selected. For example, the output from the counter that is applied to the divide-by-32 counter from the 300 position of the TE range switch is 9600 Hz (32 x 300). Therefore, the timing bit rate applied to the RCB function from the counter is the actual frequency selected by the TE range switch.

5-216. The incoming data pulses (DIXX) are conditioned in the data receiver and are then applied to the transition detector and to the RCB function. The transition detector, in turn, generates a reset signal to the two counters each time a positive-going or negative-going pulse transition is detected. Since the output of the counters is the same frequency as the incoming data, the MSB from the divide-by-32 counter should occur as a synchronized center sample pulse to clock the conditioned data pulse applied to the RCB function from the data receiver.

5-217. Rate Conversion Buffer (RCB) Function (Figure 5-18).

5-218. The RCB functional circuits are basically the same as those described for the RCB card. The data pulses from the TE or TR circuits are clocked through the appropriate TE or TR position of switch S3 by the associated TE or TR timing pulses. The data pulses are applied through the data buffer to the data elastic storage register.

5-219. The data elastic storage register is a 16-port register that has the capability for data bits to be written into the register at the same time that stored data are read out (at a different address). The write address counter, which is sequentially incremented

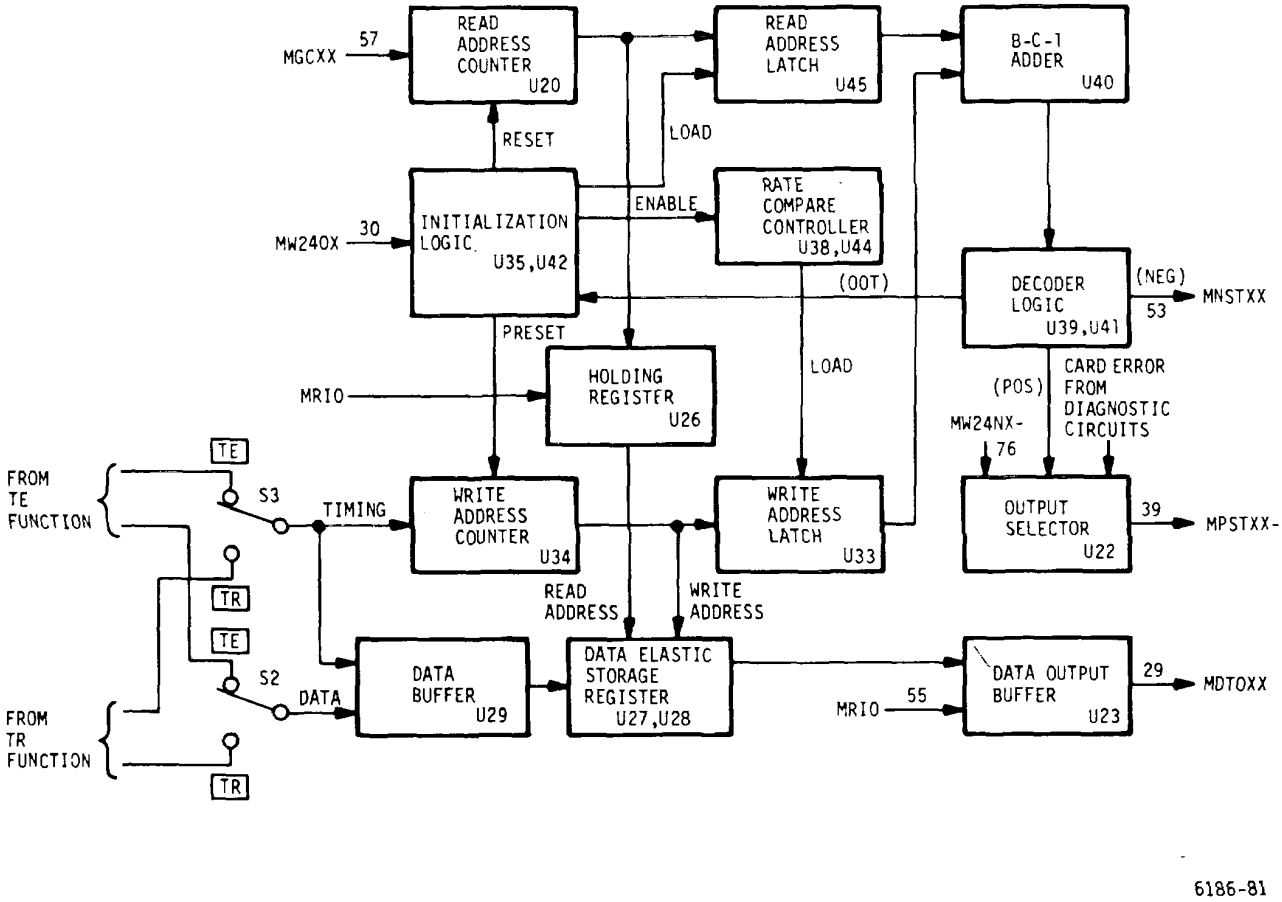


Figure 5-18. TE/TR Card, Rate Conversion Buffer Circuits - Block Diagram

by the incoming timing pulses associated with the incoming data, generates the 4-bit write addresses that are applied to the data elastic storage register and to the write address latch. The read address counter is sequentially incremented by the applied gated clock signals (MGCXX). The read address counter generates the read addresses that are applied to a holding register and to the read address latch. The read addresses are clocked out of the holding register to the elastic storage register by system clock signal MRIO. The serial data out of the data elastic storage register are reclocked into the data output buffer by the system clock signal MRIO. The data in the data output buffer are selectively sampled by the GC/DM card.

5-220. Input-Output Data Rate Compare Function. The data and associated timing applied to the RCB circuit, are asynchronous to the multiplexer timing and can vary $\pm$250 ppm from the multiplexer's nominal data rate. Any variation of the applied data rate with respect to the multiplexer's data rate is detected and compensation is initiated by this function. A rate compare is initiated when a read address is loaded into the read address latch by the load signal applied from the initialization logic to the latch during bit 0 of word 24. At the same time, a load enable signal is applied from the initialization logic to the rate compare control. With the load enable signal applied, the rate compare controller generates a load signal when the next timing signal from the timing receiver is applied. The load signal causes the write address latch to load in the write address from the write address counter. The load and load enable signals from the initialization circuit are inhibited if an OOT signal is generated by the decoder logic. The addresses in the two latches are applied to the B-C-1 adder, where the write address count is subtracted from the read address count to provide a 4-bit count to the decoder logic. The decoder logic, in turn, decodes the adder output to determine if a stuffing action is required, an out-of-tolerance condition exists, or no action is required. The decoder logic is configured so that, during a rate compare, the offset between the write and read address is a predetermined count. Should the offset between the write address and the read address become greater than the predetermined count, a positive stuff (POS) command is decoded. If the offset between the write address and the read address is less than the predetermined count, a negative (NEG) command is decoded. When the offset variation between the addresses is greater than the compensatory capability of the buffer function, an out-of-tolerance (OOT) command is decoded. When the read address is effectively tracking the write address (within tolerance), none of the above commands are generated, indicating a no-action condition.

5-221. An out-of-tolerance (OOT) signal from the decoder logic is a reset signal to the initialization logic. When the signal is applied to the initialization circuit, the circuit generates a reset signal to the read address counter and resets the counter to a count of 0. The initialization logic also generates a preset signal, two clock times later, to the write address counter and presets the counter to a count of 10. The preset and reset signals are generated from the initialization logic during word 24. The offset in count (normally a count of 8) between the two counters prevents them from generating identical read and write addresses to the elastic storage register at the same time.

5-222. A negative stuff command (NEG) applied to the decoder logic is decoded into negative stuff request signal MNSTXX- that is routed to the OEG card. In turn, a positive stuff

command (POS) applied to the decoder is decoded into a positive stuff request that is routed to the output selector. The output selector transmits a card diagnostic signal on the positive stuff request line (MPSTXX-) during word 24 as described in the diagnostic functional discussion. After word 24 occurs, the output selector produces positive stuff request signal MPSTXX- when a positive stuff (POS) output is applied to it from the decoder logic.

5-223. Diagnostic Function (Figure 5-19).

5-224. Data transition detector No. 2, first half detector No. 2, 2-bit shift register No. 2, and associated logic duplicate the 3-bit code generated by the transition encoder functional circuits. The operation of the duplicate transition encoding diagnostic circuits is the same as that described for the equivalent functional circuits. When the card uses the transition encoding circuits, the 3-bit code data from the diagnostic circuits are applied through switch S1, connected in the TE position, to the data buffer. When the card uses the timing recovery circuits, conditioned data from data receiver No.2 are applied through switch S1, connected in the TR position, to the data buffer. The data (data in) applied to the data buffer are clocked by its associated timing signals to the data comparator. The data (data out) from the data output buffer are also applied to the data comparator.

5-225. The address comparator continually compares the write address stored in the write address latch with the read address from the read counter in the RCB functional circuits. When a compare is made, the A=B output from the address comparator is applied to the data compare enable circuit.

The data compare enable circuit, in turn, generates an enable signal to the data comparator when an address compare is made and a gated clock signal MGCXX is present. The enable signal applied to the data comparator is clocked by system clock signal MRIOX.

5-226. The data comparator actually performs a random compare of one data in bit against one data out bit. Both bits being compared are from the same address and should be of the same polarity. When the bits being compared are not of the same polarity and an enable signal is applied to the data comparator, an error signal is generated and applied to the card error detector.

5-227. The enable activity detector is held in conduction by the enable signals from the data compare enable circuit. When the enable signals are missing, the detector completes its duty cycle and applies a low-level error signal to the card error detector. The timing activity detector is held in conduction by the appropriate TE or TR timing signals applied through TE/TR switch S3. When the timing signals are missing, the detector completes its duty cycle and applies a low-level error signal to the card error detector.

5-228. The data in comparator compares the conditioned data from data receivers No. 1 and No. 2. When the data do not match, a low-level error signal is applied to the card error detector.

5-229. The card error detector, in turn, generates a card error signal when any one of the four circuit error conditions is detected. The card error signal from the detector is applied to the output selector, which, in turn, generates the card error condition to the display card during word 24.

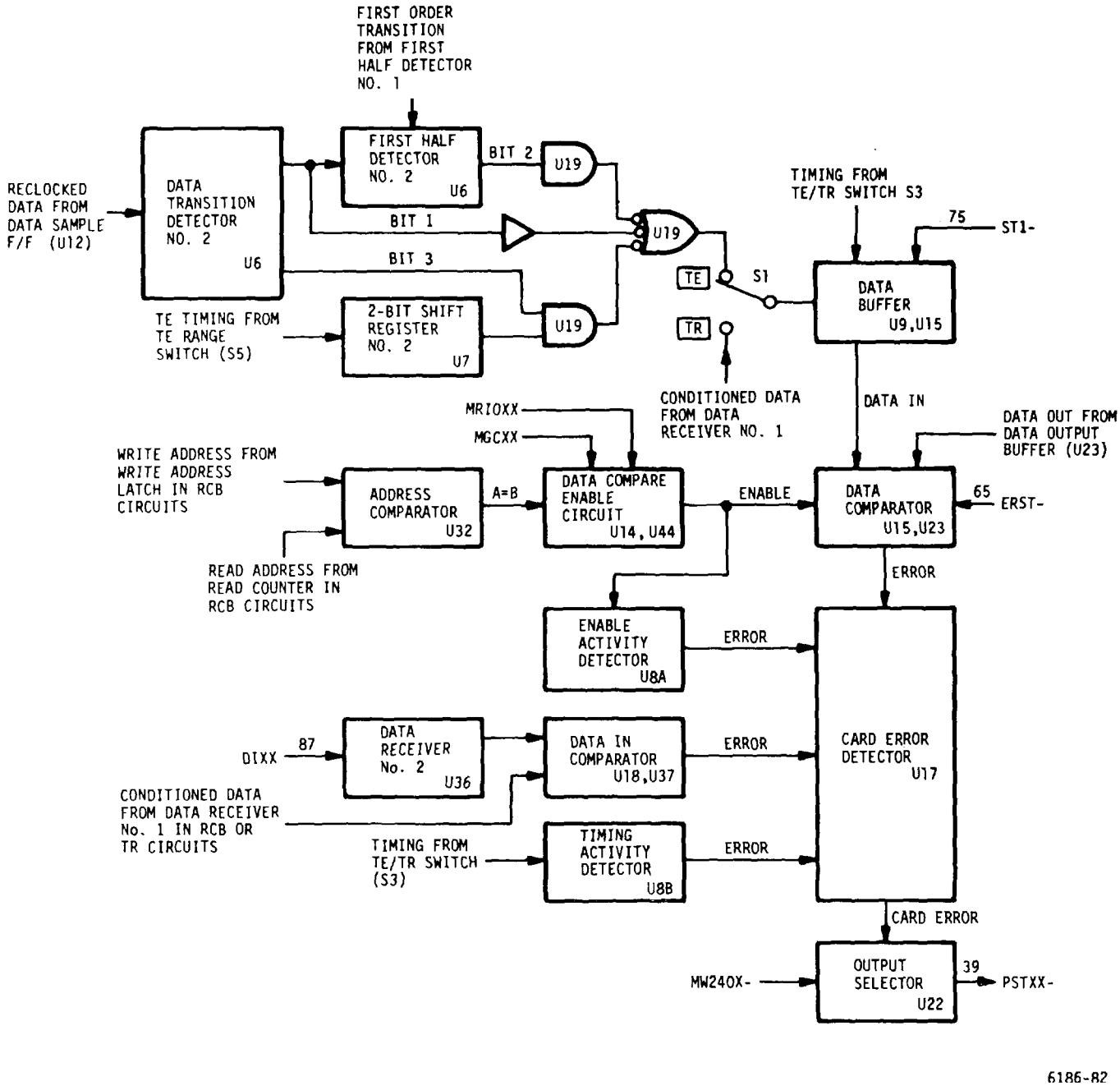


Figure 5-19. TE/TR Card, Diagnostic Circuits - Block Diagram

5-230. DETAILED CIRCUIT DISCUSSION.

5-231. Transition Encoder Function.

5-232. Divide-by-N counter No. 1, U30, is a 4-bit binary counter. The divide- by-4, -8, and -16 outputs of the counter produce the 225-Hz, 450-Hz, and 900-Hz outputs that are applied to switch positions 75, 150, and 300 of TE range switch S5. The divide-by-4, -8, and -16 outputs of divide-by-N counter No. 2, U31, produce the 300-Hz, 600-Hz, and 1200-Hz outputs that are applied to switch positions 100, 200, and 400 of TE range switch S5. The selected timing signals applied through switch S5 are applied as TE timing signals, which are actually three times the desired data bit rate, to data sample flip-flop U12. The conditioned data pulses from data receiver U36-1 are applied to exclusive OR gate U18 and J-K flip-flop U12-6. When a transition of a data pulse occurs, the output of exclusive OR gate U18-8 goes high. If the transition occurs during the first half of the TE timing signal, a high-level signal is clocked through U1-10 to U1-6. If the transition occurs during the second half of the TE timing signal, the appropriate high- level or low-level signal is clocked through J-K flip-flop U12-6. This condition places matching input levels to exclusive OR gate U18-8, resulting in a continued low-level signal being applied to J-K flip-flop U1-10. When J-K flip- flop U12-6 is clocked, exclusive OR gate U18-11 has a high output for one TE timing pulse, until J-K flip-flop U12-10 is clocked by the next TE timing signal. The high-level bit 1 pulse from exclusive OR gate U18-11 is applied to J-K flip-flop U13-6 in the 2-bit shift register. The next TE timing signal clocks the pulse through J-K flip- flop U13-6 to enable AND gate U19-8 so that bit 2 from J-K flip-flop U1-6 is applied to OR gate U25-8. If the data pulse transition occurred during the first half of the TE timing signal, the output from the AND gate is a low-level pulse. During the next TE timing signal, the output from J-K flip-flop U13-10 enables AND gate U19-11 to develop bit 3. When the transition is a positive-going signal, the output from J-k flip-flop U13-10 is positive, and therefore the output from AND gate U19-11 is low for a positive-going transition or is high for a negative-going transition. The bits 1, 2, and 3 pulses are applied sequentially in time through OR gate U25-8 to the TE position of TE/TR switch S2.

5-233. Timing Recovery Function.

5-234. The conditioned data pulses from data receiver U36-1 are applied to one-shot multivibrators U2-7 and U2-9. A positive-going or negative- going pulse applied to the two multi-vibrators triggers one of them into conduction for approximately 100 nanoseconds to develop a negative pulse that is applied through OR gate U21-3 and inverter U3-2 as a reset signal to the 2^N counter stages. The 9.8304-MHz timing signals developed by crystal controlled oscillator Q1 are applied through amplifier Q3 to the clock inputs of binary counters U4, U5, and U1l in the 2^N counter circuit. The divided down count from binary counter U4 (614.4 kHz) is applied to binary counters U5 and U11 that provide the eight selectable outputs shown in figure 5-17. The frequency range selected by TR range switch S9 is applied to binary counter U10. The divide-by-16 output of binary counter U10 is applied to J-K flip-flop U29, whose output completes a divide by 32 of the signals applied through switch S9. The counters continuously count and produce a timing signal, at the selected frequency range, between 75 bps and 9600 bps. Each time the transition detector generates a reset signal to the counters, and the timing pulse from J-K flip-flop U29-lb is

synchronous with the incoming data pulse, no apparent shift in the phase of the timing pulse in relationship to the data pulse will occur. If the timing pulse from the J-K flip-flop is slightly out of synchronization with the timing pulse transition, the resetting of the binary counters effectively shifts the timing output from J-K flip-flop U29 so that the timing pulse performs a center sample of the incoming data pulse.

5-235. Rate Conversion Buffer (RCB) Function.

5-236. The basic operation of the RCB functional circuits is basically the same as that described for the RCB card in paragraph 5-166. TE/TR switches S2 and S3 are set to receive the applied data and associated timing signals from the transition encoder or timing recovery function. The applied data through switch S2 are clocked through data buffer U29-6 to data elastic registers U27 and U28 by the timing signals applied through switch S3. The write address is applied to the data elastic registers for writing the data into the RCB function. The read address counter is clocked by gated clock pulses MGCXX from the GC/DM card and are applied through inverters U47 to the counter. The data are clocked out of the elastic registers by holding register U26, which, in turn, is clocked by system clock signal MRIOXX. The data read out of register U27 or U28 are applied through AND/OR gate circuit U22 to output data buffer J-K flip-flop U2-7. The channel data out signals (MDTOXX) are clocked out of the flip-flop by system clock signal MRIOX and are routed to the GC/DM card.

5-237. The initialization logic (U42-11) produces an enable signal that sets latch U43-11 in the rate compare control during word 24. The rate compare control, in turn, applies a load signal that latches the present write address into write address latch U33. The initialization circuit also applies a load signal that latches the present read address into read address latch U45 at the same time. The addresses in the two latch circuits are applied to B-C-1 adder U40. In turn, U40 produces an output to the decoder logic, which produces a no-action, out-of-tolerance, positive stuff, or negative stuff signal. An out-of-tolerance decode from the decoder logic results in a low- level reset signal from AND gate U39-10 that is applied to J-K flip-flop U35-10 to reset the initialization circuit. A negative stuff decode is applied from AND gate U41-8 and, through inverter U46-12 as signal MNSTXX-, to the display card. A positive stuff decode is applied from AND gate U41-11 to the output selector (AND/OR gate U22) and is transmitted as signal MPSTXX- to the display card. The output selector circuit inhibits a positive stuff signal during word 24 in each minor frame.

5-238. Diagnostics Function.

5-239. The card error detector (OR gate U17) produces a card error signal to output selector U22 when any one of four error signals is applied to it. The output selector, in turn, transmits the error signal as signal MPSTXX- when word 24 bit 0 signal MW24NX- is applied from the OEG card.

5-240. Timing activity detector U8-6 is a one-shot multivibrator that is held in conduction by the TE or TR timing signals applied through TE/TR switch S3. When the timing signals are missing, the multivibrator completes its duty cycle and applies an error signal to the card error detector.

5-241. The data-in comparator (exclusive OR gate U18-6) normally produces a low-level signal, since the conditioned data pulses from data receivers U36-8 and U36-1 are identical. When the data pulses do not compare,

the high-level signal from the exclusive OR gate is applied through inverter U37-2 as a low-level error signal to the card error detector.

5-242. Data transition detector No. 2 (U6-6), first half detector No. 2 (U6-9), and 2-bit shift register No. 2 (U7-6 and U7-10) duplicate the transition encoder functional circuits and produce 3-bit coded outputs from OR gate U25-6 that are identical to the 3-bit coded outputs from OR gate U25-8. The data pulses are applied through TE/TR switch S1 and exclusive OR gate U15-11 to data buffer U9-10. The data pulses are clocked out of the data buffer by its associated timing to exclusive OR gate U15-8 in the data comparator circuit, AND gate U21-11, and J-K flip-flop U23-10. The output data pulses from output data buffer U23-7 are also applied to one input of exclusive OR gate U15-8. And gate U21-11 receives an enable signal to pin 12 when the addresses for the two data inputs to the OR gate are the same as described in paragraph 5-253. In effect, exclusive OR gate U15-8 together with AND gate U21-11 perform random samples of one set of data bits at a time. When the two data bits applied to exclusive OR gate U15-8 are not alike for a matched set of addresses, a low-level error signal is applied from AND gate U21-11 to J-K flip-flop U23, which, in turn, produces an error signal to card error detector U17.

5-243. Address comparator U32 produces an A=B output to J-K flip-flop U44-10 in the data compare enable circuit when the write address and read address are the same. The A=B signal is clocked from U44-10 and is applied to J-K flip- flop U14-10 by gated clock signal MGCXX from the GC/DM card. The A=B signal is then clocked through J-K flip-flops U14-10 and U14-6 by system clock MRIOXX and is applied as an enable signal to AND gate U21-11. The two-clock delay provided by the flip-flop circuits compensates for delay due to design features in the output data pulse circuits.

5-244. The enable activity detector is a one-shot multivibrator (U8-6) that is held in conduction by the A=B enable signals from J-K flip-flop U14-6. When the enable signals are missing, the multivibrator completes its duty cycle and applies an error signal to the card error detector.

5-245. VOICE ENCODER (VE) CARD.

5-246. GENERAL. The VE card is the channel option card that services one incoming voice channel. The VE card receives the voice signals and encodes the signals into synchronous digital data that are eventually multiplexed into the multiplexer's serial digital data output.

5-247. BLOCK DIAGRAM DISCUSSION (Figure 5-20).

5-248. The incoming voice signals (DIXX) are applied through a bandpass filter circuit to filter out the out-of-band signals that could affect the encoder circuits. Filtering is accomplished by the attenuation of all signals below 140 Hz and above 5.0 kHz by at least 3 dB. The filtered signals from the bandpass filter are one of two signal voltages applied to a voltage comparator. Reconstructed analog signals from an integrator are the other voltages applied to the comparator.

5-249. In normal operation, the encoder circuits try to make the reconstructed analog signals duplicate the incoming filtered audio signal. Since exact duplication is never achieved, the comparator produces a continuous error (delta) output signal, which, in turn, manipulates the generation of the reconstructed analog signals and the

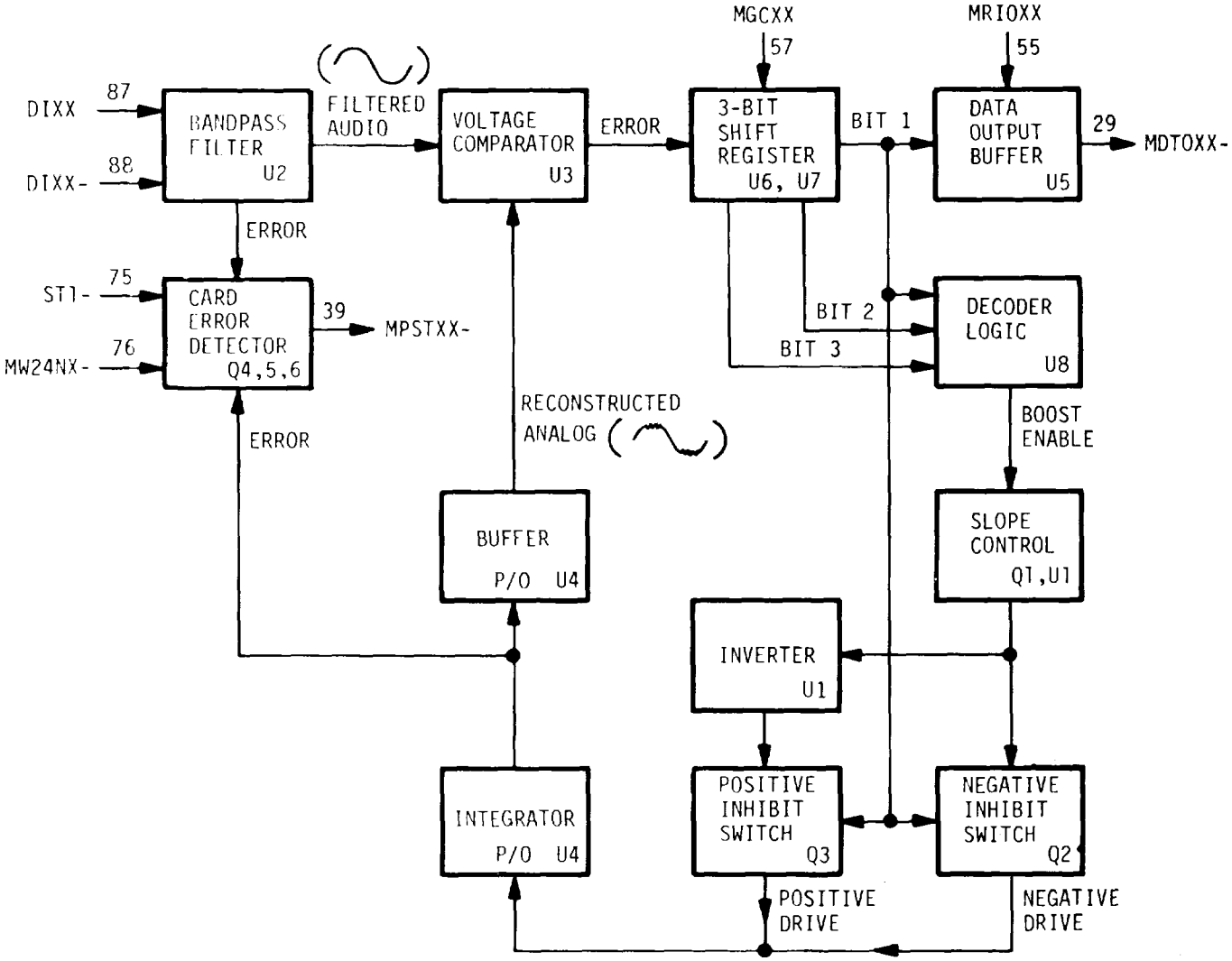


Figure 5-20. VE Card - Block Diagram

derived digital outputs. In normal operation, the encoder circuits continuously change the reconstructed analog signals to minimize the voltage differences between the two signal voltage levels applied to the comparator. It is from this error signal that the digital representation for the analog signals is developed as described in the discussion that follows.

5-250. The decoder logic samples the three bits in the 3-bit shift register for a condition whereby all the outputs are ones or zeros. When the condition exists, the integrator has been driven in the same direction for the last three clock times (MGCXX). At this time, the decoder logic generates an enable signal to the integrator control circuit.

5-251. The integrator control circuit provides a positive or negative drive signal to the integrator. The integrator, in turn, generates the integrated signal that is representative of the incoming analog signal. The integrated signal is subject to constant correction in order to decrease the delta voltage between the incoming signal and the integrated signal. Figure 5-21 shows a typical input audio signal and the integrated signal developed and applied to the comparator. The integrated signal is subject to constant positive or negative signal correction in an attempt to continually decrease the delta voltage output that results from the constant signal comparison.

5-252. A continuous series of high- level or low-level error signal outputs from the comparator is applied to the first stage of a 3-bit shift register. When the reconstructed analog signal voltage level exceeds the voltage level of the applied filtered audio signal voltage, a high level dc voltage is effectively generated from the comparator and is applied to the 3-bit shift register. In turn, a low-level output is generated and applied to the register when the filtered audio signal voltage level exceeds the reconstructed analog signal voltage level. The high-level or low-level dc voltages from the comparator are clocked as digital ones or zeros into the 3-bit data shift register by gated clock pulses MGCXX from the GC/DM card. Bit 1 from the first stage of the shift register is sampled and clocked through the output data buffer by multiplexer system clock signals MRIOX-. Bit 1 is also applied as an enable or inhibit control signal to the negative inhibit switch and the positive inhibit switch.

5-253. The decoder logic generates a boost enable signal to the slope control when it decodes three consecutive zeros or ones from the 3-bit shift register. A series of three consecutive ones or zeros indicates that the integrator has been driven in one direction for three consecutive clock times (MGCXX). The condition normally occurs when high amplitude audio signals or high frequency audio signals are being encoded and the output of the integrator is unable to decrease the amplitude of the error voltage between the filtered audio signal and the reconstructed analog signal. Therefore, when three consecutive ones or zeros are detected by the decoder logic, the boost enable signal is generated to increase the drive voltage from the slope control. Thus, an increased (greater slope) output from the integrator is obtained so that the error voltage between the two signals can be minimized.

5-254. The slope control generates the drive voltage that determines the slope of the output signal from the integrator. The negative drive voltage from the slope control is applied to an inverter and to the negative inhibit switch. The inverted output from the inverter is applied as a positive drive

voltage to the positive inhibit switch. The polarity of the bit 1 (one or zero) signal applied to the two switches determines which switch is enabled to apply either the negative drive or the positive drive signal to the integrator. The integrator, in turn, responds to the applied drive voltage and produces the reconstructed analog signal that is applied through a buffer to the comparator.

5-255. When the decoder logic generates the boost enable signal, the active negative or positive drive signal applied to the integrator increases in amplitude to produce a sharper slope for the drive signal applied to the integrator. The integrator output, in turn, has a sharper rising or falling slope that enables the reconstructed analog signal voltage to increase at a greater rate, thus decreasing the error output from the comparator. As shown in figure 5-21, the reconstructed analog voltage waveform requires continuous corrections to maintain a decreasing error voltage condition. Once the error voltage equals or exceeds the filtered audio signal voltage, the error signal polarity out of the comparator switches from a one to a zero, or from a zero to a one, thus interrupting the successive string of the same polarity pulses from the comparator. The boost enable output from the logic decoder output then returns to its normal decreased drive state until the next series of three ones or zeros is generated from the comparator to indicate the need for a faster correction voltage change.

5-256. Figure 5-21 illustrates the relationship between the data output pulses (MDTOXX-) and the reconstructed analog signals from the integrator. The figure also shows how the reconstructed analog signal effectively tracks the filtered audio signal. When decoded in a demultiplexer, the reconstructed analog signal will be a true reproduction of the original filtered audio signal.

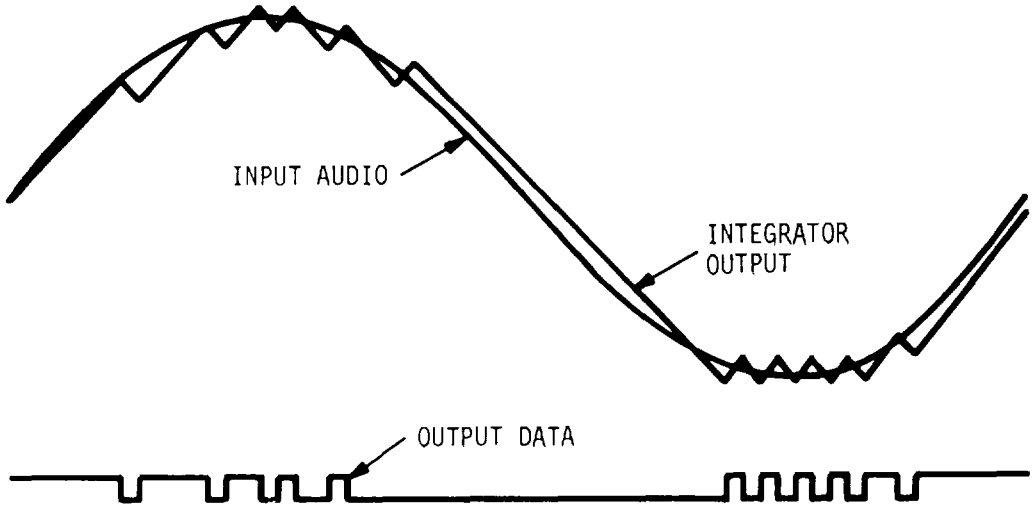


Figure 5-21. VE Card - Waveform Diagram

5-257. The card error detector circuit performs a diagnostic function. The detector samples outputs from the bandpass filter and integrator circuits. When an error occurs, an error signal is generated from the detector during word 24 on the positive stuff request (MPSTXX-) line to the OEG card. Self-test signal ST1- generates an error signal from the, circuit, during word 24, when the SELF TEST switch on the front panel is pressed. During word times other than word 24, signal MPSTXX- is not used.

5-258. DETAILED CIRCUIT DISCUSSION.

5-259. Functional Circuits.

5-260. The voice signals are applied to the primary of isolation transformer T1. The input impedance of the transformer primary is 600 ohms. Operational amplifiers U2-10 and U2-12 function as a bandpass filter circuit. Operational amplifier U2-10 is configured as a low-pass filter circuit and operational amplifier U2-12 is configured as a high-pass filter circuit. The overall gain through U2-10 and U2-12 is approximately 6 db. The filtered analog signals from U2-12 are applied to comparator U3. The comparator also receives the reconstructed analog signals from buffer U4-10. 5-261. When the amplitude of the filter audio signal is greater than the amplitude of the applied reconfigured analog signal, a high-level (one) output is generated from U3 to flip-flop U6-6 in the 3-bit shift register. The output from comparator U3 is serially clocked through the shift register by gated clock signals MGCXX. Bit 1 from U6-6 is the pulse applied as a data pulse to U5-6 in the data output buffer. The digital coded data bits are stored in the buffer for two multiplexer system clock periods (MRIOX-) before being sampled by the GC/DM card.

5-262. The data bits from U6-7 in the shift register are also applied through inverter U9-2 to the base circuits of transistor switches Q2 and Q3. When the output from the inverter is low, switch Q2 is enabled and effectively grounds the negative input from slope control amplifier U1-12 to the negative input (pin 1) of integrator U4-12. The condition allows the positive drive voltage from inverter U1-10 to drive U4-12. In turn, a high output from U9-2 enables switch Q3 and effectively grounds the positive input from slope control amplifier U1-10 to the negative input of integrator U4-12. In turn, this condition allows the negative drive voltage from slope control U1-12 to be applied to integrator U4-12. Therefore, the output from U4-12 varies in relationship to the polarity of the drive voltages applied to U4-1 from U1-12 or U1-10. Figure 5-20 shows the variable output from buffer U4-10 as it is applied to comparator U3 to develop the error voltage that drives the encoder circuits.

5-263. The Q and Q outputs from the three flip-flops that make up the 3- bit shift register are routed to AND gates U8-6 and U8-12. When the three Q or Q outputs are identical, the decoder logic generates a low-level signal that biases Q1 off. This condition drives the voltage level applied to pin 1 of U1-12 more positive and, in turn, drives the output from U1-12 more negative and the output from U1-10 more positive. The positive or negative driver voltage applied to pin 1 of integrator U4-12, in turn, causes the integrator output voltage to vary with an increased slope effect on the reconstructed analog signal applied to the comparator. As soon as the decoder logic detects a reverse output from the first stage of the three-bit shift register, Q1 is biased back into conduction, reducing the dc level to pin

1 of U1-12. This results in a decreased drive voltage to integrator U4-12, thus decreasing the slope of the reconstructed analog signal applied to the integrator circuit.

5-264. Diagnostic Function. Transistors Q4 and Q6 are normally cut off and transistor Q5 is conducting. When an error condition is detected, either transistor Q4 or Q6 is forced into conduction and biases Q5 off. This condition causes Q5 to change from a low input to a high input to inverter U9-8. Inverter U10-11 holds a low-level inhibit to inverter U9-8 at all times except during word 24. Word 24 signal MW24NX- produces a high-level enable output from inverter U10-11 to inverter U9-8 during word 24 and permits Q5 to generate a high-level error signal to the inverter when an error is detected on the card. Transistor Q5 is biased off to generate the high-level error signal when a voltage change to the base of Q4 and Q6 is greater than ±5 volts. This occurs when an operational amplifier malfunctions or when a logic circuit malfunctions and causes one or more of the operational amplifiers to saturate in one direction. The outputs of operational amplifier U2-10, U2-12, and U4-12 provide the diagnostic sample voltages to the base of Q4 and Q6. In turn, a high level input to inverter U9-8 during word 24 produces the low-level error indication using signal MPSTXX-.

5-265. SEQUENCER (SEQ) CARD.

5-266. GENERAL. The seq card is one of the common card types in the multiplexer set. Three major multiplexer timing. and control signals are generated by the seq card: the end-of-scan signals, which identify the end of each word period, are applied to the GC/DM and OEG cards; channel address signals, which select the active channel to receive a gated clock signal, are applied to the GC/DM card; the minor frame equals PS signal is generated and applied to the GC/DM card during each minor frame period that is designated to perform an overhead service function for a selected used port. Paragraphs 5-267 through 5-289 contain the block diagram discussions based on figure FO-3. Paragraphs 5-290 through 5-305 contain the detailed circuit discussion based on the seq card logic diagram in the circuit diagrams manual.

5-267. BLOCK DIAGRAM DISCUSSION (Figure FO-3).

5-268. General.

5-269. In the following discussions, the circuits on the sequencer card are divided into three functions: write, read, and diagnostic. Before the equipment is initially placed in operation, two sets of switches on the card, the PORT STRAPPING switches and the PORTS IN USE switches, are strapped to a selected system configuration. The PORT STRAPPING switches effectively identify the active data channels and the used ports associated with each channel. The PORTS IN USE switches identify the maximum number of ports used in a system configuration.

5-270. Each of the 31 PORT STRAPPING switches represents a port location. A used port representing an active channel is strapped to the A input, and each additional used port associated with an active channel is strapped to the S input. Electrically, an A strapped port is a binary one (+5 vdc) and an S strapped port is a binary zero (ground). Port 1 is assigned active channel 1 and is hardwired in the A strapped configuration. Ports 2 through 31 can be strapped to designate up to an additional 14 active channels, together with their associated used ports. Each system configuration uses a minimum of 15 ports; additional strapping of ports 16 through 31 is

dependent on the individual system requirements. Port assignments are in sequential order. For example, a system configuration using 20 ports will use the first 20 ports (ports 1 through 20); ports 21 through 31 are not used.

5-271. The PORTS IN USE switches control the length of each scan (number of active ports interrogated) in a word format by controlling the maximum number of active ports in the system configuration. A 5-bit binary code for the total number of active ports used for channel addresses is strapped into the PORTS IN USE switches.

5-272. Write Function.

5-273. The major function of the write circuits is to enter a 4-bit channel address for each active port into the random access memories (R.A.M.) on the card. System clock signals RIO and RIO- synchronize the circuits on the card and are derived from system clock signals MRIO from the OEG card. The port scan counter is clocked by RIO and produces sequential 5-bit binary counts (S1, S2, S4, S8, and S16) that are the port addresses to the active port mux, the ports-in-use comparator, and the active port mux in the channel address diagnostics. The counter is incremented until the end-of-scan signal (DEOS-) from the end-of-scan register is applied to it. The signal presets the scan counter to a count of one. The end-of-scan register generates EOS1 when the ports-in-use comparator has a match between the port address and the 5-bit binary count from the PORTS IN USE switches. Thus, each complete scan (or one data word) has a time duration that is equal to the RIO duration times the number of active ports. For example, 22 RIO clock pulses occur in a 22-bit data word that contains 21 active ports and one overhead bit.

5-274. As the port scan counter is incremented, the active port mux sequentially interrogates the PORT STRAPPING switches. When an active channel port is interrogated, a count is multiplexed through the active port mux to increment the active channel counter. The active channel counter is not incremented when the active port mux interrogates a port that is in the S strapped configuration. When a scan is completed, the active channel counter should contain a binary address count that is equal to the number of active channels in the system. The binary address counts from the counter are the sequential channel addresses that are written into the R.A.M. Since the counter is not incremented by strapped ports, the channel address of the last active channel is read into the R.A.M. for each strapped port assigned to an active channel. Table 5-2 shows a typical system configuration based on the use of 22 active ports associated with nine active channel assignments.

5-275. The channel addresses from the active channel counter are also applied to the maximum-channel-used register, which continually generates a binary count that is equal to the maximum number of active channels in the system configuration. The binary count (CHMAXO through CHMAX3) applied to the display card is, in effect, a static count that does not change until the system is reconfigured.

5-276. The R.A.M. accepts channel addresses when a write enable signal is applied from the write/read control. The R.A.M. can store up to 32 sets of 4-bit words. A maximum of 31 sets of 4-bit words (channel addresses) are stored in the R.A.M. when the maximum number of active ports (31) are used. The surplus memory stores in the R.A.M. are inactive in system configurations that use less than 31 active ports. The memory locations that receive the channel addresses are selected by the

Table 5-2. Typical Channel Address Input to R.A.M.

Ports in Use = 22		Scan Counter Output	Write Port Address Counter / R.A.M. Word Addressed	Active Channel Address to R.A.M.
Port No.	Active (A) / Strapped (S)			
1	A	1	(Two-count delay)	
2	S	2	0	0
3	S	3	1	1
4	S	4	2	1
5	A	5	3	1
6	S	6	4	1
7	S	7	5	2
8	A	8	6	2
9	A	9	7	2
10	S	10	8	3
11	A	11	9	4
12	S	12	10	4
13	A	13	11	5
14	S	14	12	5
15	A	15	13	6
16	S	16	14	6
17	S	17	15	7
18		18	16	7
19	S	19	17	7
20	S	20	18	7
21	A	21	19	7
22	A	22	20	7
23		23	21	8

Table 5-2. Typical Channel Address Input to R.A.M. (Cont.)

Ports in Use = 22		Scan Counter Output	Write Port Address Counter / R.A.M. Word Addressed	Active Channel Address to R.A.M.
Port No.	Active (A) / Strapped (S)			
24	Don't care	1	22	9
25	since only			
26	the ports			
27	that are			
28	in use are			
29	interrogated.			
30				
31				

5-bit write port address (PS1, PS2, PS4, PS8, and PS16) applied through the read/write port address selector. The read/write port address selector, in turn, applies the write port address to the R.A.M. when a write address enable from the write/read control is applied to it. The write port address counter is incremented by MRIO and continues to count until it is reset by EOS1 from the end-of-scan register. When the counter is reset, the last count should be the 5-bit binary count for the maximum number of active ports.

5-277. The write/read control generates the write enable to the R.A.M. and the write address enable signal to the read/write port address selector when an error signal is generated from OR gate U47A. The write enable condition lasts for one complete scan cycle (MEOS2 to MEOS2). The controller generates an inhibit signal to AND gate U39 for one scan cycle during every other scan. In normal operation, a write condition should occur when the multiplexer set is powered on and when an error signal is applied to OR gate U47A as described in the diagnostic function.

5-278. Three levels of end-of-scan signals (EOS, EOS1, and EOS2) are generated from the end-of-scan register each time an A=B signal is applied to it. Signal EOS1 occurs one RIO clock time after each end of scan, and EOS2 occurs one clock time after EOS1 occurs. Note that DEOS resets the port scan counter to a count of 1 and EOS1 resets the write port address counter to a count of 0. The result is a two- RIO-clock delay between the two counters. The delay is required to recover a two-RIO-clock delay related to the logic implementation. Signal EOS1 presets the active channel counter to zero and causes the maximum 4-bit channel address from the active channel counter to be loaded into the maximum channel used register.

5-279. Read Function.

5-280. The major function of the read circuits is to generate the 5-bit read port addresses that select and read out the 4-bit channel addresses stored in the R.A.M. for each active port. The read circuits are configured so that the 5-bit read port addresses to the R.A.M. are applied, not in sequential order, but in the near-homogeneous sequence as described below.

5-281. As the read port address counter is incremented by RIO, sequential 5-bit read port addresses are generated for the active ports in the system. To obtain the near-homogeneous readout of the channel addresses for the active ports, the weights of the binary bits from the read port address counter to the read/write port address selector are reversed (LSB becomes MSB, etc). The result is a near-homogeneous selection of channel addresses for the active ports as shown in table 5-3.

5-282. The decimal state of the reverse binary codes listed in table 5-3 shows that some of the forward binary numbers for ports greater than

Table 5-3. Homogeneous Port Addresses to R.A.M.

Read Port Address Counter 5-Bit Binary Output	Decimal State	Read Port Address to R.A.M. After Reversal of Binary Weights	Equivalent Decimal State
MSB LSB		MSB LSB	
0 0 0 0 0	0	0 0 0 0 0	0
0 0 0 0 1	1	1 0 0 0 0	16
0 0 0 1 0	2	0 1 0 0 0	8
0 0 0 1 1	3	1 1 0 0 0	24
0 0 1 0 0	4	0 0 1 0 0	4
0 0 1 0 1	5	1 0 1 0 0	20
0 0 1 1 0	6	0 1 1 0 0	12
0 0 1 1 1	7	1 1 1 0 0	28
0 1 0 0 0	8	0 0 0 1 0	2
0 1 0 0 1	9	1 0 0 1 0	18
0 1 0 1 0	10	0 1 0 1 0	10
0 1 0 1 1	11	1 1 0 1 0	26

Table 5-3. Homogeneous Port Addresses to R.A.M. (Cont)

Read Port Address Counter 5-Bit Binary Output	Decimal State	Read Port Address to R.A.M. After Reversal of Binary Weights	Equivalent Decimal State
MSB LSB		MSB LSB	
0 1 1 0 0	12	0 0 1 1 0	6
0 1 1 0 1	13	1 0 1 1 0	22
0 1 1 1 0	14	0 1 1 1 0	14
0 1 1 1 1	15	1 1 1 1 0	30
1 0 0 0 0	16	0 0 0 0 1	1
1 0 0 0 1	17	1 0 0 0 1	17
1 0 0 1 0	18	0 1 0 0 1	9
1 0 0 1 1	19	1 1 0 0 1	25
1 0 1 0 0	20	0 0 1 0 1	5
1 0 1 0 1	21	1 0 1 0 1	21
1 0 1 1 0	22	0 1 1 0 1	13
1 0 1 1 1	23	1 1 1 0 1	29
1 1 0 0 0	24	0 0 0 1 1	3
1 1 0 0 1	25	1 0 0 1 1	19
1 1 0 1 0	26	0 1 0 1 1	11
1 1 0 1 1	27	1 1 0 1 1	27
1 1 1 0 0	28	0 0 1 1 1	7
1 1 1 0 1	29	1 0 1 1 1	23
1 1 1 1 0	30	0 1 1 1 1	15
1 1 1 1 1	31	1 1 1 1 1	31

22 are required to obtain the reverse binary numbers for ports 3, 19, 11, 7, and 15. For example, the binary count for 25 in reverse is port 19. Also, in the forward binary code listing, binary numbers for 7, 11, 15, 19, 23, 27 and 29 are deleted, since their reverse binary numbers are greater than 22. For example, binary count 7 in reverse is port 28. Therefore, to add and delete the necessary forward binary numbers, the circuit function described in paragraph 5-293 is required.

5-283. The following circuits perform the addition and deletion function necessary to develop an address for each of the active ports in the system. The 5-bit read port address from the read port address counter is applied to an N+1l adder that increases the binary count by one. The weights of the 4-bit binary code output from the adder are reversed so that the address applied to the read ports-in-use comparator is the same as the read port address being applied to the R.A.M. plus one. The reversed binary address is compared against the ports-in-use binary count that represents the maximum number of active ports in the system. When the reversed read port address is a binary number that exceeds the maximum number of active ports, an A is greater than B output from the comparator enables the read reset generator. The read reset generator, in turn, produces a preset signal that presets the read port address counter to its present count plus two. Thus, the counter skips the undesired read port address and proceeds to the next count, which is an active port. Thus, the read port counter produces an equal number of read port addresses that equals the number of active ports. Table 5-4 shows the truncated listing for a 22 used ports system.

5-284. Each active port has access to overhead service one time in each major frame period during a selected minor frame. The port assignment for a given minor frame is controlled by the minor frame equals port sequence comparator. The comparator generates an A=B output signal when the read port address from the read port address counter matches the minor frame count (MMFCO through MMFC4). An A=B output signal is generated once each scan, but is generated through AND gate U47B as signal MMF=PS during word 28. At the time that MMF=PS is generated, the port receiving the overhead service is the reverse binary equivalent of the binary output from the read port address counter. Since the port selected is the reverse binary equivalent of the counter output, each active channel receives the near-homogeneous overhead service at its associated ports.

5-285. Diagnostic Function.

5-286. The diagnostic circuits on the sequencer card perform two functions. The main function is to provide an error indication when a hardware malfunction occurs. Two diagnostic signals can be generated from the diagnostic circuits: loss of end of scan signal MLEOS-, which is generated when a loss of the end-of-scan signal is detected; and sequencer diagnostic signal MSEQ-, which is generated when a hardware malfunction affecting the channel address sequence is detected. The second function of the circuits is to initiate a R.A.M. rewrite condition when a channel address check detects an out-of-sequence condition.

5-287. The end-of-scan activity detector generates an error signal when signal MEOS2 from the end-of-scan register is missing. The error signal is applied to OR gate U47A and to the loss-of-scan diagnostic latch. The

Table 5-4. Truncated Port Addresses to R.A.M. in 22 Used Ports Configuration

Read Port Address Counter 5-Bit Binary Output (After Truncation)	Decimal State	Read Port Address to R.A.M. After Reversal of Binary Weights	Equivalent Decimal State
MSB LSB		MSB LSB	
0 0 0 0 0	0	0 0 0 0 0	0
0 0 0 0 1	1	1 0 0 0 0	16
0 0 0 1 0	2	0 1 0 0 0	8
0 0 1 0 0	4	0 0 1 0 0	4
0 0 1 0 1	5	1 0 1 0 0	20
0 0 1 1 0	6	0 1 1 0 0	12
0 1 0 0 0	8	0 0 0 1 0	2
0 1 0 0 1	9	1 0 0 1 0	18
0 1 0 1 0	10	0 1 0 1 0	10
0 1 1 0 0	12	0 0 1 1 0	6
0 1 1 0 1	13	1 0 1 1 0	22
0 1 1 1 0	14	0 1 1 1 0	14
1 0 0 0 0	16	0 0 0 0 1	1
1 0 0 0 1	17	1 0 0 0 1	17
1 0 0 1 0	18	0 1 0 0 1	9
1 0 1 0 0	20	0 0 1 0 1	5
1 0 1 0 1	21	1 0 1 0 1	21
1 0 1 1 0	22	0 1 1 0 1	13
1 1 0 0 0	24	0 0 0 1 1	3
1 1 0 0 1	25	1 0 0 1 1	19

Table 5-4. Truncated Port Addresses to R.A.M. in 22 Used Ports Configuration

Read Port Address Counter 5-Bit Binary Output (After Truncation)	Decimal State	Read Port Address to R.A.M. After Reversal of Binary Weights	Equivalent Decimal State
MSB LSB		MSB LSB	
1 1 0 1 0	26	1 1 0 1 1	11
1 1 1 0 0	28	0 0 1 1 1	7
1 1 1 1 0	30	0 1 1 1 1	15

loss-of-scan diagnostic latch generates signal MLEOS- when an error signal is applied to it. Signal MLEOS- is applied to the display card to inhibit error indications from the channel cards that use MEOS2. An error, signal to OR gate U47A sets the out-of-sequence diagnostic flip-flop and generates error signal MSEQ- that is applied to the display card. The output from U47A also sets the write/read control so that a write function to the R.A.M. is generated for one scan time. In normal operation the inhibit signal from the write/read control is applied to AND gate U39 during every other scan time to inhibit the channel address comparator output for every other scan time. The comparator output is inhibited during the time that a write function is being performed on the R.A.M. in the channel address diagnostics. The inhibit prevents the comparator from initiating an error condition during normal operation when the diagnostic R.A.M. is in the write mode. Therefore, a noncompare in the comparator exists during the scan when the equipment is in the write mode. When in the error state, the loss-of-scan diagnostic latch and/or the out-of-sequence diagnostic flip-flop resets when the RESET switch on the front panel is pressed. Both diagnostic circuits are set to their error state when the self-test switch on the front panel is set to the on (up) position. When the SELF TEST switch is set to the off (down) position, error reset signal ERST- is generated and resets the diagnostic circuits.

5-288. Error signal PSERR- is generated from the port sequence error detector when signal MMF=PS is generated at the same time that the port-is- in-sequence comparator output is A is greater than B. The A is greater than B signal indicates an unused port that should not be serviced. In turn, the MMF=PS signal is developed only for active ports that are serviced. For example, assuming that the maximum number of active ports in a given system configuration is 22, minor frames 23 and up are not used for overhead servicing of ports. Therefore, when the MMF=PS signal is present, the comparator output should be A is not greater than B.

5-289. The channel address diagnostic circuits are a duplication of the functional circuits that produce the channel addresses (MCHAD1 through MCHAD8). The 4-bit channel addresses from the diagnostic and functional circuits are

applied to the channel address comparator. In normal operation, the channel addresses should compare and produce an A=B output from the comparator. The A-B output is applied through inverter U31 and inhibits AND gate U39. The inhibit signal applied to AND gate U39 from the write/read controller is generated every other scan time (EOS2 to EOS2). Therefore, an error signal is developed and applied to OR gate U47A when the channel addresses are not the same and the inhibit signal to AND gate U39 is not present. The operation of the out-of-sequence flip-flop and the write/read controller is the same as that described in paragraph 5-287.

5-290. DETAILED CIRCUIT DISCUSSION.

5-291. Write Function. Port scan counter U2, U3 is incremented by system clock signals MRIO applied through inverters U4 and US5. At the end of each scan (EOS to EOS), the counter is preset to a count of one by end-of-scan signal DEOS- from flip-flop U21-6 in the end-of-scan register circuits. The counter sequentially generates one 5-bit port address (signals S1, S2, S4, S8, and S16) for each used port in the system configuration. Each port read address causes active port multiplexer US, U27 to interrogate one of the PORT STRAPPING switch positions. Each PORT STRAPPING switch set in the A position causes a low output from U8 or U27 to be applied to OR gate U15-6 to produce a high input to flip-flop U29. In turn, each high input to U29 increments active channel counter U16 one count. Therefore, during one complete scan, or word time, counter U16 is incremented to a count that equals the number of active channels in the configuration. In turn, a complete word or scan time is obtained when the port address from counter U2, U3 that is applied to ports-in-use comparator U34 is equal to the ports-in-use count that is applied to U34 from the PORTS IN USE switches. At the time that the counts are equal, an A=B signal is applied from U34 to flip-flop U21-6 in the end-of-scan register circuits. The Q output from flip-flop U21-6 produces end-of-scan signal DEOS- when the next system clock signal MRIO occurs. In turn, the Q output from U21-5 is a high input to flip-flop U21-9. The Q output from U21-7 goes low when the next system clock signal MRIO occurs. The low signal presets write port address counter U9, U22 and active channel counter U16, and clears read port address counter U36, U43. The Q output from U21-7 also inhibits AND gate-U37-3 in the read reset generator. The Q output from U21-9 is applied to flip-flop U33-9 to generate end-of-scan signals MEOS2B and MEOS2B-. The Q output from U21-9 is also applied to flip-flop U33-5, which generates end- of-scan signal MEOS2 that is applied to flip-flop U40-5 in the write/read control circuit. The Q output from U33-6 is applied as a clock signal to flip-flop U32-9 in the write/read control circuit.

5-292. Write port address counter U9, U22 is sequentially incremented by system clock signals MRIO. The 5-bit write port address from U9, U22 is applied through read/write port address selector U10, U23 to R.A.M. U18, U19 during the write function. Each time system clock signal MRIO and the write enable signal from the write/read control circuit are applied to AND gated U39-3, the 4-bit binary channel address in the active channel counter is written into the R.A.M.

5-293. When the equipment is turned on, the channel addresses-read out of the functional R.A.M. are not the same as the channel addresses read out of the diagnostic R.A.M. over a given period of time, since the circuits have a random start. Therefore, when channel address comparator U20 does not produce an A=B signal during a compare

time, the write/read control circuits generate a write enable signal to the functional write circuits for one scan time. Once the channel addresses are correctly written into the two R.A.M.'s, the channel address comparator produces A=B signals in a no-error condition. In turn, the write/read control circuits inhibit the write mode until a no-compare condition is detected by U20. The operation of the write/read control circuits is described in paragraph 5-298.

5-294. Read Function. The 5-bit read port address from read port address counter U36, U43 is applied to N+1 adder U44 and to minor frame equals port sequence comparator U28, U42. The port address from U36, U43 is also applied, with the weights of the binary bits reversed, to read/write port address selector U10, U23. The output from U44 is applied to the A inputs of read ports-in-use comparator U35. At this point, the weights of the binary bits are again reversed to their original value to produce the same address (plus one) that is applied to U10, U23. When the address from U35 is greater than the fixed binary count from the PORTS IN USE switches, an enable signal is applied to one input of AND gate U37-3 in the read reset generator circuit. The termination of end-of-scan signal enables U37-3 and a high is applied from OR gate U37-6 to flip-flop U29-7. When U29-7 is clocked and a high is applied from inverter U45-4, AND gate U37-8 applies a low load signal to U36, U43. This causes counter U36, U43 to skip the next sequential count since the count preset into the counter is equal to the existing count plus two. This function prevents the counter from generating a port number that is higher than the highest number of used ports in the system configuration.

5-295. Each 5-bit channel address from the read port address counter is also applied to the B inputs of minor frame equals port sequence comparator U42, U28. The minor frame count signals (MMFCO through MMFC3) are applied to the A inputs of U42. Exclusive OR gate U28- 8 processes the MSB (MMFC4) of the 5-bit channel address. Comparator U42 processes the other four bits. Each time the channel address applied to U42, U28 is the same as the minor frame count, an A=B (high) signal is generated from U42 to AND gate U47-6, and a low signal is generated from U28-8 and is applied through inverter U31-6 to AND gate U47-6; Therefore, AND gate U47-6 produces a low output during word 28 when a compare is made. The signal is applied through inverter U31-4 to produce signal MMF=PS.

5-296. Read/write port address selector U10, U23 applies a write address to R.A.M. U18, U19 in the write mode each time a write enable (high) signal is applied from the Q output of flip- flop U32-8. In turn, a read enable (low) signal is applied from the Q output of U32-8 to U10, U23 in the read mode, allowing the read address to be applied to the R.A.M. The write or read enable signal that is applied through AND gate U39-3 to the R.A.M. is controlled by the Q output from flip-flop U32-9. During the read mode, the 4-bit binary channel address in the selected R.A.M. address is read out of the QO through Q3 outputs of R.A.M. U18, U19 to the four associated reclocking flip-flops (U25-5, U25-9, U26-5, and U26-9). The Q outputs of the four reclocking flip-flops produce the four output channel address signals MCHAD1, MCHAD2, MCHAD4, and MCHAD8.

5-297. The Q outputs of the four reclocking flip-flops are applied to the A inputs of channel address comparator U20. The four channel address signals generated in the channel address diagnostic circuits are applied to the B inputs of U20. In normal operation, an A=B output from U20 is applied through inverter U31-8 as an inhibit signal to one input of AND gate U39-6.

When a no-compare is detected in U20, the inhibit signal to AND gate U39-6 becomes an enable signal, The Q output from flip-flop U32-6 in the write/read control circuit goes high every other time end-of-scan signal MEOS2 is generated. The high Q output enables the other input to AND gate U39-6. At the time that both inputs to U39-6 are high, a low error signal is applied to OR gate U47-12 to produce a high input to flip-flop U40-9 in the write/read control circuits. This condition causes the write/read control circuits to initiate a write mode.

5-298. Write/Read Control Circuit. Flip-flop U40-9, together with flip- flop U32-9, produces a write enable signal to read/write port address selector U10, U23 and to R.A.M. U18, U19 when the output from OR gate U47-12 is high. The output from OR gate U47-12 is forced high by one of three conditions: (1) when the functional and diagnostic channel addresses are not the same, (2) when end-of-scan signal MEOS2 is missing, and (3) when error signal PSERR- is generated. A high output from OR gate U47-12, together with system clock signal MRIO, produces a high Q output from U40-9 to flip-flop U32-9. When the next end-of-scan signal from flip-flop U33-6 is applied to U32-9, the Q output from U32-9 goes high and enables one input of AND gate U39-3 in the R.A.M. input. In turn, U39-3 enables the write input of the R.A.M. each time system clock signal MRIO- occurs. The low Q output from U32-8 enables the write address input of read/write port address selector U10, U23. The Q output from U32-8 also presets flip-flop U32-6 and clears flip-flop U40-9. This causes the Q output from U32-6 to inhibit AND gate U39-6 so that the read mode is enabled when the next end-of-scan signal occurs. Flip-flop U40-9 is held in the clear state to ensure that flip-flop U32-8 is set for a high Q output by the next end-of-scan signal and a normal read mode is produced. The write cycle is completed when the next end-of-scan signal sets the Q output of U32-9 low to inhibit AND gate U39-3 in the R.A.M. input. At this time, U39-3 applies the read enable signal to the R.A.M. The high Q output from U32-8 enables the read address input to the read/write port address selector.

5-299. Flip-flop U40-5 in the write/ read control circuit is toggled by end-of-scan signal MEOS2 from flip- flop U33-5. This flip-flop produces the read and write enable signals to the channel address diagnostic circuits. When the Q output of U40-5 is high, one input of AND gate U39-11 is enabled and a write enable signal is applied to R.A.M. U12, U13 each time system clock signal MRIO- occurs. In turn, the low Q output from U40-5 enables the write address input to read/write port address selector U11, U23. At the same time, the Q output from flip-flop U32-6 is a low inhibit input to one input of AND gated U39-6, which inhibits channel address comparator U20 when the channel address diagnostic circuits are in the write mode. When the next end-of-scan signal toggles U40-5, the channel address diagnostic circuits switch to the read mode. In turn, the Q output from U32-6 enables the channel address comparator. Therefore, channel address comparator U20 is inhibited during the write mode to prevent an erroneous no-compare from U20.

5-300. Diagnostic Circuits. As described in the preceding paragraph, the channel address diagnostic circuits produce duplicate channel address signals during every other scan time (MEOS to MEOS). The operation of the diagnostic channel address circuits is identical to that of the functional channel address circuits. The major components in the diagnostic channel

address circuits are active port multiplexer U1, U14, active channel counter U6, R.A.M. U12, U13, read/write port address selector U6, U23, and channel flip-flop set U7. When a no-compare condition is detected by address comparator U20, the output from OR gate U47-12 goes high to initiate the write mode as previously described. The high output from OR gate U47-12 is also applied to flip-flop U30-7. The flip- flop, in turn, produces sequencer diagnostic error signal MSEQ- when the output from OR gate U47-12 is high and signal MRIO occurs.

5-301. End-of-scan activity detector U48-10 is held in conduction during normal operation by end-of-scan signals MEOS2 from flip-flop U33-5. When the signals are missing, the duty cycle of U48-10 expires and sets latch U39, U47 to produce loss of end of scan signal MLEOS-. The low output from U48-10 is also applied to OR gate U47-12 to initiate signal MSEQ- from flip-flop U30-7.

5-302. In normal operation, during each minor frame period, port-is-in- sequence comparator U41 produces an A is greater than B (high) signal when the minor frame count in signals MMFCO through MMFC4 is greater than the count applied to U41 from the PORTS IN USE switches. In each minor frame period that an A is greater than B signal is generated, minor frame is in port sequence signal MMF=PS is not generated in a no-error condition. In turn, signal MMF=PS is generated during word 28 of each minor frame period that U41 does not generate the A is greater than B output signal in a no-error condition. This diagnostic function is performed to ensure that a used port is not selected for overhead servicing during a minor frame period that is not eligible for overhead service. The number of minor frames eligible for overhead service is equal to the number of used ports in the configuration.

5-303. When word 28 signal MW28 is applied through inverter U45-6 to the port sequence error detector circuit, the Q output from flip-flop U38-5 goes high to enable one input of AND gate U46-6. AND gate U46-6 remains inhibited to produce a high output during word 28 by the low inhibit input from inverter U45-6. In turn, the output from inverter U45-10 is a low input to flip-flop U38-9 until word 28 signal MW28 terminates at the end of word 28. At the end of word 28, the output of inverter U45-6 goes high and briefly enables AND gate U46-6 until system clock signal MRIO- occurs and the Q output of U38-5 goes low. While U46-6 is enabled, the output from U45-10 is high to the K input of flip- flop U38. At the time that signal MRIO- occurs, U38 is clocked and the Q output to AND gate U46-11 goes high. The Q output from U38-7 is driven high at the end of each word 28. Therefore, when signal MMF=PS is generated during word 28, both inputs to AND gate U46-11 are high for one clock time and causes a high Q output from flip-flop U30-5 when the next signal MRIO occurs. During the rest of word 28, the J and K inputs to flip-flop U30-5 remain low and the Q output from the stage does not change. Therefore, the Q output from U30-5 is a high input to one input of exclusive OR gate U28-11. When the minor frame count applied to ports-in-sequence comparator U41 during the minor frame period is equal to or less than the number of used ports, a high input is applied from inverter U45-2 to the other input of exclusive OR gate U28-11. Therefore, when word 28 is terminated, the output from inverter U45-10 goes high for a brief time as explained above and the high signal enables one input of AND gate U37-11. Since both inputs to exclusive OR gate U28-11 are high at this time, a low inhibit signal is applied from U28-11 to U37-11 to prevent the generation of error signal PSERR-.

5-304. When signal MMF=PS is generated during word 28 and an A is greater than B output is produced from U41, an error condition exists. At this time, the input to exclusive OR gate U28-11 from inverter U45-2 is low and the input to the exclusive OR gate from U30-5 is high. This condition causes a high input to AND gate U37-11 from the exclusive OR gate at the time that a high is applied to the other input of U37-11 from U45-10. This error condition allows AND gate U37-11 to be enabled and produce error signal PSERR- to OR gate U47-12 and produce the diagnostic signals previously described.

5-305. Self-test signal ST2- sets diagnostic latch U39, U47 and presets flip-flop U30-7 to generate diagnostic error signals MSEQ- and MLEOS- during the self-test mode. When the self-test mode is completed, error reset signal ERST clears flip-flop U30-7 and resets diagnostic latch U39, U47 to its normally off state when the equipment is in a no-error state. Signal ERST also resets the circuits to their no-error state when the DISPLAY RESET switch on the front panel is pressed.

5-306. GATED CLOCK/DATA MUX (GC/DM) CARD.

5-307. GENERAL. The GC/DM card is one of the common card types in the multiplexer set. One of the GC/DM cards is used in the multiplexer and a second card is used in the demultiplexer. The functional discussions for the circuits on the card are divided into three parts: format generation functional circuits, which generate word counts 1 through 29, minor frame counts 1 through 31, terminal minor frame count 31, and the three overhead stuffing codes that are used in the other common cards; gated clock generation functional circuits, which generate the gated clock signals for up to 15 active channels; and data mux circuits, which perform time division multiplexing of the digital data from 1 to 15 channel cards, plus overhead data, into one digital data output stream that is routed to the reference timer card. The block diagrams related to the block diagram discussions are shown in figures 5-22 through 5-26. The logic diagrams associated with the detailed circuit discussion for the GC/DM card are in the circuit diagrams manual.

5-308. BLOCK DIAGRAM DISCUSSION.

5-309. Format Generation Function (Figure 5-22).

5-310. The generation of the timing signals is initiated and controlled by end-of-scan signals MEOS2B and MEOS2B- from the sequencer card. End- of-scan signal MEOS2B- increments the word counter from words 1 through 29. Each time word 29 signal MW29 is generated, a preset-to-1 signal is applied to the counter from the words 28/29 decoder.

5-311. The 5-bit word count signals WCO through WC4 from the word counter are applied to the word 27 decoder, the read only memory (ROM), and to the words 1 through 23 decoder. The words 1 through 23 decoder generates an enable signal to the ROM during word times 1 through 23, and an inhibit signal to the ROM during word times 24 through 29. The decoder also generates word 24 through word 29 signal DW2429 that is applied to the data mux function on this card during word times 24 through 29.

5-312. The ROM generates two sets of the three stuffing codes NAC, NSC, PSC, and NACD, NSCD, PSCD during words 1 through 23. Signals NAC, NSC, and PSC are applied to the data mux function and signals NACD, NSCD, and PSCD are applied to the diagnostic data mux
function.

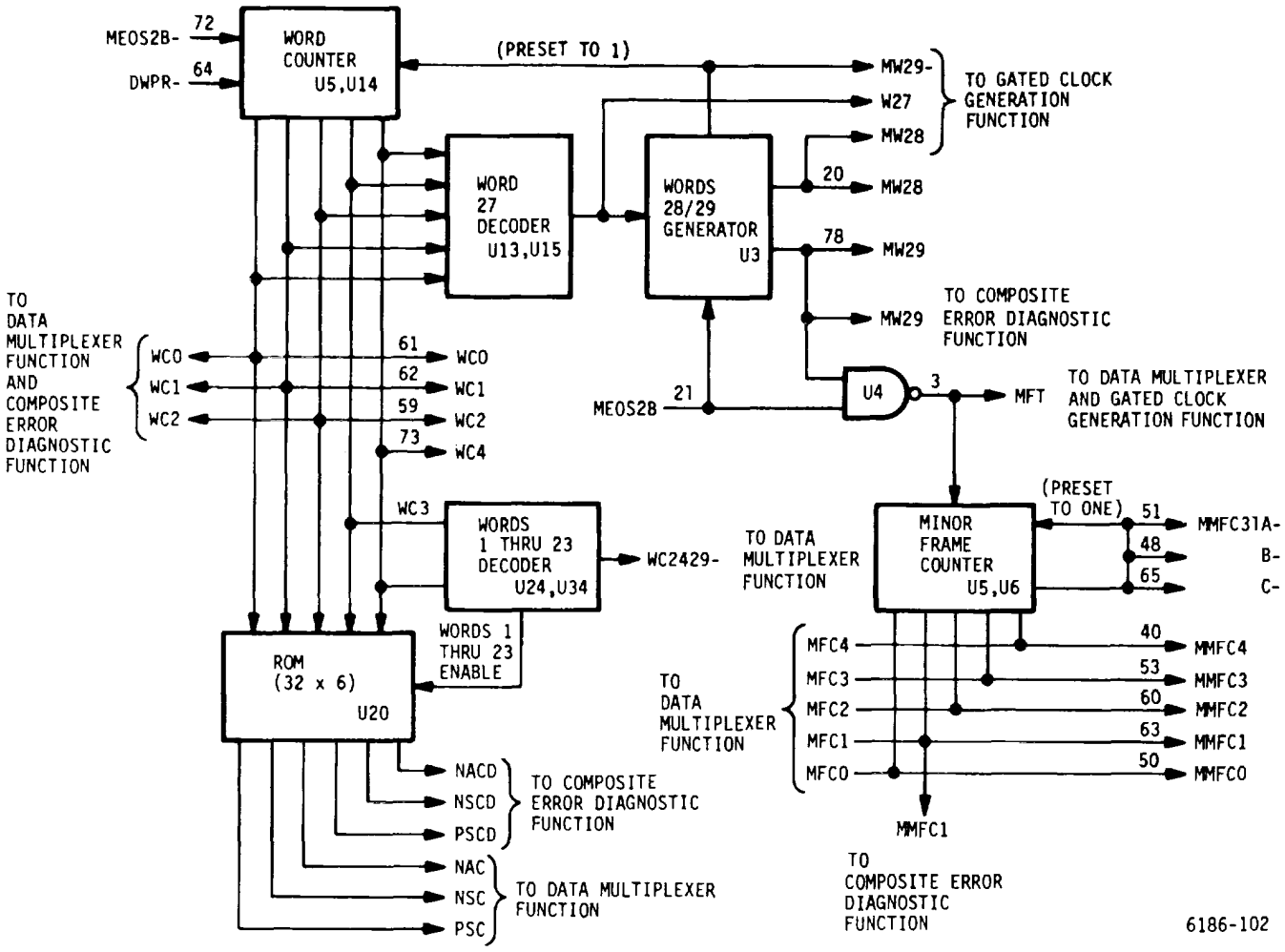


Figure 5-22. GC/DM Card, Format Generation Circuits - Block Diagram

5-313. At word count 27, the word 27 decoder generates word 27 that is applied to the words 28 and 29 generator once each minor frame. Words 28 and 29 are clocked out of the generator by end-of-scan signal MEOS2B from the sequencer card. Word MW29- is applied to the data mux function routed to the OEG card, and is also used to preset the word counter to a count of 1. Signal word 29 is applied to the word 29 activity detector in the diagnostic circuits and is also routed to the OEG card. Word 28 is routed to the sequencer card.

5-314. When signals MEOS2B and MW29 are present, AND gate U4 generates minor frame transition signal MFT that increments the minor frame counter once each minor frame. Signal MFT is also applied to the gated clock function on the card. The minor frame counter produces 5-bit minor frame count signals MMFCO through MMFC4 that sequentially count from minor frame counts 1 (MMFC1) through 31 (MMFC31). The counter also generates three sets of minor frame 31 signals MMF31A, MMF31B, and MMF31C that are routed to the channel card locations in the multiplexer.

Minor frame count MMFC1 is applied to the minor frame activity detector circuit in the diagnostic function.

5-315. Gated Clock Generation Function (Figure 5-23)

5-316. Gated clock signals are generated and applied to the RCB and TE/TR channel cards to systematically clock channel data out of storage registers on the channel cards to the output data multiplexer on the GC/DM card. During each data word, one gated clock signal is generated for each used (active or strapped) port in the multiplexer configuration. The total number of gated clocks generated during one word period is a preset variable between 15 and 31. Each used port in a multiplexer configuration is assigned to one of the active channels. The gated clock signal generated for a given used port carries the channel address of the active channel to which it is assigned. For example, if active channel No. 1 has four used ports, it will

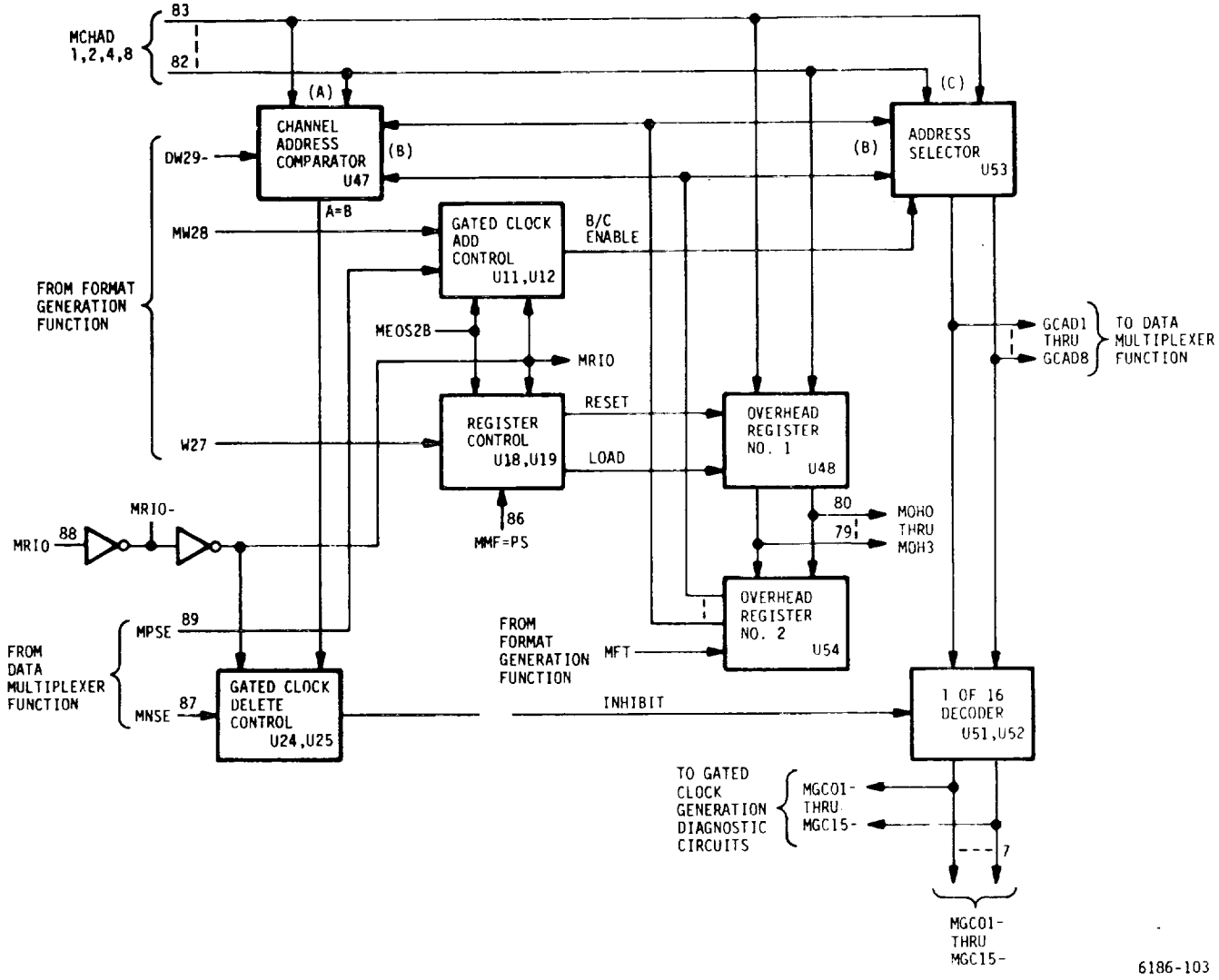


Figure 5-23. GC/DM Card, Gated Clock Generation Circuits - Block Diagram

normally receive four gated clock signals MGCO1. The port-to-channel assignment is programmed and performed on the sequencer (seq) card. The seq card, in turn, applies the appropriate channel assignment for each used port back to the GC/DM card through 4-bit binary channel address signals MCHAD1 through MCHAD8. Since a maximum of 15 active channels can be used, gated clock signals from the GC/DM card are designated as MGC01 (channel 1) through MGC15 (channel 15).

5-317. In addition to the normal gated clock signals that are generated as described in paragraph 5-316, each used port receives overhead servicing during a designated minor frame in each major frame period. During word 29 of the minor frame designated for a particular port, the total number of gated clock signals applied to the active channel with which the port is associated may be increased or decreased by one, or left unchanged. If a gated clock signal is deleted, it is the first gated clock signal normally routed to that channel during word 29. If an extra gated clock is added, it is generated and applied to the channel during bit 0 of word 29.

5-318. In normal operation, 4-bit binary channel address code MCHAD1 through MCHAD8, from the sequencer card, selects the channel number of the channel card that will receive a gated clock signal. The channel address is routed to the channel address comparator, overhead register No. 1, and the address selector. In normal operation, the channel address for the channel that receives the next gated clock is routed directly to the C input of the address selector. The C input is enabled by the C enable signal from the gated clock add control. The address in the address selector is applied to the 1-of-16 decoder and is decoded into the appropriate gated clock signal (MGC01 through MGC15) that is routed to the designated channel card.

5-319. An overhead service function is initiated when minor frame equals port sequence signal MMF=PS selects the channel address associated with the used port that has access to overhead service during a given minor frame period. One signal MMF=PS is applied one time to the register control circuit for each used (active and strapped) port associated with each channel address during one major frame period. Before signal MMF=PS is applied to the card from the sequencer card, MEOS2B and word 27 signal W27 enable the register control circuit to generate a reset signal to overhead register No. 1. When reset, the output from overhead register No. 1 is 0000. The output remains 0000 until signal MMF=PS is present to identify a minor frame that services a used port. Therefore, the output is 0000 for each minor frame period associated with an unused port. The 0000 channel address prevents unused ports from gaining access to overhead service as described in the detailed theory of operation. Signal MMF=PS enables the register control circuit to generate a load signal to overhead register No. 1 during word 28. The load signal, in turn, loads the present channel address (MCHADO through MCHADB) into overhead register No. 1. This is the channel address for the active channel that receives overhead service during the next minor frame period. At the end of each minor frame, minor frame transition signal MFT enables overhead register No. 2 to load the channel address in the output of overhead register No. 1. At this time, the address loaded into overhead register No. 2 is applied to the B input of the channel address comparator and to the address selector. The channel address loaded into register No. 2 is also applied as overhead address count signals MOHO through MOH3 to the OEG card.

5-320. The channel address applied to the B input of the channel address comparator identifies the channel selected for overhead servicing. When the incoming channel address applied to the A input of the channel address comparator during word time 29 matches the address at the B input, signal A=B is generated and applied to the gated clock delete control circuit. The gated clock delete control circuit, in turn, generates an inhibit signal to the 1-of-16 decoder when A=B and negative stuff enable signal MNSE are applied to it. The inhibit signal applied to the l-of-16 decoder prevents the circuit from decoding and generating a gated clock signal for the channel address being applied to it. Thus, one normal gated clock signal is deleted from the designated channel address during word 29 for a negative stuff overhead function.

5-321. When positive stuff enable signal MPSE and end-of-scan signal EOS2B are applied to the gated clock add control circuit during word 28, a B enable signal is generated and applied to the address selector. The B enable signal to the address selector routes the channel address at the B input to the l-of-16 decoder. The 1of-16 decoder, in turn, decodes and generates a gated clock signal for the selected channel address. Thus, one additional gated clock signal is generated during bit 0 of word 29 in the performance of the positive stuff overhead function. The channel address routed through the address selector is also applied as 4-bit binary channel address signals GCAD1 through GCAD8 to the data multiplexer function to select the channel data inputs to the multiplexer for the active channel cards.

5-322. Data Multiplexer Function (Figure 5-24). 5-323. The data multiplexer functional circuits interleave up to 15 channel data inputs from the channel cards, plus the overhead data input, into one serial digital data stream that is routed to the reference timer card. The 4-bit binary channel addresses (GCAD1 through GCAD8) select the inputs applied to the output data multiplexer. The signals are routed through three delay registers to provide an accumulated time delay of three MRIO time periods and compensate for the time delay in the logic implementation that is required to apply a gated clock to a channel card, interrogate the channel for data, and then transmit the data back to the output data multiplexer. Each 4-bit channel address selects one of the channel data inputs or the overhead data input that is applied to the output data multiplexer. Channel data out signals MDT001 through MDT015 are the maximum number of inputs that can be routed from the channel cards to the output data multiplexer. Only those signals representing the active channels are actually applied to the output data multiplexer. For example, a system with six active channels applies signals MDT001 through MDT006. Once each word time, an overhead bit is routed from the overhead data multiplexer to the output data multiplexer. During each word time, one data bit representing each strapped port associated with the active channels is applied to the output data multiplexer. Under control of channel address signals GCAD1 through GCAD8, the inputs to the output data multiplexer are interleaved into a serial data stream that is applied to a reclocking flip-flop circuit. The flip-flop circuit, in turn, produces complementary output serial data streams MSD and MSD that are clocked by multiplexer clock MRIO. Output serial data stream MSD, which is the multiplexer output signal, is routed to the reference timer card, and MSD- is applied to the frame sync for loopback test purposes.

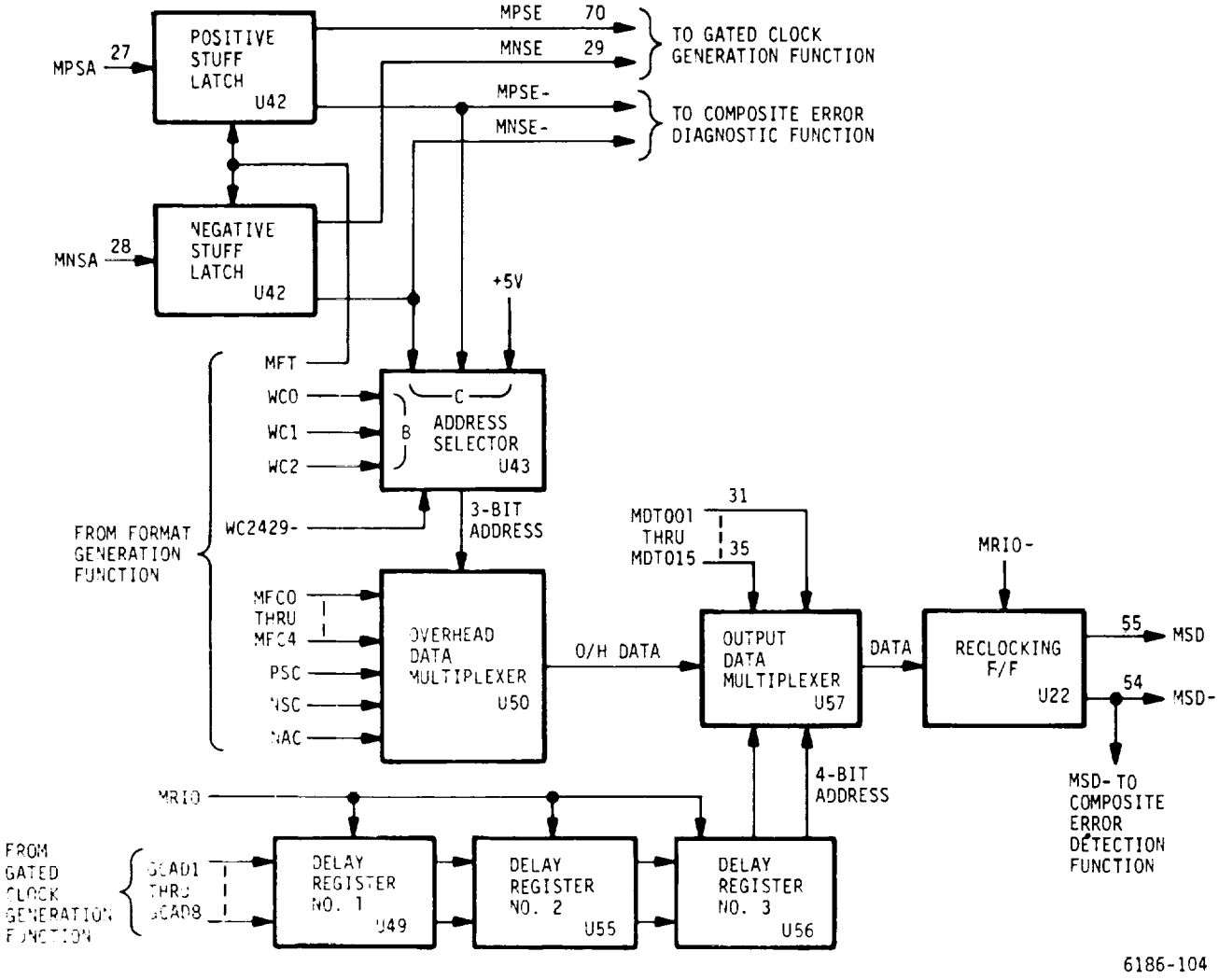


Figure 5-24. GC/DM Card, Data Multiplexer Circuits-Block Diagram

5-324. The overhead data from the overhead data multiplexer are applied to the output data multiplexer during the bit 0 time of each word in the output data format. The total overhead message for one port during a minor frame uses bit 0 in each word in the following format:

Words 1 through 23:	Contain one of three 23-bit synchronization patterns used in the demultiplexer function. Each of the synchronization patterns, in turn, also contains one of the three stuffing codes in the demultiplexer overhead function.
Words 24 through 28:	Contain 5-bit minor frame count for channel identification.
Word 29:	Contains overhead stuff sense bit when a channel is processing a positive stuff code.

5-325. The address selector provides the 3-bit address that selects the overhead data inputs to the overhead data multiplexer. The absence of word count signal WC2429 enables the C input to the address selector during words 1 through 23, and the presence of the signal enables the B input to the address selector during words 24 through 29. The C input provides one 3-bit address code that selects the positive stuff (PSC) code, the negative stuff (NSC) code, or the no-action stuff (NAC) code input that is applied to the overhead data multiplexer. The B input provides the 3bit address codes that sequentially select the inputs that supply 5-bit minor frame count signals MFCO through MFC4 to the overhead data multiplexer. The positive and negative stuff latches provide two bits of the stuff codes applied to the C input of the address selector. The third bit is permanently connected as a 1-bit input. When the need for a positive stuff action is established, positive stuff acknowledge signal MPSA from the OEG card sets the positive stuff latch to produce positive stuff enable signal MPSE, which is routed to the gated clock function, and signal MPSE-, which is applied to the address selector. When a negative stuff action is required, signal negative stuff acknowledge MNSA from the OEG card sets the negative stuff latch to produce negative stuff enable signal MNSE, which is routed to the gated clock function, and signal MNSE-, which is applied to the address selector. When a no-action (no stuff required) condition exists, neither latch is set. Therefore, the overhead data multiplexer sequentially multiplexes the appropriate PSC, NSC, or NAC stuff command, followed by the appropriate minor frame code, to the output data multiplexer.

5-326. Diagnostic Function.

5-327. General. The diagnostic functional circuits monitor the major signals on the card and produce one of two diagnostic error signals (MDM- and MGC-) to the display card when an error condition is detected. The diagnostic function is divided into two parts: the composite error detection circuits, which produce diagnostic data mux error signal MDM-, and the gated clock error detection circuits, which generate diagnostic gated clock error signal MGC-.

5-328. Composite Error Detection Function (Figure 5-25). In normal operation, the minor frame activity detector and the word 29 activity detector produce high-level (no error) signals to OR gate U12. When the minor frame count signal (MFC1) or the word 29 signal (MW29) from the format generation function is missing, the associated activity detector produces a low-level error signal to OR gate U12.

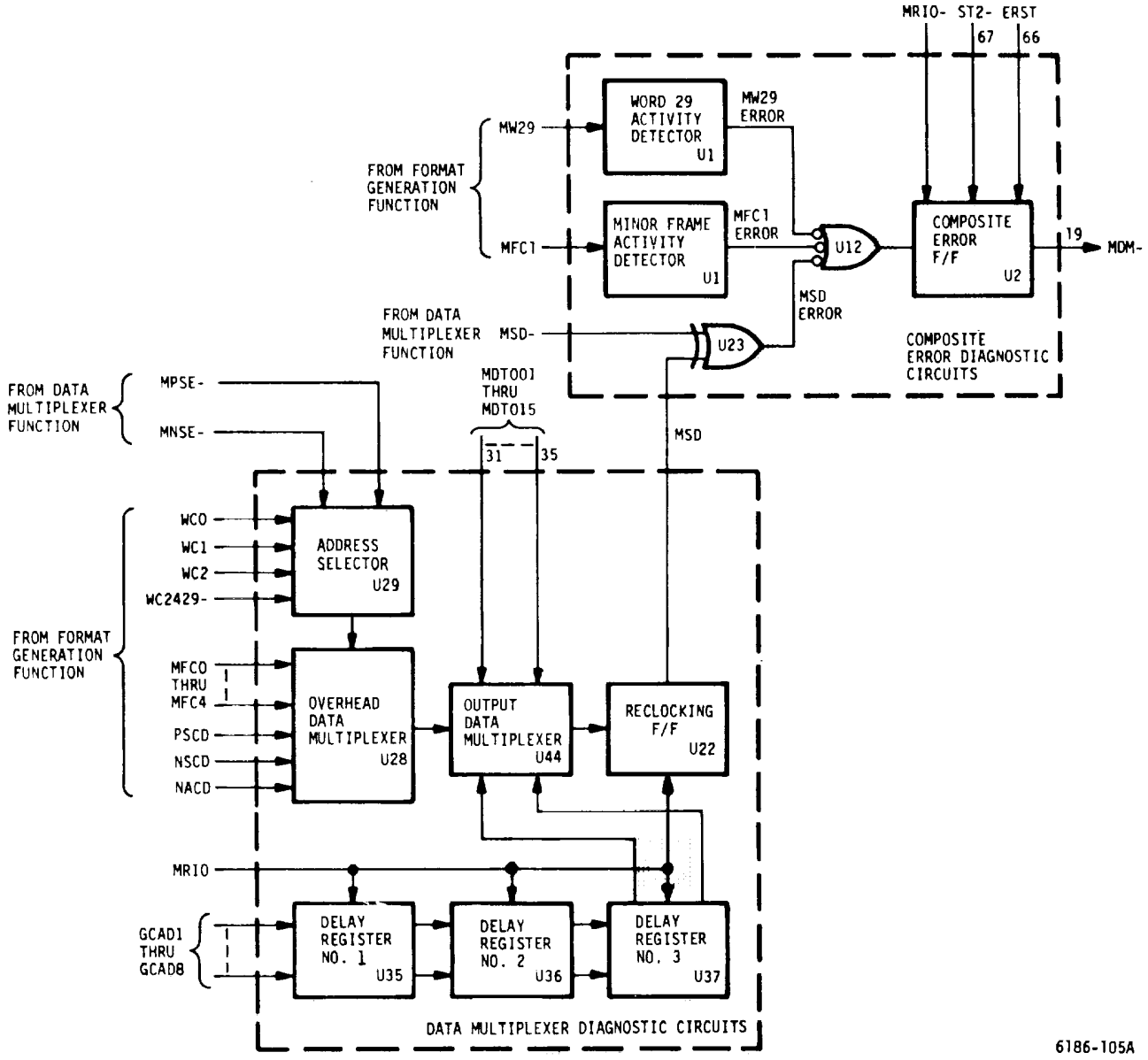


Figure 5-25. GC/DM Card, Composite Error Detection Circuits - Block Diagram

OR gate U12 sets the composite error flip-flop, which generates data mux diagnostic error signal MDM to the display card. Exclusive OR gate U23 effectively compares the MSD output from the functional data multiplexer circuits with the MSD output from the diagnostic data multiplexer circuits. The diagnostic data multiplexer circuits are identical to the functional data multiplexer circuits and produce identical but complementary MSD and MSD signals. Therefore, in normal operation, MSD and MSD are complementary to each other and make exclusive OR gate U23 produce a high-level (no error) signal to OR gate U12. If one of the two inputs to the exclusive OR gate malfunctions, exclusive OR gate U23 produces a low-level error signal so that signal MDM is generated. Self-test signal ST2sets the composite error flip-flop for an error indication when the SELF TEST switch on the front panel is set to the on (up) position. Error reset signal ERST resets the flip-flop when the SELF TEST switch on the front panel is set to the off (down) position or the DISPLAY RESET switch on the front panel is pressed.

5-329. Gated Clock Error Detection Circuits (Figure 5-26). In normal operation, four gated clock comparators sample gated clock signals MGCO1 through MGC15 (A input) from the gated clock generation function against the same signals (B input) generated by the diagnostic gated clock generation circuits. The diagnostic gated clock generation circuits are identical to the functional circuits and produce gated clock signals that normally are identical to those produced by the functional circuits. When a malfunction occurs, a mismatch is detected by one of the four comparators and one of the four A=B inputs to AND gate U9 goes low and sets the gated clock error flip-flop to generate diagnostic gated clock error signal MGC that is applied to the display card. The gated clock error flip-flop can be set and reset by signals ST2and ERST as explained in paragraph 5-328.

5-330. DETAILED CIRCUIT DISCUSSION.

5-331. Format Generation Function.

5-332. The word counter, consisting of flip-flop U5 and binary counter U14, is incremented by end-of-scan signal MEOS2B to produce 5-bit binary word counts WCO through WC4 that address read only memory (ROM) U20. The word counter counts sequentially until it is reset by word count 29 from flip-flop U3-7 in the words 28/29 generator. In the multiplexer function, preset inputs P1 and P2 on binary counter U14 are set to 00 by the application of signal M+5R through inverter U15. This configuration I)resets the word counter to a count of 1 after word 29. In the demultiplexer function, word counter preset signal DWPR is applied one time to inverter U15 when synchronization is initially obtained in the frame sync card. Signal DWPR sets the P1 and P2 inputs on binary counter U14 to 11 and also applies a preset signal through OR gate U4, and inverter U13, presetting the counter to a count of 12. After initial reset in the demultiplexer function, the word counter is preset to a count of 1.

5-333. The ROM is programmed to generate six outputs that are selected by 5-bit word count signals WCO through WC4 applied from the word counter. As shown in table 5-5, the ROM outputs are two identical sets of the three stuffing codes (PSC, NSC, NAC for the functional circuits and PSCD, NSCD, NACD for the diagnostic circuits).

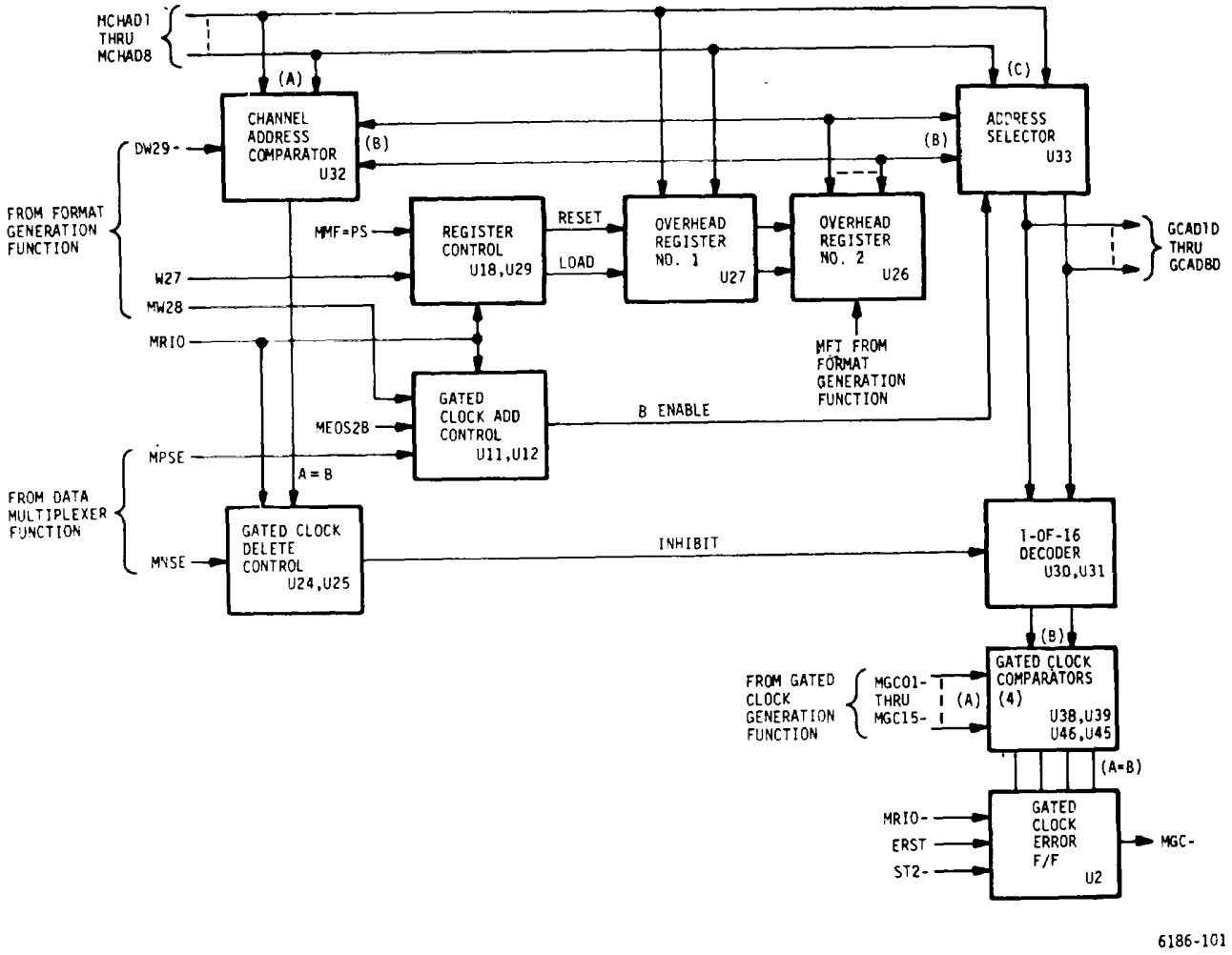


Figure 5-26. GC/DM Card, Gated Clock Generation Diagnostic Circuits - Block Diagram

The codes also contain the synchronization codes that are used in the frame sync card to detect frame synchronization of the incoming serial data stream. The ROM generates one bit from each output during each word. The addresses from the word counter apply sequential addresses in the other shown in table 5-5.

5.-334. The word 27 decoder, consisting of AND gates U15 and U4 and inverters u13 and U21, applies a high level signal, through inverter U13-4 during word 27, to J-K flip-flop U3-5, AND gate U19-3; and AND gate U19-6. The words 28/29 decoder is a two-bit shift register consisting of J-K flip-flops U3-5 and U3-9. when word 27 is applied to U3-5, it is clocked through the two stages by end-of-scan signal MEOS2B to generate words 28 and 29. Word 29 signal MW29 is applied to word 29 activity detector Ul-10 in the composite error detector circuits for diagnostic purposes.

Table 5-5. List of ROM Outputs (Stuff Codes)

DATA WORD (BIT 0 POSITION)

		1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
WORD COUNT INPUTS:	WC0	1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
	WC1	0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1
	WC3	0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1
	WC4	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
STUFF CODE OUTPUTS:		
PSC	Y1, Y4	1 1 0 0 1 1 1 0 1 0 1 1 1 1 1 1 0 1 1 0 1 0 1
NSC	Y2, Y5	1 1 0 0 0 0 0 1 0 1 0 1 1 1 0 0 1 0 1 1 0 1 0
NAC	Y3, Y6	0 0 1 1 0 0 0 0 1 0 1 0 0 0 1 1 0 1 0 1 0 1 0

5-335. Word 29 signal MW29 and end of-scan signal MEOS2B enable AND gate U4-3 to produce the minor frame transition signal MFT. Signal MFT clocks the minor frame counter consisting of flip-flop U5 and binary counter U6. The minor frame counter is incremented by signal MFT until the frame count 31. Signal MMF31, the terminal count from U6, is generated by the binary counter. Signal MFC1 is applied to minor frame activity detector U1-6 in the composite error detector circuits for diagnostic purposes. Multiplexer minor frame count signals MMFCO through MMFC4 are routed to the seq card. Minor frame terminal count signals MMF31A-, MMF31B-, and MMF31Care distributed to channel card locations Al through A15 for use by the RCB cards.

5-336. Minor frame count signals MFCO through MFC4 from minor frame counter U5, U6 are applied to overhead data multiplexer U50 to identify the used port that is receiving overhead service in the minor frame being addressed at any given time.

5-337. Gated Clock Generation Function.

5-338. Channel address signals MCHADO through MCHAD8 from the sequencer card contain the address of the active channel selected to receive a gated clock signal. The channel address signals are applied at the multiplexer clock rate (MRIO) to the inputs of overhead register No. 1 (U48) and to the C input of address selector U53. In normal operation, AND gate U12-6 in the gated clock control circuit is inhibited by the absence of MPSE. This condition sets flip-flop U11 in the gated clock add control circuit to generate an enable signal to the C input of U53.

In this state, the applied channel address signals are routed directly through U53 to the inputs of 1-of-16 decoder U51, U52. The l-of-16 decoder contains two 1-of8 decoders that decode the four-bit channel address into the appropriate gated clock signal (MGCO1 through MGC15) representing the selected channel address. In this normal operating configuration, one gated clock signal is generated for each channel address clocked into the circuits.

5-339. overhead service for a given channel address is initiated when minor frame equals port sequence signal MMF=PS is applied to U18-5 in the register control circuit. Signal MMF=PS from the sequencer card is only applied to U18-5 during word 28 of each minor frame that services a used port. During word 27, signal W27 and end-of-scan signal MEOS2B initiate the master reset signal from AND gate U19-3 in the register control circuit. The master reset signal, in turn, resets the output from overhead register No. 1 (U48) to 0000 in word 27 of each minor frame period. The output from U48 remains 0000 during each minor frame period not assigned to service a used port. When signal MMF=PS is generated, a load signal is applied to overhead register No. 1, and the channel address (MCHADO through MCHAD8) applied to the card is loaded into overhead register No. 1.

5-340. The output from overhead register No. 1 (U48) is applied to overhead register No. 2 (U54) and to the OEG card as overhead address count signals MOHO through MOH3. The channel overhead address count signals interrogate the OEG card to see if the selected channel is requesting one of the three overhead service conditions: positive stuff, negative stuff, or no action. The OEG card, in turn, applies signal MPSE for a positive stuff condition, signal MNSE for a negative stuff condition, or neither signal to indicate a no-action condition. When a channel address is applied to the GC/DM card during a minor frame period associated with an unused port, signal MMF=PS is not generated, and the channel address from overhead register No. 1 remains 0000. Channel address 0000 on the OEG card is an inactive channel; therefore, a no action condition is reflected back to the GC/DM card. Signal MPSE or signal MNSE is never applied to the GC/DM card in response to channel address 0000. The channel address in overhead register No. 1 is clocked into overhead register No. 2 (U54) by minor frame transition signal MFT. Signal MFT is generated from AND gate U4-3 when signals MEOS2B and MW29 are applied to the AND gate. The channel address clocked into overhead register No. 2 is applied to the B input of channel address comparator U47 and to the B input of address selector U53.

5-341. When a positive stuff action is designated for the channel address being interrogated on the OEG card, signal MPSE is applied to U12-6 in the gated clock add control circuit. Signal MPSE, together with signals MEOS2B and word 28 (from flip-flop U3-5) enable AND gate U12-6 so that flip-flop U11, in turn, generates the B enable signal to address selector U53. The B enable signal enables the B input of U53 so that overhead address stored in overhead register No. 2 (U54) is applied to 1-of-16 decoder U51, U52. The 1-of-16 decoder, in turn, generates one additional gated clock signal during bit 0 of word 29 for the active channel address designated for the positive stuff bit.

5-342. When a negative stuff action is designated for the channel address being interrogated on the OEG card, signal MNSE is applied to AND gate U24-12 in the gated clock delete control circuit. When signal MFT occurs, the channel address being interrogated on the OEG card is applied through overhead register No. 2 (U54) to the B input of channel address comparator U47.

During word 29, the comparator is enabled and output signal A=B is produced when the incoming channel address matches the overhead channel address applied to the B input of the comparator. Signal A=B and signal MNSE are applied to AND gate U24-12. The output from flip-flop U25 to AND gate U24 is high for one multiplexer clock time (MRIO). AND gate U24, in turn, generates an inhibit to AND gate U16-11 for one clock time. This condition causes a high-level inhibit signal to 1-of-16 decoder U51, U52, preventing one gated clock signal from being generated for the designated channel address. Flip-flop U25 is configured so that only one signal A=B can enable AND gate U24-12 in word 29 of a minor frame. Otherwise, other used ports strapped to the selected active channel could also develop a negative stuff condition when the redundant channel address appears and is compared with the channel address applied to the B input of channel address comparator U47.

5-343. Data Multiplexer Function.

5-344. Output data multiplexer U57 combines up to 15 channels of output data (MDT001 through MDT015) from the active channels in the multiplexer, together with one overhead data channel input from overhead data multiplexer U50. Channel addresses GCAD1 through GCAD8 from address selector U53 sequentially select the data inputs to output data multiplexer U57. Channel addresses GCAD1 through GCAD8 are routed through delay registers No. 1, No. 2, and No. 3 (U49, U55, and U56) to the multiplexer. The three registers provide a time delay that is equal to three multiplexer clocks (MRIO) to compensate for the time delay in the data TTL circuit applications. The channel addresses applied from U56 to data output multiplexer U57 sequentially select one overhead data bit from overhead multiplexer U50 and one bit from each of the channel data inputs (MDT001 through MDT015) applied from the active channel cards. The single serial data stream from multiplexer U57 is applied through inverter U13-12 to reclocking flip-flop U22. Complementary serial data streams MSD and MSD are clocked out of U22 at the multipliexer clock MRIO rate. Signal MSD is routed to the reference timer card and signal MSD is applied to the composite error detection function.

5-345. Overhead data multiplexer U50 combines the overhead data inputs for a selected port into the serial overhead data format that is applied to one input of output data multiplexer U57 during bit 0 of words 1 through 28 in each minor frame period. The serial overhead data contains one of the three stuff command signals (PSC, NSC, and NAC) in bit 0 of words 1 through 23 of each minor frame. Bit 0 of words 24 through 28 of each minor frame contains the 5-bit binary code for the port receiving overhead service during a given minor frame. Positive stuff command signal MPSA and negative stuff command signal MNSA from the OEG card are applied through three AND gates U34 to positive stuff latch U42-10 and negative stuff latch U42-6. At the end of each minor frame, the selected stuff command is clocked into the appropriate latch by minor frame transition signal MFT from AND gate U4-3. When a positive stuff condition is initiated, latch U42-9 produces signal MPSE, which is applied to U12-6 (pin 70 strapped to pin 89) in the gated clock generation circuits, and U49-10 produces signal PSE-, which is applied to the C input of address selector U43. Initiation of a negative stuff generates signal MNSE from latch U42-7, which is applied to U24-12 (pin 29 strapped to pin 87) in the gated clock generation circuits, and U42-6 produces signal NSE-, which is applied to the C input of address selector U43.

For a no action condition, neither signal MPSA nor MNSA is generated. Therefore, signals MNSE and MPSE are not generated and signals PSE and NSE are high-level inputs to the C input of address selector U43.

5-346. The absence of word count signal WC2429enables the B input of U43 during words 1 through 23. During words 1 through 23, one 3-bit stuff command code is applied through U43 to the data select inputs of overhead data multiplexer U50. The 2-bit stuff code enables the data inputs at pin 6, 7, or 9 so that the appropriate stuff code (NAC, NSC or PSC) is routed through multiplexer USO0 to input IO of output data multiplexer U57. The 3-bit binary stuff command codes that can be applied during words 1 through 23 are shown below.

5-347. Word count signal WC2429enables the B input of U43 during words 24 through 29. Five sequential binary addresses derived from word count signals WC0, WC1, and WC2 are applied through the B input of U43 to the data select inputs of overhead data multiplexer U50. The WCO, WC1, and WC2 codes applied during words 24 to 29 are 000 (enables pin 1 on U50) through 101 (enables pin 5 on U50). Minor frame count signals MFCO through MFC4 from minor frame counter U5, U6 are applied in reverse order to input pins 1 through 5 of U50. The most significant digit (signal MFC4) is applied to pin 1 (first bit sampled), and the least significant digit (signal MFCO) is applied to pin 5 (last bit sampled). The reverse binary code read out of US0 during bit 0 of words 24 through 28 identifies the used port being serviced during the minor frame identified in the frame count signals at the output of counter US, U6. For example, minor frame 3 (count 00011 from U5, U6) services port 24 (count 11000 from U50).

5-348. Diagnostic Function.

5-349. Composite Error Detection Circuit. A low-level input to any one of the three inputs to OR gate U12-8 places a high-level signal to the input of error flip-flop U2. The flip-flop, in turn, produces data mux diagnostic error signal MDM- when the next multiplexer clock signal MRIO- clocks the flip-flop. Two of the inputs to OR gate U12 are provided from word 29 activity detector U1-10 and from minor frame activity detector U1-6. Both activity detectors are retriggerable multivibrators that are held in conduction by the word 29 signals (MW29) or minor frame signals (MFC1). When the signal is missing, the stage will complete its duty cycle and produce a low-level error signal to OR gate U12. The third input to OR gate U12 is from exclusive OR gate U23-6, which samples signal MSD from the functional data multiplexer circuit and diagnostic signal MSD from the diagnostic equivalent circuits. When a malfunction occurs, signals MSD and MSD- will eventually compare and cause the exclusive OR gate to generate a low-level error signal to OR gate U12.

Signal to Latch U42	3-Bit Address Code to U50 From U43			Stuff Input to U50
	S0	S1	S2	
MPSA (positive stuff)	1	0	1	Pin 6 (PSC)
MNSA (negative stuff)	0	1	1	Pin 7 (NSC)
Neither (no action)	1	1	1	Pin 9 (NAC)

5-350. Gated Clock Error Generation Circuit. The gated clock error generation circuit consists of four 8input comparators U45, U38, U46, and U39 that provide four A=B outputs to AND gate U9-8, which, in turn, provides a signal to the input of gated clock error flip-flop U2. When the 15 gated clock outputs (MGCO1 through MGC15) from function 1-of-16 decoder U51, U52 compare with the gated clocks from the diagnostic 1-of-16 decoder U30, U31, four high-level signals A=B hold AND gate U9-8 in conduction so that a low-level signal is applied to the input of flip-flop U2. When one or more of the functional gated clocks in one of the comparators do not compare with the diagnostic gated clocks, the A=B output goes low and inhibits AND gate U9. In turn, AND gate U9 places a high to the input of flip-flop U2 so that gated clock error signal MGC is produced the next time signal MRI0-clocks the flip flop. Both error flip-flops U2-6 and U2-7 can be set to the self-test state by self-test signal ST2and can then be reset by signal ERST.

5-351. OVERHEAD ENABLE GENERATOR OEG CARD.

5-352. GENERAL.

5-353. The OEG card is one of the common cards. Two OEG cards are used in the multiplexer set: one in the multiplexer and one in the demultiplexer. The block diagram for the circuits described in the block diagram discussion is shown in figure 5-27. The logic diagram associated with the detailed circuit discussions is contained in the circuit diagrams manual.

5-354. In the multiplexer, the OEG card performs three functions. First, the OEG card accepts positive and negative stuffing requests from the active channel cards and then multiplexes the positive stuffing requests into one positive stuff acknowledge output stream, and the negative stuff requests into one negative stuff acknowledge output stream. The two serial output streams are routed to the GC/DM card for overhead servicing. During word 24 the positive stuff acknowledge stream contains the diagnostic status for the channel cards. This data is routed to the display card as part of the diagnostic function during word 24. Second, system clock signal $_{R0}$ from the reference timer card is applied to the OEG card, which then redistributes the signal as multiplexer system clock signals MRIO1through MRI08to other cards in the multiplexer. Third, the OEG card generates word 24, word 24 end of scan 2, word 24 bit 0, and end-of-scan (EOS) signals by decoding signals from the word counter and end-of-scan logic. The signals are then routed to the channel cards and to the display card for timing purposes.

5-355. In the demultiplexer, the negative stuff request circuits are not used on the OEG card. The positive stuff request lines are used only for the diagnostic data required for the diagnostic function on the display card.

5-356. BLOCK DIAGRAM DISCUSSION.

5-357. In the multiplexer, positive stuff request signals MPST01through MPST15from the channel cards are applied through the ON positions of the DIAGNOSTICS AND OVERHEAD switches to positive stuff multiplexer No. 1 Negative stuff request signals MNST01through MNST15are applied to negative stuff multiplexer No. 1.

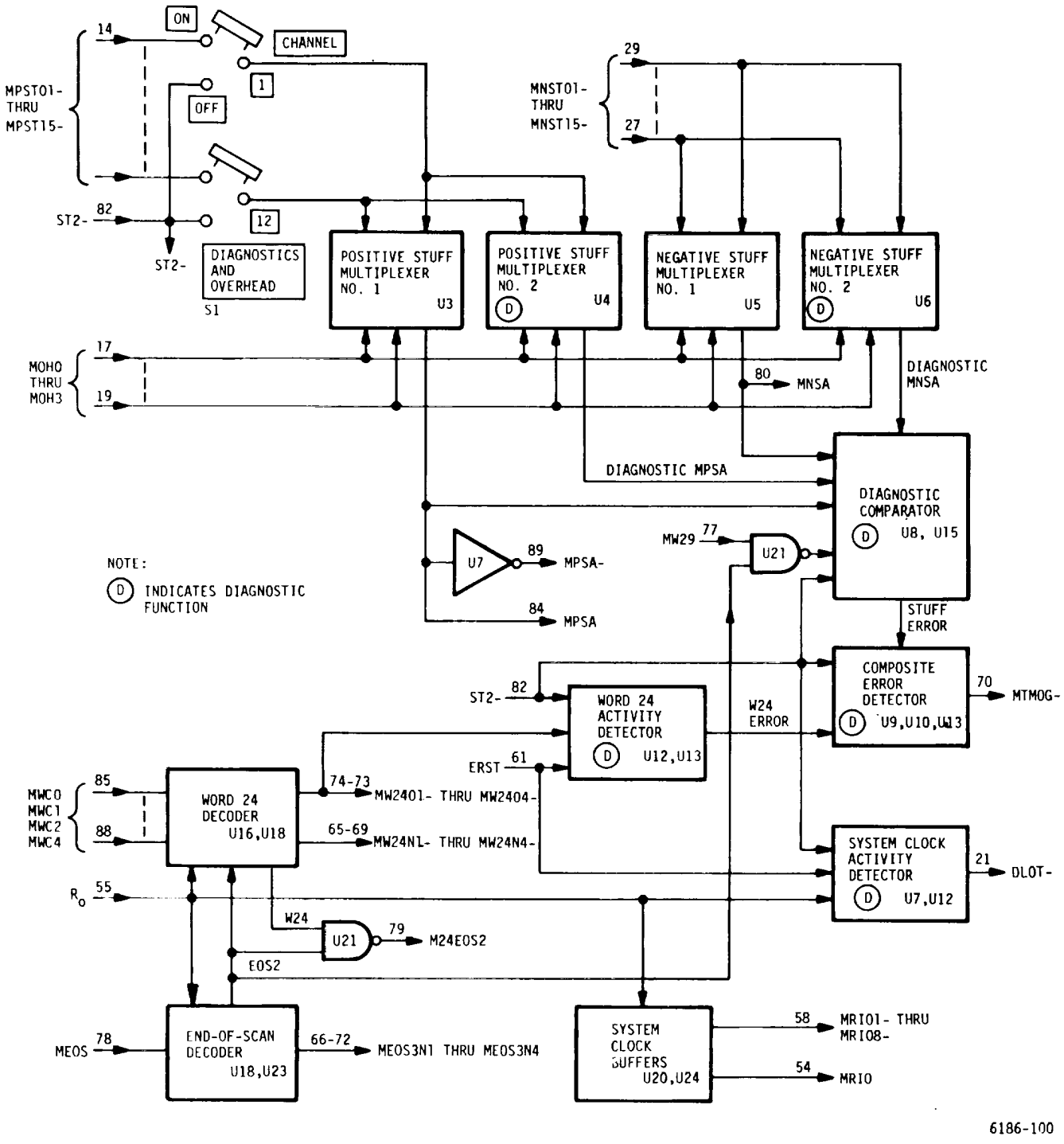


Figure 5-27. OEG Card - Block Diagram

Overhead address count signals MOH0 through MOH3 from the GC/DM card contain the 4-bit channel addresses that select the one channel to be interrogated in both multiplexers during each minor frame. Positive and negative stuff acknowledge signals MPSA and MNSA from the two multiplexers are routed back to the GC/DM card as part of the overhead function. Positive stuff acknowledge signal MPSA from positive stuff multiplexer No. 1 is routed to the display card, where the signal is interrogated for diagnostic error data during word 24. Self-test signal ST2 is applied through the OFF positions of the DIAGNOSTICS AND OVERHEAD switches to the inactive channel inputs of positive stuff multiplexers No. 1 and No. 2 to prevent false diagnostic error indications during the self-test mode.

5-358. The word 24 decoder generates word 24 signals when word count signals MWC0, MWC1, MWC2 and MWC4 from the GC/DM card are a count 23 and end of-scan signal EOS2 from the end-of scan decoder is generated. The output signals from the decoder are word 24 signals MW24N1through MW24N4 and word 24 bit 0 signals MW2401through MW2404-. The output signals are applied to the channel cards and to the frame sync card. Word 24 end-of-scan signal M24EOS2 from AND gate U21 is generated and routed to the display card when the two decoder circuits generate word 24 and EOS2.

5-359. The end-of-scan decoder generates end-of-scan signals EOS2, and EOS3 that represent two levels of the end-of-scan signal. Each sequential EOS signal is separated in time by one R clock time. Signal EOS2 is applied to AND gate U21 and to word 24 decoder as an enable signal. End-of scan signals MEOS3N1 through MEOS3N4 generated by the decoder are routed to the channel cards.

5-360. System clock signal R_o is applied through system clock buffers and is distributed as system clock signals MRIO1through MRI08to the channel cards. Clock signal MRIO is also derived from signal R_o and is applied to the GC/DM and sequencer cards.

5-361. Positive stuff multiplexer No. 2 and negative stuff multiplexer No. 2 are part of the diagnostic function. The two multiplexers duplicate the outputs of positive and negative stuff multiplexers No. 1. Diagnostic stuff acknowledge MPSA and MNSA signals from the two diagnostic multiplexers are applied to the diagnostic comparator, where they are compared with the functional MPSA and MNSA outputs. When the output signals being compared are not alike, the diagnostic comparator generates a stuff error signal to the composite error detector. The composite error detector, in turn, generates OEG card diagnostic signal MTMOG as described in paragraph 5-364.

5-362. The system clock activity detector monitors system clock signal R_o and generates diagnostic loss-of timing error signal MLOT when the signal is missing. Once the error condition is detected, signal MLOT is applied to the display card until the DISPLAY RESET switch on the front panel is pressed. When the switch is pressed, reset signal ERST is applied to the detector. If the malfunction is corrected, the detector returns to its no-error state. When the SELF TEST switch on the front panel is set to the on (up) position, self-test signal ST2is applied to the card and the detector is set to its error position until the SELF TEST switch is returned to the off (down) position. When the SELF TEST switch is set to the off (down) position, reset signal ERST is automatically applied to the card and the detector is reset to its no-error state.

5-363. The word 24 activity detector monitors the word 24 output from the word 24 decoder and generates a word 24 error signal to the composite error detector when either the word 24 decoder or end-of-scan decoder signals are missing. The detector can be set or reset by signal ST2 or ERST as explained in paragraph 5-362.

5-364. The composite error detector generates OEG card diagnostic signal MTMOG to the display card when a stuff error or W24 error signal is applied. Once the error input to the detector is removed, the detector output returns to its no-error state. The detector circuits can be set to the error state by self-test signal ST2- as explained in paragraph 5-362.

5-365. DETAILED CIRCUIT DISCUSSION.

5-366. In certain unique system configurations, a channel may possibly be active but not have a channel card installed. Therefore, the 15 DIAGNOSTICS AND OVERHEAD switches (S1) are provided on the OEG card to prevent false channel card diagnostic error signals when the multiplexer is in the self-test mode. The switch is set to the ON position for each active channel that has a channel card installed. In turn, the switch associated with each active channel not having a channel card installed is set to the OFF position. Settings of switches associated with inactive channels may be in the ON or OFF positions, since inactive channels are not sampled. In the self-test mode, each channel input to positive stuff multiplexer U3 that has the switch in the ON position receives the diagnostic error status from the associated channel card. Each channel card input to multiplexer U3 that has the switch set in the OFF position receives a low-level self test signal ST2in the self-test mode, and a high-level no-error signal in normal operation. A low-level diagnostic signal input to multiplexer U3 is processed as a no-error condition in the overhead diagnostic function. Without the DIAGNOSTICS AND OVERHEAD switching capability, an active channel not fitted with a channel card would yield a high-level error signal, which would be applied to the channel input of multiplexer U3 to indicate a faulty diagnostic-error condition during the self-test mode. Setting the appropriate DIAGNOSTICS AND OVERHEAD switches to the OFF positions for these channels prevents an undesirable self-test condition.

5-367. Positive stuff request signals MPSTO1through MPST15from the active channels in the multiplexer are applied through the ON positions of the switches (S1) to inputs on positive stuff multiplexer No. 1 (U3). Overhead address count signals MOHO through MOH3 select the multiplexer channel that is interrogated and multiplexed into a single positive stuff output data stream as positive stuff acknowledge signal MPSA. Signal MPSA is routed to the GC/DM card. The signal is also applied to exclusive OR gate U8-6 in the diagnostic comparator circuit. As part of the card diagnostic function performed during word 24, signal MPSA is applied through .inverter U7-3 and is routed as signal MPSA to the display card. Negative stuff request signals MNSTO1through MNST15are processed through negative stuff multiplexer No. 1 (U5) to generate a single negative stuff output data stream as negative stuff acknowledge signal MNSA. Signal MNSA is routed to the GC/DM card.

5-368. Signals MPSA and MNSA are compared in the diagnostic comparator circuit with their equivalent diagnostic MPSA and MNSA signals from positive and negative stuff multiplexers No. 2 (U4 and U6). The compare function is performed by four exclusive OR gates (U8). When an error condition is detected (mismatch), the exclusive OR gates cause flip-flop U15 to generate a high-level Q output which, in turn, causes OEG card diagnostic signal MTMOG- to be generated from OR gate U13-4 in the composite error detector circuit.

5-369. System clock signal R_o from the reference timer card is applied through a series of inverters (U20 and U24) to produce system clock signals MRIO and MRIO1through MRI08-. Retriggerable one-shot multivibrator U12-10 in the system clock activity detector circuit is held in conduction by signal R_o. When R_o is missing, the one-shot multivibrator's duty cycle expires and its output sets latch U7, which, in turn, generates loss of timing signal DLOT- that is applied to the display card. The latch remains set until reset signal ERST is applied when the DISPLAY RESET switch on the front panel is pressed.

5-370. When word count 23 is applied to AND gate U16-6 by word count signals MWC0, MWC1, MWC2, and MWC4, and end-of-scan signal EOS2 from U23-5 is applied to clock flip-flop U18-6, the word 24 signal is generated. The word 24 signal is buffered and distributed through inverters U14 and U19 as word 24 signals MW24N1through MW24N4- to the channel cards. The output from U18-6 is also applied to AND gate U21-11, which, in turn, produces signal M24EOS2 when end-of-scan signal EOS2 is applied at its other input from flip-flop U23-5 during word 24. AND gate U16-8 also produces a word 24 output when the word 24 output from U18-6, EOS3 from U18-7, and R_o are present. The pulsed output from AND gate U16-8 is applied to the four U22 inverters to produce word 24 bit 0 signals MW2401through MW2404-. These signals are also routed to the channel cards.

5-371. End-of-scan signal MEOS is clocked through two stages of flip-flop U23 by R to generate end-of-scan + 2 bits signal EOS2 for U18-6 in the word 24 detector circuit. Signal EOS2 is also clocked through U18-9 to produce end-of-scan +3 bits signal EOS3. Signal EOS3 from flip-flop U18-9 is buffered through the three U19 inverters and inverter U22 to produce end-of-scan 3 signals MEOS3Nl through MEOS3N4 for the channel cards.

5-372. Setting the SELF TEST switch on the front panel to the on (up) position applies self-test signal ST2to the card. Signal ST2- inhibits retriggerable multivibrator U12-7 in the word 24 activity detector circuit, which sets latch U13 so that a high level error signal is applied to AND gate U9-8 in the composite error detector circuit. Retriggerable multivibrator U12-10 in the system clock activity detector circuit is also inhibited by ST2- so that latch U7 is set to produce diagnostic loss of timing error signal DLOT-. In the self test mode, during word 24, all the active inputs to the four multiplexers are low. Signal ST2- is applied through the three U11 inverters and the OFF positions of DIAGNOSTICS AND OVERHEAD switch S1 to place a low level signal on each of the unused inputs of the two positive stuff multiplexers. This configuration ensures a continuous high input to each of the four exclusive OR gates (U8) in the comparator circuit. Signal ST2- places a high-level signal to one input of exclusive OR gates U8-3 and U8-11. The result is a high-level error signal from J-K flip-flop U15-7 in the comparator circuit to AND gate U9-8 in the composite error detector circuit. The three high-level inputs to AND gate U9 result in the generation of low-level OEG card diagnostic signal MTMOG from OR gate U13-4 in the composite error detector circuit. Reset signal ERST is applied to the card when the SELF TEST switch on the front panel is set to the off (down) position or the DISPLAY RESET switch on the front panel is pressed. Signal ERST resets the two diagnostic latch circuits (U7 and U13) and forces J-K flip-flop U15-7 to reset and return the diagnostic circuits to their functional no-error state, assuming that there are no malfunctions on the card.

5-373. REFERENCE TIMER (RT) CARD.

5-374. GENERAL. The reference timer card is one of the common cards used in the multiplexer. The card generates system clock signal R_o that is applied to the OEG card, which, in turn, duplicates and distributes the master clock signal as multiplexer clock signal MRIO to the multiplexer cards. The card accepts the multiplexed serial digital data (MSD) from the GC/DM card, develops the multiplexer timing out signal TIMOUT, and clocks the associated timing data and timing pulses from the card at the selected R_o rate. Timing signals T3600 and T4800, generated on the card, are routed to the transition encoder cards in the multiplexer. The block diagram for the circuits described below are shown in figures 5-28 and 5-29. The logic diagram associated with the detailed circuit discussion is contained in the circuit diagrams manual.

5-375. BLOCK DIAGRAM DISCUSSION.

5-376. System clock signal R_o is developed from external multiplexer timing signals (TIMIN) that are applied to the line receiver circuits (figure 5-28) or from a master oscillator on the card. The input to be used for developing R_o selected by strapping switch S5 to its INT or EXT position. The signals through S5 are applied to the 15-stage binary counter and to the loss-of-timing activity detector. Switch S6 is strapped to position 1 (output of S5) when the selected R_o is the same frequency as the source frequency. The switch is strapped to one of the positions 2 through 16 when the R_o selected is a binary quotient of the source frequency. Signal R_o through S6 is applied to the system clock buffer and to the phase-adjust circuit. The R_o output from the buffer is applied to the data retiming flip-flop, system clock activity detector and to the OEG card. The phase adjust circuit contains a factory adjustment (S3) that phases the timing output signals (TIMOUT and TIMOUT-) to the serial digital data outputs (SDATAO and SDATAO-). The data and timing output signals from the line switches can be applied to a balanced or unbalanced line. When the system is used in a balanced configuration, the output data and timing line switches are set so that the two data signals and the two timing signals are applied to balanced lines. When the system is used in an unbalanced configuration, the output data and timing line switches are set so that the SDATAO and TIMOUT-signal outputs are inhibited by connecting their output pins to ground.

5-377. The timing error detectors monitor the TIMOUT and TIMOUT-output voltages, and detectors generate a diagnostic error signal to the composite OR gate and latch circuits when a malfunction is detected. The composite OR gate and latch circuits also have error signal inputs from the 3600Hz and 4800-Hz activity detectors in the transition encoder timing circuits on the card. The five diagnostic error inputs are ORed together, and when any one of the inputs contains an error condition, the error signal sets the latch circuit to generate reference timer diagnostic signal MRT that is applied to the display card. The loss of-timing activity detector error output is set when the timing signal through S5 is missing. Reset signal ERST resets the error detection circuits back to their no-error state when the DISPLAY RESET switch on the front panel is pressed. Diagnostic signals MLOT and MRT are produced to represent error conditions when the SELF TEST switch on the front panel is set to the on (up) position and self test signal ST2is applied to the error detection circuits.

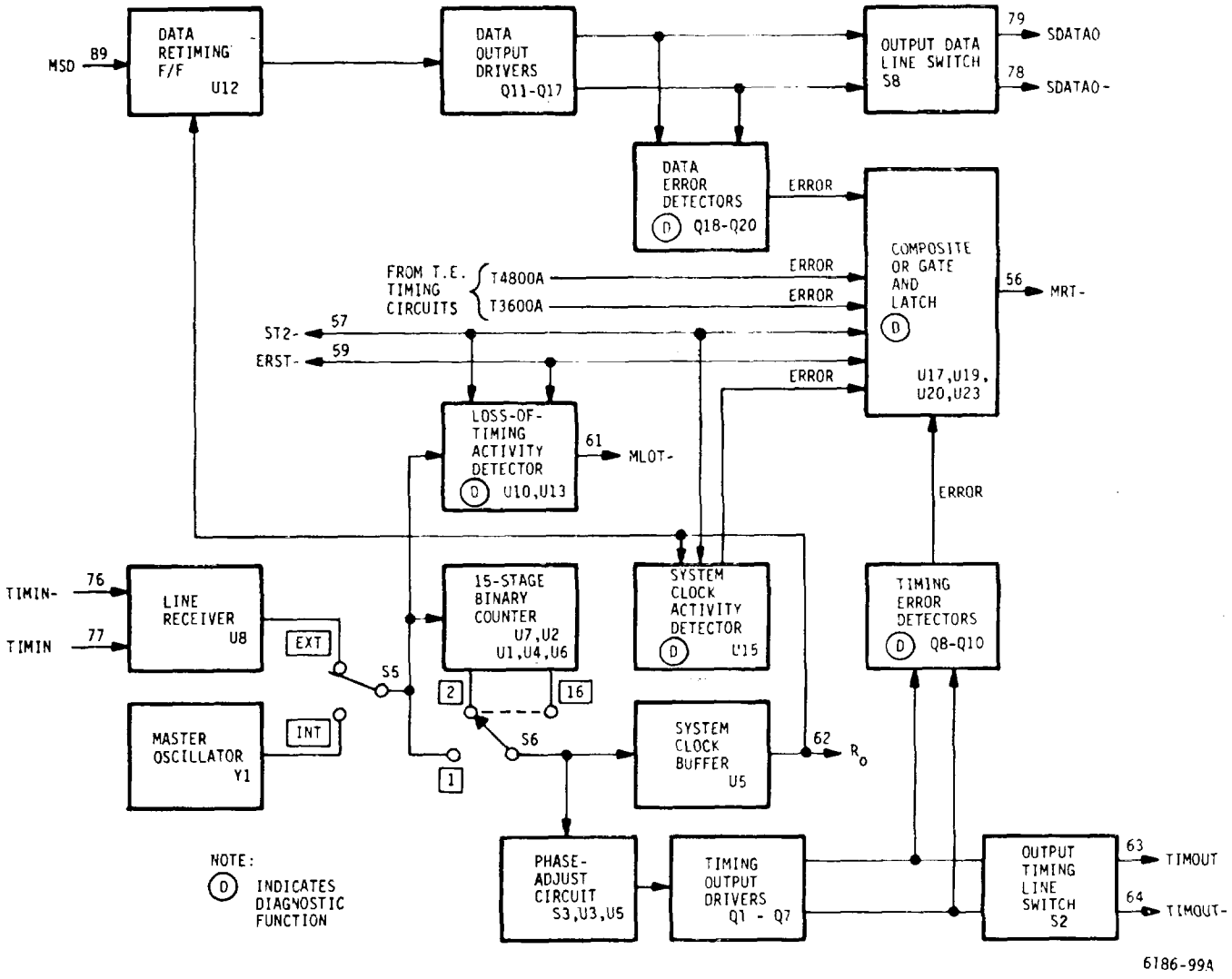


Figure 5-28. RT Card, Data and Timing Circuits - Block Diagram

Setting the SELF TEST switch to the off (down) position applies reset signal ERST to the circuits and forces them to their no-error state.

5-378. The transition encoder timing circuits (figure 5-29) generate timing signals T3600 (3600 Hz) and T4800 (4800 Hz) that are used by the TE/TR channel cards in the multiplexer. The timing oscillator generates a 1.8432MHz (±0.01 percent) timing signal that is applied to an eight-stage $\div 2^n$ binary counter. The N=8 (7.2 kHz) output from the counter is applied to the divide-by-two counter, which, in turn, supplies the 3600-Hz timing signals to the 3600-Hz distribution buffers. The distribution buffers produce 3600-Hz timing signals T3600A, T3600B, and T3600C that are routed to the channel card locations.

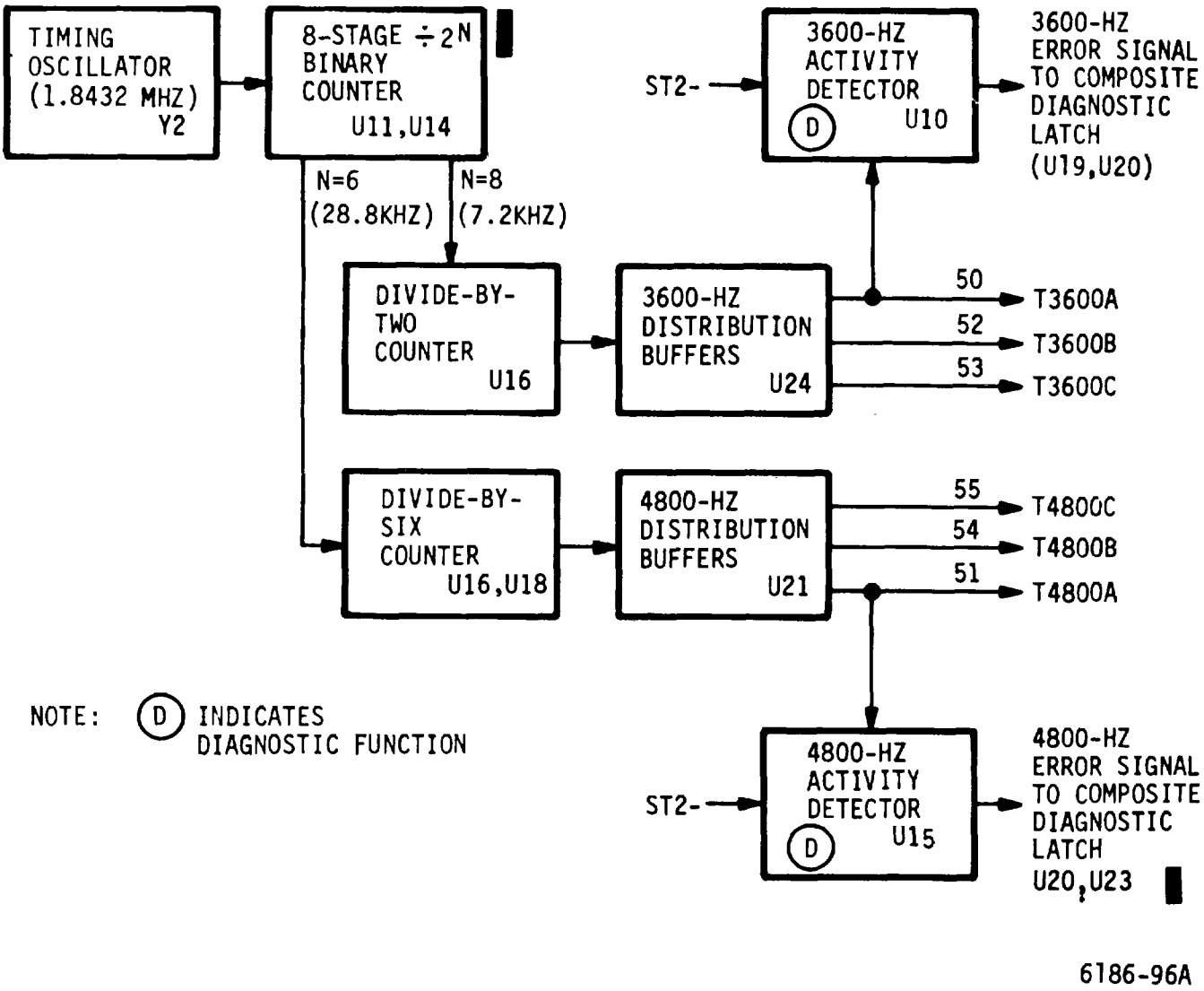


Figure 5-29. RT Card, Transition Encoder Timing Circuits - Block Diagram

The N=6 (28.8 kHz) output from the eight-stage ÷ N binary counter is applied to the divide-by six counter, which, in turn, supplies the 4800-Hz timing signals to the 4800-Hz distribution buffers. The distribution buffers produce 4800-Hz timing signals T4800A, T4800B, and T4800C that are routed to the channel card locations. The 3600-Hz and 4800Hz activity detectors sample the timing signals and generate diagnostic error signals to the composite OR gate and latch circuits on the card when timing signals T3600A and T4800A are missing. The two activity detector circuits are set and held in the error state by self-test signal ST2 when the SELF TEST switch on the front panel is set to the on (up) position. When the SELF TEST switch is set to the off (down) position, signal ST2 is removed and the activity detector circuits return to their no-error state.

5-379. DETAILED CIRCUIT DISCUSSION.

5-380. Timing Circuits.

5-381. System clock signal R_o is developed from timing signals TIMIN and TIMIN-, which are applied from an external source, or R_o is developed from timing oscillator Y1 on the card. Selection of the timing source is made by strapping switch S5 to its EXT or INT position. The oscillator is a plug-in module that provides one base frequency selected for a given system application. The oscillator or the external timing input frequency is selectable within the range of 155 Hz to 10 MHz. However, the 15-stage binary counter permits a source signal within the range of 5 MHz to 10 MHz to cover all of the desired frequencies within a given system configuration. When the external source is used, the TIMIN and TIMIN signals are applied to differential line receiver U8. The line receiver processes the incoming digital timing signals into TTL logic levels, which, in turn, are applied to switch S5. The signals through S5 are applied to the first stage of the 15 stage binary counter, to switch position S6-1, and to one-shot multivibrator U10 in the loss-of-time activity detector.

5-382. The timing signals through switch S5 are routed through inverter U3 to J-K flip-flop U1 in the 15-stage binary counter. The four J-K flip-flops (U1, U4) perform a high-speed divide-by-16 of the incoming timing signals to provide outputs to pins 2 through 5 of switch S6. Four-bit binary counters U6, U7, and U2 perform divide-by-32 through divide-by-32768 of the incoming timing signals to provide outputs to pins 6 through 16 on switch S6. The timing output signal strapped through switch S6 is system clock signal R_o that is applied to inverter U3 in the phase-adjust circuit. Signal R_o is also routed through inverters U5, which perform a buffer function, to the OEG card.

5-383. Switch S3 in the phase-adjust circuit is factory preset. The switch is set so that timing out signals TIMOUT and TIMOUT are in phase with the serial digital data output pulses (MSD) as shown in figure 5-30. The timing signals from the phase-adjust circuit are applied through polarity switch S1 to amplifiers Q1 and Q2 in the timing output drivers circuit. Polarity switch S1 is used in system configurations to change the polarity of the timing pulses with respect to the digital data pulses. Transistor Q3 is a constant current source for amplifiers Q1 and Q2. Amplifiers Q1 and Q2 in turn, drive push-pull emitter-followers Q4 through Q7. Setting switch S2 to the balanced position (B) connects breakdown diodes VR2 and VR4 (2.4 vdc) in parallel with breakdown diodes VR3 and VR5 (5.6 vdc) in the base circuit of emitter-followers. This balanced configuration produces balanced +3-volt TIMOUT and TIMOUT signals. Switch S2 in the unbalanced position (U) connects only breakdown diodes VR3 and VR5 into the base circuit of the emitter-followers so that a +6-volt TIMOUT signal is generated and TIMOUT signal output from the card is grounded. Diodes CR2 and CR3 in the collector circuits of Q1 and Q2

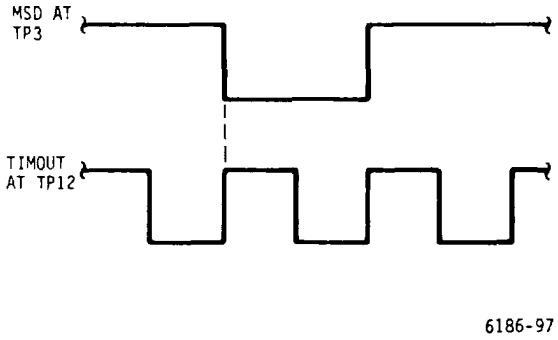


Figure 5-30. RT Card, Reference Timing - Waveform Diagram

provide sharp cutoff and turn-on characteristics for the push-pull emitter followers.

5-384. The RC time constant of retriggerable one-shot multivibrator U10 in the loss-of-timing activity detector is long enough that the continuous timing pulses through S5 can hold the stage in conduction. When the timing signals are interrupted, U10 completes its duty cycle and its output sets latch U13. Setting latch U13, in turn, produces diagnostic loss-of-timing error signal MLOT that is applied to the display card. Self-test signal ST2- is applied to set latch U13 when the SELF TEST switch on the front panel is set to the on (up) position. Reset signal ERST to the latch circuit is applied when the SELF TEST switch is set to the off (down) position. Signal ERST is also generated when the DISPLAY RESET switch on the front panel is pressed and then released. When error signal MLOT is generated, the LOSS OF MUX TIMING indicator on the front panel lights and remains lighted until signal MLOT- is removed.

5-385. Transistors Q8 and Q9 in the timing error detector circuit are normally off and Q10 is conducting. When signal TIMOUT or the TIMOUT is missing, a voltage unbalance occurs that forces either Q8 or Q9 into conduction. When Q8 or Q9 conducts, Q10 is forced into cutoff. When Q10 is cut off, a high-level diagnostic error signal is applied from Q10 to gates U19 and U20 in the composite OR gate and latch circuit. Self-test signal ST2is applied to Q10 when the SELF TEST switch on the front panel is set to the on (up) position. Signal ST2forces Q10 into cutoff and a simulated error signal is applied to the composite OR gate and latch circuits to test the diagnostic circuit function. Transistor Q10 is forced into conduction when the SELF TEST switch is set to the off (down) position.

5-386. Data Retiming Circuits.

5-387. The multiplexed serial data (MSD) is clocked through flip-flop U12 by system clock signal R The data are routed through polarity switch S7 to the data output drivers circuit that generates the balanced or unbalanced serial data out signals SDATAO and SDATAO-. The operation of the data output drivers circuit (Q11 through Q17) is functionally the same as that described for the timing output drivers circuit. When switch S8 on the card is set to the unbalanced position (U), output signal SDATAO is tied to ground and SDATAO is $\pm$6 vdc. When S8 is in the balanced condition (B), signals SDATAO and SDATAO are $\pm$3 vdc signals.

5-388. The operation of data error detectors Q18 through Q20 is functionally the same as that described for the timing error detector circuit. A defective output data signal generates a diagnostic error signal from Q20 to the composite OR gate and latch circuits.

5-389. Transition Encoder Timing Circuits. Timing oscillator Y2 generates 1.8432-MHz ($\pm$0.01 percent) timing signals that are applied to eight-stage N binary counter Ull, U14. The N=6 (28.8 kHz) output from U14-13 is applied to divide-by-six counter U16, U18 to produce the 4800-Hz timing signals. These signals are routed through three distribution buffer gates U21 to provide the T4800A, T4800B, and T4800C timing outputs. The N=8 (7.2 kHz) output from U14-11 is applied to divide-by-two counter U16 to generate the 3600-Fz timing signals. These signals are routed through three distribution buffer gates U24 to provide the T3600A, T3600B, and T3600C timing outputs. Timing signals T3600A and T4800A are applied to one-shot multivibrators U10 and U15 in the 3600-Hz and 4800-Hz activity detectors. When one of the timing signals is interrupted, the associated multivibrator completes its duty cycle and a diagnostic error signal is applied to composite OR gate U17, causing signal MRT to be generated as explained in the following discussion.

5-390. Composite OR Gate and Latch Circuits.

5-391. Latch U20, U23 generates diagnostic reference timer card error signal MRT when an error is detected or when self-test signal ST2is applied to the card. Latch U20, U23 is reset by signal ERST from the front panel as previously described.

5-392. The three retriggerable one-shot multivibrators (U10-9, U15-6, and U1510) are normally held in conduction by timing signals T3600A and T4800A and system clock signal $R_{o.}$ An error condition (loss of signal) to any one of the multivibrators causes the appropriate multivibrator's duty cycle to expire and set latch U20, U23 through OR gate U17 and AND gate U20. A high-level error signal from the timing or data diagnostic circuits applied to OR gate U19 sets the latch to the error condition through OR gate U17-6 and AND gate U20-3.

5-393. When the system is in the self-test mode, self-test signal ST2inhibits AND gate U20-3 to prevent any simulated error inputs from OR gate U17-6 from setting latch U20, U23. Signal ST2forces the diagnostic circuits to generate high-level inputs to AND gate U17-8 when the card diagnostic circuits are operational. AND gate U17, in turn, sets latch U20, U23, thus generating signal MRT-. When the SELF TEST switch on the front panel is set to the off (down) position, signal ST2goes high (diagnostic enable) and signal ERST resets latch U20, U23 to its no error state.

SECTION IV

DEMULTIPLEXER CARDS FUNCTIONAL OPERATION

5-394. INTRODUCTION.

5-395. This section contains the block diagram and detailed circuit discussions for each of the card types used in the demultiplexer. The detailed circuit discussion for each card follows the associated card-level block diagram discussion. The following cards are described in this section.

5-396. SMOOTHING BUFFER (SB) CARD.

5-397. GENERAL. The SB card is a channel option card that may be used to service one data output channel with its associated timing. The SB card function is basically the complement of the RCB card function performed in the multiplexer. Functionally, the SB card demultiplexes one channel of data out of the high-speed data stream from the far-end multiplexer.

The data are converted from a synchronous format into the original asynchronous format that was applied to the far-end multiplexer. The original timing associated with the data is also regenerated. The block diagram discussions are based on the block diagram shown in figure FO-4. The detailed circuit discussions are based on the SB card logic diagram in the circuit diagrams manual.

5-398. BLOCK DIAGRAM DISCUSSION.

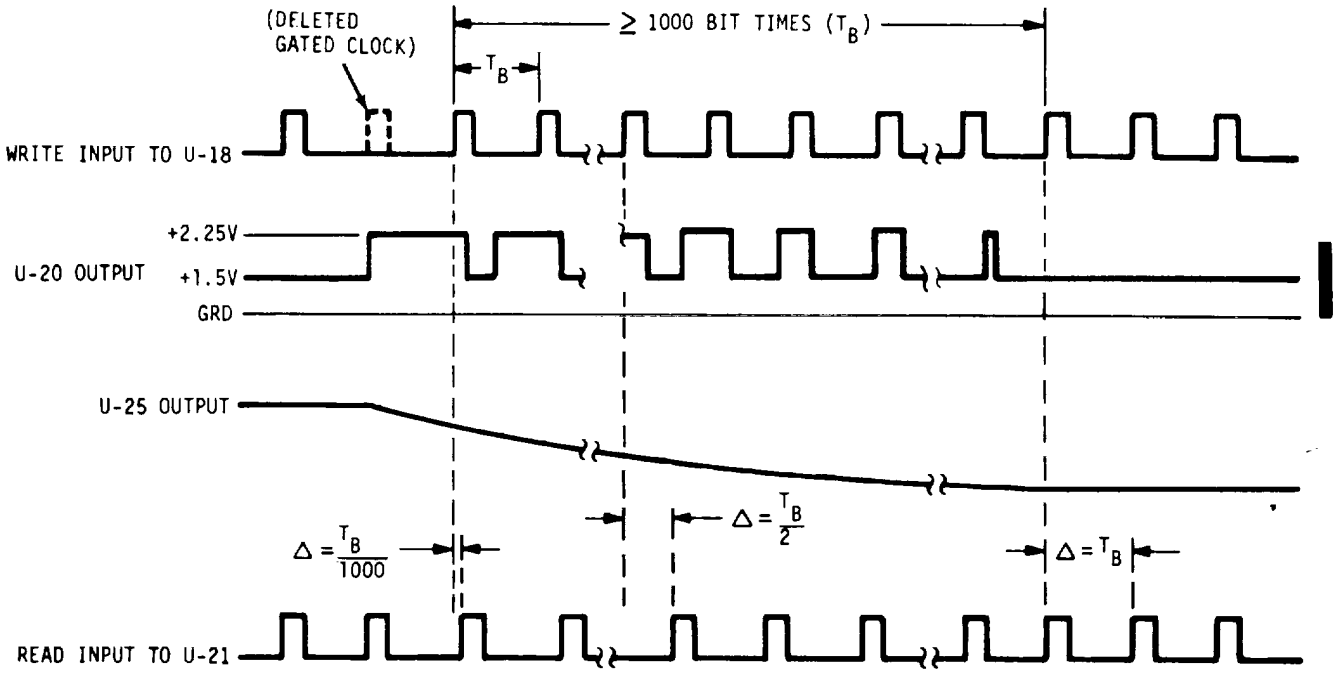
5-399. GENERAL. The SB card can be operated in one of two modes of operation. The mode of operation is controlled by setting the URD/SB switch to the URD or the SB position. The mode of operation is determined by the mode of operation selected for the far-end RCB card in the multiplexer function. The system requirements that control the mode of operation selected are described in the RCB card discussion in paragraph 5-169. As described in the following paragraphs, the basic operation of the SB card is the complement (or reverse) of the RCB card. The data elastic storage register in the SB card writes in the data under control of a synchronous clock and reads out these data under control of an asynchronous clock. This synchronous to asynchronous form conversion is accomplished using a smoothing function that produces output data bits at the same rate at which the data were applied to the RCB card of the far-end multiplexer. This basic smoothing concept is described in paragraph 5-64.

5-400. Input-Output Buffer Function. The incoming channel data bits (DTIX-) are clocked through the data input buffer by associated gated clock signals DGCXX. The gated clock signals are applied directly to the data input buffer in the SB mode of operation, or the signals are processed through the coarse rate conversion circuits when the circuits are operated in the URD mode of operation. The write address counter, which is sequentially incremented by gated clock signals DGCXX, generates the 4-bit write addresses that are applied to the data elastic storage register and to the write address latch. The write address signals applied to the data elastic storage register control the memory locations in which the applied data bits are stored. The data elastic storage register is identical to the data elastic storage register in the RCB card and has the same write and read capability. The read address counter that generates the 4-bit read addresses to the data elastic storage register is clocked by the read clock signals from the analog phase-locked loop (APLL) circuit. The data clocked out of the data elastic storage register are clocked through the data output buffer to the data output drivers. The output clock signals that clock the data through the data output buffer are also generated by the APLL circuits. The timing output drivers are also clocked by the output clock signals from the APLL circuit. The data and timing output signals are conditioned in the output drivers and are routed through their associated output line switch circuits that are set to produce a balanced or an unbalanced line output. When the output is applied to a balanced line configuration, the output data and timing line switches are set so that the two channel data out signals (DOXX and DOXX-) and the two timing out signals (TOXX and TOXX-) are generated. In an unbalanced condition, only signals DOXX and TOXX are generated. The end-of-scan activity detector samples end-of-scan signal DEOS3NX. The detector is a retriggerable one shot multivibrator that is held in conduction by signals DEOS3NX. When the signals are missing, the one-shot multivibrator duty cycle expires and generates an inhibit signal that inhibits the data output of the data output buffer.

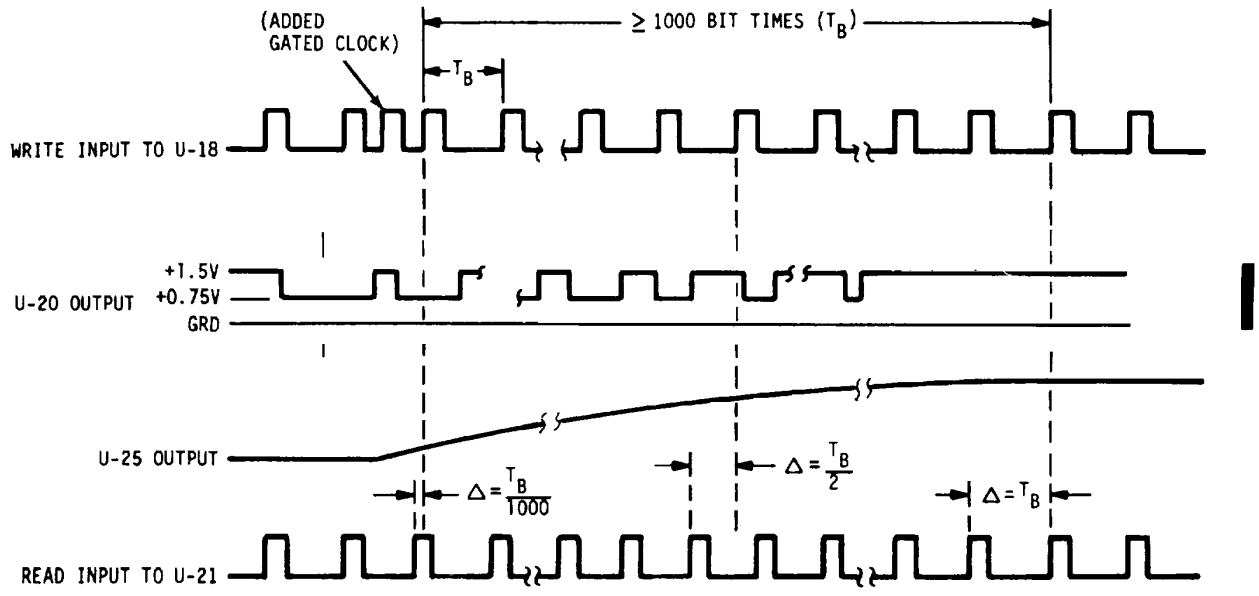
5-401. APLL Circuit. The write and read address counters are clocked by independently generated timing signals. The write address counter is clocked by gated clock signal DGCXX, and the read address counter is clocked by the divided output of a voltage-controlled multivibrator (VCM). The APLL circuit phase locks the output of the VCM with the incoming gated clock signal, causing the VCM to generate a number of read clock pulses equal to the number of write clock pulses being applied to the data elastic storage register over a given period of time. A smoothing function is also accomplished by the APLL circuit. Gated clock pulses are added and deleted as a result of the overhead servicing function. The addition or deletion of a gated clock pulse represents an instantaneous change in the applied gated clock frequency. Since synchronization circuits of user equipment cannot operate with such a change applied to their inputs, instantaneous bit rate deviation is not acceptable. The APLL circuit therefore detects the instantaneous gated clock addition or deletion, and gradually (smoothly) increases or decreases the output rate of the VCM by one bit time over an extended number of VCM clock times. The gradual change in VCM output rate causes the gated clock and VCM rates to become nominally equal, while precluding unacceptable short-term rate variations in the channel's output timing signal. Thus, in performing the smoothing function, the APLL circuit maintains a phase locking of the gated clock and VCM output signals, and prevents an underflow or overflow of data in and out of the data elastic storage register.

5-402. As in the RCB card, an 8-bit offset is maintained between the write and read addresses being applied to the data elastic storage register. This is accomplished by applying the MSB of the 4-bit read address and the inverted MSB of the 4-bit write address to the two inputs of the APLL phase detector. In the locked condition, these two signals are coincident at the phase detector inputs, and the inversion of the write address MSB yields the desired 8-bit offset. When an individual gated clock pulse is added or deleted, the resulting phase shift between the gated clock and VCM output signals is detected by the phase detector, which produces a series of control pulses. These control pulses are applied to an active filter circuit, causing a gradual dc control voltage change to be applied to the voltage-controlled multivibrator (VCM) input. The width of dc control voltages applied to the phase detector is proportional to the degree of phase differential that is detected. The greater the phase differential, the wider the width of each control pulse from the phase detector. In turn, as the two signals being compared by the phase detector approach an in-phase relationship, the width of the control pulses decreases and the pulses are turned off when the two signals are phase locked. This changing control voltage causes the VCM output frequency to slew to a rate nominally equal (after division by a divide-by-2n counter) to that of the gated clock signal. In practical operation, a continuous in-phase relationship is not maintained, but continuous control pulses are generated that force the VCM output to slew near the gated clock pulse input rate and effectively maintain a pulse for-pulse relationship over any given period of time.

5-403. Figure 5-31 conceptually depicts key APLL waveforms and serves to illustrate overall APLL operation. In figure 5-31, part A, a gated clock is deleted from the U-18 write input (negative stuffing), causing the dc control voltage to appear at the output of phase detector U20. When applied to active filter U25, the dc control voltages cause the active filter to produce a negative-going change in the control voltage applied to the VCM.



-A NEGATIVE STUFF-



-B POSITIVE STUFF-

Figure 5-31. APLL Circuit Stuffing - Waveform Diagram

After division by a divide-by-2n counter, the output of the VCM is applied as a clock signal to read address counter U21. As shown in figure 5-31, part A, the divided output frequency of the VCM is gradually decreased over an interval of 1000 or more data bit times. At the end of this period, it is once again nominally equal to the gated clock rate, as evidenced by the lack of an dc control voltage from phase detector U20. It should be noted that an equal number of clocks is applied to write address counter U18 and to read address counter U21 over the period shown in figure 5-31. This indicates that a long-term reduction has been made in the read counter clock rate in response to a short-term rate change in the gated clock driving the write counter. Figure 5-31, part B, illustrates APLL operation in the inverse (positive stuffing) situation (i.e., long-term increase of the read clock rate in response to a short-term increase in the gated clock rate). In this case, a series of less positive control voltages are generated from the phase detector. These control signals produce positive-going control voltages to the VCM.

5-404. Coarse Rate Conversion Circuits. The circuits in the coarse rate conversion circuits on the SB card are identical to those on the RCB card. The functional application of the two circuits is also identical. The coarse rate conversion circuits (figure 5-32) produce modified gated clocks to the write address counter when switch S3 is set to the URD position. In normal operation, end-of-scan signal DEOS3NX increments the word counter to generate a 10-bit binary code that sequentially advances one count during each word until the end-of-scan signal in word 24 of minor frame count 31 occurs. At this time, the word counter preset control generates a preset signal that presets the word counter binary output to zero.

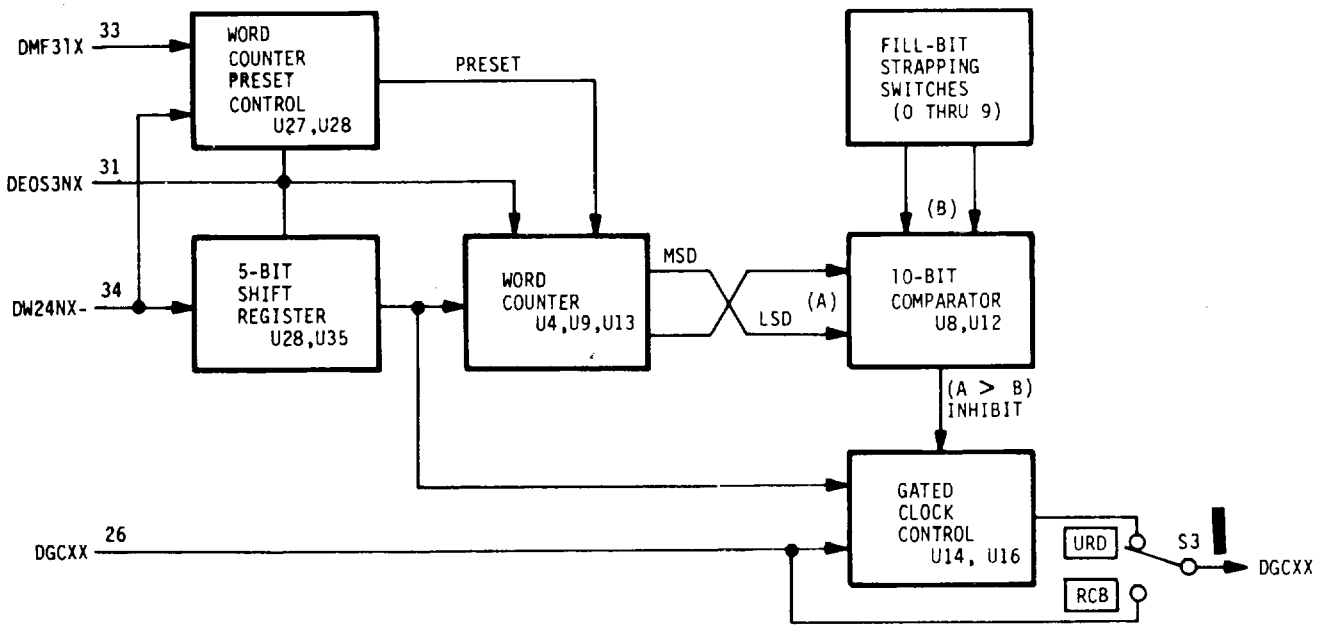


Figure 5-32. SB Card, Coarse Rate Conversion Circuits - Block Diagram

The end-of-scan signal DEOS3NX, together with word 24 DW24NX-, clocks a data bit into the 5-bit shift register so that an inhibit signal is clocked out from the register during word 29. The inhibit signal during word 29 inhibits the word counter and the gated clock control so that a gated clock is not deleted during word 29. Each word Count from the word counter is applied as the A input to the 10-bit comparator. Before the circuits are activated, 10 fill-bit strapping switches (0 through 9) are strapped to a predetermined count that is related to the number of gated clocks to be deleted during a major frame. The 10-bit binary code from the strapping switches is applied as the B input to the 10-bit comparator. The 10-bit comparator continually compares the 10-bit binary code (A) from the word counter against the programmed 10-bit binary code applied from the fill-bit strapping switches. Each time a binary code applied as the A inputs is less than the programmed B input, the gated clock inhibit signal is generated and applied to the gated clock control logic. The outputs from the word counter are reversed so that the MSB of the counter is applied to the LSB of the A input to the 10-bit comparator. As a result, the near homogeneous spread of the gated clock deletions is obtained by the reversed binary count function.

5-405. Diagnostic Circuits. A data diagnostic compare function is initiated when word 24 bit 0 signal DW240X is applied to the address compare control circuit (Figure FO-4). At this time, the address compare control generates an enable signal to the write address latch and to the data latch. The write address latch stores the 4bit write address associated with the data bit that is being written into the data latch and the data elastic storage register at this time. Approximately eight bit times later, the address comparator receives a 4-bit read address that should compare with the address stored in the write address latch. The A=B signal generated by a compare is applied to the diagnostic flip-flop. When the next output clock signal from the divide-by-2n counter is applied to the flip-flop, a compare enable signal is generated by the flip-flop. At this time, the compare enable is applied to the data compare logic to perform a compare of the data bit stored in the data latch against the equivalent data bit out of the data output buffer. Since the two bits have the same address, they should be identical pulses. When they are not the same, an error signal is developed and applied to the composite diagnostic logic to generate a card error output signal. The card error output signal is applied on the positive stuff request (DPSTXX-) line to the OEG card.

5-406. The composite diagnostic logic also receives error inputs from the data output drivers and the timing output drivers circuits. When any one of the three error signals is applied to the logic, the card error signal (DPSTXX-) is generated. The composite diagnostic logic is reset by error reset signal DERRS when the DISPLAY RESET switch on the front panel is pressed. In turn, the composite diagnostic circuits are enabled and produce signal DPSTXX when self-test signal ST1is applied when the SELF TEST switch on the front panel is set to the on (up) position.

5-407. DETAILED CIRCUIT DISCUSSION.

5-408. Input-Output Buffer Function. The incoming channel data pulses (DTIX-) are clocked through data input buffer U1-8 and are applied serially to data elastic storage register U22, U23. The data are clocked through the buffer and into the storage register by gated clock signals DGCXX. The gated clocks increment write address counter U18, which, in turn, produces the sequential 4-bit write addresses that are applied to the data elastic storage register.

The 4 bit read addresses that select the locations from which the data are read out are produced by read address counter U21. Read address counter U21 is incremented by the read clock pulses from the APLL circuit. The data pulses from the storage register are serially clocked through data output buffer U1-5 as complementary outputs DATOUT and DATOUT-

5-409. Data pulses DATOUT and DATOUT are applied through polarity switch S10 to amplifiers Q2 and Q3 in the data output drivers circuit. Switch S10 provides a way to change the phase relationship of the two data pulse outputs with respect to the associated timing pulses to meet different system configuration requirements. Transistor ^{Q4} is a constant-current source for amplifiers Q2 and Q3. Amplifiers Q2 and Q3, in turn, drive push-pull emitter followers Q5 through Q8. Setting switches S14 and S15 to the balanced (B) position connects breakdown diodes VR2 and VR3 (3.3 vdc) in parallel with breakdown diodes VR1 and VR4 (6.2 vdc). The breakdown diodes are in the base circuits of the push-pull emitter followers. In the balanced configuration, +3-volt channel data out signals DOXX and DOXX are produced. In the unbalanced configuration, switches S14 and S15 are set to the U position to remove breakdown diodes VR2 and VR3 from the circuits and let breakdown diodes VR1 and VR4 control the base voltages to the push-pull emitter-followers. In the unbalanced mode of operation, a +6-volt signal DOXX is produced. In the unbalanced mode of operation, switch S18 grounds the DOXX output. Switch S19 provides the appropriate wave-shaping capacitor associated with the three different output conditions: balanced mode of operation or a 75-ohm or 6K-ohm unbalanced mode of operation. Operation of the timing output drivers circuit and associated switches is functionally the same as that of the data output drivers circuit and associated switches discussed previously.

5-410. APLL Circuit. The count 8 output from write address counter U18 is inverted and applied as the reference input to pin 1 of phase detector U20. The count 8 output from read address counter U21 is applied directly to pin 3 of phase detector U20 as the variable input. Even though the write address count output is used as the reference input to U20, it will be seen that it is the overhead function of adding or deleting gated clock pulses at this input to U20 that causes the phase detector function to detect a phase shift. This application causes the phase detector to initiate commands that force the read address to follow the pulse changes from the write address counter. Phase detector U20 monitors the negative going transition of each of the two pulses applied to it. When the two count 8 outputs are proper, there is a difference count of 8 between the two 4-bit addresses. Therefore, the count 8 pulse from the write address counter is high when the count 8 pulse from the read address counter is low. Since the count 8 from the write address counter is applied through an inverter to U20, both pulses applied to U20 have the same phase and polarity in normal operation. When the two transitions of the pulses occur at the same time, U20 determines that they are phase locked and the output from U20 returns to a +1.5 volt level. When a gated clock pulse to the write address counter is deleted, U20 detects that the pulse from the read address counter is leading in phase the pulse output from the write address counter. Therefore, more positive (+2.25V) dc control signals are generated from U20 and are applied to the active filter circuit. The dc control signals are generated until a phase lock is obtained between the two pulses applied to U20. In turn, when an additional gated clock pulse is generated, U20 detects that the pulse from the read address counter is lagging the pulse from the write address counter.

Therefore, a series of less positive (+0.75V) dc control signals is generated from the output of phase detector U20. In turn, the signals are applied to the active filter circuit.

5-411. The active filter circuit contains a series of programmable RC time constant that are associated with operational amplifier U25. A series of more positive signals from U20 is processed into a negative-going dc slope voltage that is applied as a control voltage to voltage-controlled multivibrator (VCM) U31. In turn, a series of less positive signals from U20 is processed into a positive-going dc slope voltage that is applied to U31. There are two VCM's in U31. The positions of switches S24 and S25 determine which VCM is used in a given system application. A positive-going dc slope voltage causes the output frequency from U31 to increase. A negative-going dc slope voltage causes the output frequency from U31 to decrease. The output from U31 is applied through switch S25 to divide-by-16 counter U26 or to divide-by-2^n counter U32.

5-412. Six switches are involved in the configuration of the APLL circuit. Each switch has four positions (A through D). The switches are as follows: S7 in the input circuit of integrator U25; S12 that selects the time constant associated with U25; S24 and S25 that select one of the two VCM's (U31) to be activated; S8 that adds or removes divide-by-16 counter U26 from the configuration; and S5 that selects the one output frequency from the APLL circuit that equals F_o for the channel. The frequencies associated with each of the four switch positions A through D are shown opposite switch S5 on sheet 3 of the SB card logic diagrams.

5-413. Divide-by-16 counter U26 is activated when switch position B or D is selected for a given circuit configuration. The output from U31 is divided by 16 in U26 and is then applied to divide-by-2n counter U32. In switch position A or C, U26 is bypassed and the output from U31 is applied directly to U32. The selected output from U32 has several functions. One output is routed through inverters U33 and U2-8 as the read clock signals that increment read address counter U21. One output from inverter U33 and U2-10 is applied as the output clock signals to clock the data bits (DATOUT and DATOUT-) through output buffer U1 to the data output drivers circuit. The output clock signals are also applied through three inverters U2 to produce timing output signals TIMOUT and TIMOUT to the timing output drivers circuit. The output applied through inverter U2-10 is applied as output clock signals that clock diagnostic flip-flop U36-9. In the overall APLL operation, the deletion of an incoming gated clock pulse causes U20 to detect that the pulse transition from the read address counter is leading the pulse transition from the write address counter. The result is that the read clock pulses from the APLL circuit to the read address counter start to decrease in frequency very slowly, hardly affecting the overall nominal bit rate. In turn, the addition of a gated clock pulse causes U20 to detect that the pulse transition from the read address counter is lagging the pulse transition from the write address counter. The result is that the read clock pulses from the APLL circuit to the read address counter start to increase in frequency very slowly. The functional waveform representation of the APLL circuit function is shown in figure 5-31.

5-414. Coarse Rate Conversion Circuits. When switch S3 is in the SB position, a +5-volt enable signal is applied to one input of AND gate U16-3. This configuration allows each gated clock signal DGCXX applied to the SB card to be routed to the write address counter. When switch S3 is in the URD position, a selected number of incoming gated clock pulses is inhibited by inhibit signals applied from the CRC circuits to AND gate U16-3.

The functional operation of these circuits is the same as that described for the coarse rate conversion circuits in the RCB card. The specific components associated with the functions performed in the CRC circuits are shown on the block diagram in figure 5-32.

5-415. Diagnostic Circuits. In a no error condition, the three error inputs to OR gate U14-8 are high to produce a low input to AND gate U15-6. The high output from U15-6 enables the strobe input to OR gate U7-6. This condition produces a low output from U7-6 since all inputs to U7-6 are high in a no error condition. When one of three error inputs to OR gate U14-8 goes low, the output from AND gate U15-6 goes high and produces a low inhibit strobe input to OR gate U7-6. This condition forces a high from U7-6 that produces card error signal DPSTXX through inverter U10-12. When an error signal is generated by one of the outputs from the drivers circuit and is applied through inverter U10-2 or U10-4, latch U14, U15 is set and holds the diagnostic circuits in the error state until the DISPLAY RESET switch on the front panel is pressed. At this time, reset signal DERRS is applied through exclusive OR gate U11-11 to reset latch U14, U15 and returns the diagnostic circuits to their no-error state, assuming that there are no faulty circuits on the card. In the self-test mode, signal ST1is applied to exclusive OR gate U11-8 to produce a low inhibit signal to AND gate U15-6. The output from U15-6 at this time is an enable strobe to OR gate U7-6. At this time, OR gate U7-6 only produces the desired error condition when all three error inputs applied to it are low. When all three error inputs are low, the output of U7-6 goes high, causing signal DPSTXX to be generated. When the self-test function is complete, signal ST1goes high and error reset signal DERRS is applied to the circuits to reset them to their no-error state.

5-416. A faulty condition in the data output drivers circuit causes emitter followers Q5 through Q8 to produce a higher or lower (unbalanced) dc voltage to the base circuits of Q9 and Q11. When one of the two stages is forced into conduction, Q10 turns off and produces a high output that is applied to inverter U10-4 in the composite diagnostic logic. The output from inverter U10-4, in turn, causes error signal DPSTXX to be generated. In the timing output drivers circuit, Q19, Q21, and Q20 perform the same diagnostic function for the timing output drivers circuit. The output from Q20 is applied to inverter U10-2 in the composite diagnostic logic, resulting in generation of error signal DPSTXX-.

5-417. A diagnostic address compare function is initiated when word 24 bit 0 signal DW240X is applied to the SB card. Signal DW24OXis applied through inverter U34-10 to enable AND gate U15-3. The other input to AND gate U15-3 is enabled when the last diagnostic address compare function is completed. If the previous diagnostic address compare function is not complete at the time signal DW240Xis applied, a new address compare is not initiated. When AND gate U15-3 is enabled, the output signal is applied through inverter U16-6 to clock the preset 4-bit write address into write address latch U19. The low output from AND gate U15-3 is also used to set latch U29-6, U29-8. The latch output, in turn, applies a high input that is clocked into the J input of flip-flop U30-10 by the next read clock from the APLL circuit. At this time, the Q output from U30-9 presets flip-flop U30-7 and resets latch U29-6, U29-8. The output from flip-flop U30-7 enables address comparator U24 and presets flip-flop U37-9 whose output inhibits AND gate U15-3. The inhibit signal to U15-3 prevents the next DW240Xsignal from entering a new 4-bit address in U24 before the existing compare function is completed.

An SB card that has a minimum of used ports assigned to it may not obtain the required bit counts (approximately eight) to establish a compare in the address comparator before the next one or more DW240X signals are applied.

5-418. At the time that the read 4-bit address applied to address comparator U24 is the same address as that stored in write address latch U19, an A=B signal is applied from U24 to flip-flop U36-10. The next read clock signal produces a high signal from U36-10 that is applied to AND gate U15-11. At the time that the write address latch was set, the data bit associated with the stored write address was clocked into flip-flop U36-6 by the output from AND gate U15-3. Therefore, the data output from data buffer U1-5 should be the same data pulse that is stored in U36-6. When the two pulses are identical, the output from exclusive OR gate Ull-3 is low and the output of flip-flop U3-10 remains high. When the data bits being compared are not identical, the output of exclusive OR gate Ull-3 goes high and enables AND gate U15-11. The low output from U15-11 is clocked through flip-flop U3-10 as a low signal to OR gate U14-8. The high output from U14-8 enables AND gate U15-6, causing OR gate U7-6 to generate card error signal DPSTXX through inverter U10-12.

5-419. NARROW BAND SMOOTHING BUFFER (NBSB) CARD.

5-420. GENERAL.

5-421. The operation of the NBSB card is basically the same as that of the SB card described in paragraphs 5-396 through 5-418. The only difference between the NBSB card and the SB card is in the electrical configuration of the APLL circuit as described in paragraphs 5-422 through 5-425. Functionally, the overall operation of the two cards is the same, with two exceptions: the output rate of the NBSB card is limited to one of five values (153.6, 76.8, 50, 38.4, or 19.2 kHz); and the smoothing function performed by the APLL circuit in the NBSB card provides for a more gradual slewing of the output data bit rate than occurs in the SB card. The NBSB card APLL circuit compensates for a 1-bit adjustment (caused by positive or negative stuffing) of the input gated clock rate by gradually shifting the card's output rate one bit over an interval of approximately 20, 000 data bit times. This same smoothing function on the SB card is performed over an interval of approximately 1,000 bit times.

5-422. DETAILED CIRCUIT DISCUSSION.

5-423. The following discussion describes the APLL circuit as shown in the NBSB card logic diagram in the circuit diagrams manual. Except for the APLL circuit, the reference designations for all the other circuits on the NBSB card and the SB card are the same as shown in their respective logic diagrams. In the APLL circuit, the count 8 output from write address counter U18 is inverted through inverter U10-8 and is applied as the reference input to pin 3 of phase detector U25. The count 8 output from read address counter U21 is applied directly to pin 14 of phase detector U25 as the variable input. Even though the write address count output is used as the reference input to U25, it will be seen that it is the overhead function of adding or deleting gated clock pulses at the input to U25 that causes the phase detector function to detect a phase shift. This application causes the phase detector to initiate commands that force the read address to follow the pulse changes from the write address counter. Phase detector U25 monitors the positive-going transition of each of the two pulses applied to it. When the two count 8 outputs are proper, there is a difference count of eight between the two 4-bit addresses. Therefore, the count 8 pulse from the write address counter is high when the count 8 pulse from the read address counter is low. Since the count 8 from the write address counter is applied through inverter U10-8 to U25, both pulses applied to U25 have the same phase and polarity in normal operation.

When the two transitions of the pulses occur at the same time, U25 determines that they are phase locked and the output from U2 is effectively an open circuit. When a gated clock pulse to the write address counter is deleted, U25 detects that the pulse from the read address counter is leading in phase the pulse output from the write address counter. Therefore, a series of more-positive control signals is generated from U25 and is applied to the active filter circuit. The pulses are continuous until a phase lock is obtained between the two pulses applied to U25. In turn, when an additional gated clock pulse is generated, U25 detects that the pulse from the read ad- dress counter is lagging the pulse from the write address counter. Therefore, a series of less positive control signals replaces the normal phase-locked signal output from phase detector U25. In turn the less positive control signals are al plied through a low-pass filter circuit to voltage-controlled multivibrator (VCM) U26.

5-424. Resistors R8, R9, and R12 and capacitor C6 make up the low-pass filter. A series of positive pulses from U25 is filtered in the low-pass filter circuit into a positive-going dc slope voltage that is applied as a control voltage and increases the output frequency from VCM U26. In turn, a series of negative-going pulses from U25 is filtered into a negative-going dc slope voltage that causes the output frequency from U26 to decrease. The out- put pulses from U26 are applied through inverter U20-15 to divide-by-16 counter U32.

5-425. Four switches are involved in the operational configuration of the APLL circuit. Switch S7 in the input circuit of U26 is set to the NORM position during normal operation. Switch positions MAX and MIN of S7 are used in the initial factory calibration of potentiometers R14, R16, R18, and R73 in the VCM circuit. Switches S8 and S12 are set to the 50K position when switch S5 is set to the 50K position. Switch S5 is set to the nominal output rate of the channel. When switch S5 is set to the 153.6K, 76.8K, 38.4K, or 19.2K position, switches S8 and S12 are set to the 153.6K position. The selected out- put from U32 is applied through switch S5 and inverter U33-2 to the same circuits as those described in the SB card theory of operation.

5-426. TRANSITION DECODER (TD) CARD.

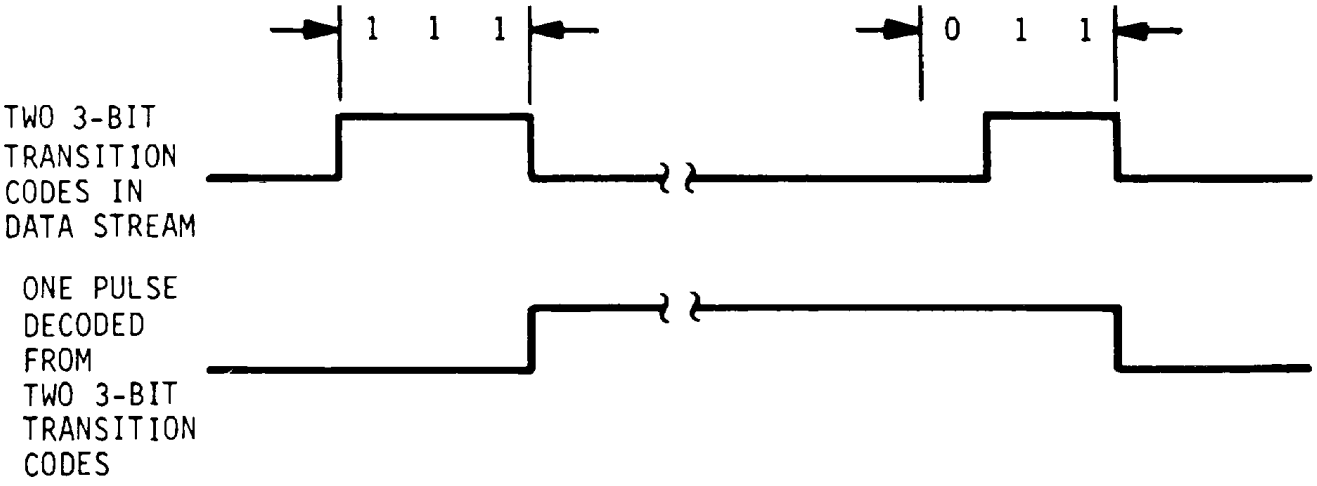
5-427. GENERAL. The TD card is a channel option card that may be used to service one digital data output channel that does not have associated timing. The function of the TD card is basically the complement of the function of the TE/TR card in the multiplexer. Functionally, the TD card demultiplexes one selected channel of digital data out of the high-speed serial data stream from the far-end multiplexer. The demultiplexed data are converted from a synchronous format to the asynchronous digital format of their original application to the far-end multiplexer. The block diagram discussion is based on the block diagram in figure FO-5. The de-tailed circuit discussions are based on the TD card logic diagram in the circuit diagrams manual.

5-428. BLOCK DIAGRAM DISCUSSION.

5-429. Input-Output Buffer Function. The incoming digital channel data pulses (DTIX-) are clocked through the data in- put buffer to the data elastic storage register by gated clock signals DGCXX. The gated clock signals are also applied to the write address counter, which, in turn, produces the 4-bit write address that is applied to the data elastic storage register and to the write ad-dress latch. The operation of the data elastic storage register is the same as that of the data elastic storage register described in the SB card theory of operation.

The read address counter that produces the 4-bit read addresses to the data elastic storage is incremented by the read clock signals from the analog phase-locked loop (APLL) circuit. The data read out of the data elastic storage register are clocked into the transition decoder No. 1 circuits. In the transition decoder No. 1 circuits, each set of 3-bit transition codes is decoded to produce one positive-going or negative-going transition enable signal that clocks the data out- put buffer. The data from data output buffer No. 1 are routed to the data output drivers circuit. Figure 5-33 shows a typical pulse output produced from the data output buffer as a result of decoding two sets of 3-bit transition codes. The data applied to the data output drivers circuit are conditioned and then applied through the data output line switch circuit to pro- duce a balanced or unbalanced output from the TD card. In a balanced line output configuration, two complementary channel data out signals (DOXX and DOXX-) are produced. Only one output signal (DOXX) is produced in the unbalanced line output configuration.

5-430. APLL Circuit. The read clock signals to the read address counter and the clock signals to the transition decoder are produced by the APLL circuit. The read clock signals to the read ad- dress counter are phase locked to the write clock signals by the APLL circuit to ensure that the number of read clocks applied to the read address counter equals the number of write clock (DGCXX) signals applied to the write address counter. The smoothing function per- formed by the APLL circuit described in the SB card theory of operation is also performed by the APLL circuit on the TD card. The overall operation of the APLL circuit is the same as that described for the SB card. Basically, the phase detector monitors the count eight out- puts from the read and write address counters and generates corrective signals to the active filter circuit when a phase change is detected between the negative-going transitions of the write and read address pulses. In turn, the active filter circuit generates the sloping dc control voltage that controls the voltage-controlled multivibrator (VCM) output frequency. The output from the VCM is applied to the divide-by-2n counter. The counter, in turn, generates the read clock pulses applied to the read address counter in the input-output buffer function.



6186-158

Figure 5-33. TD Card, 3-Bit Transition Code - Waveform Diagram

5-431. Diagnostic Circuits. A diagnostic address compare function is initiated when word 24 bit 0 signal DW240X is applied to the address compare control circuit, the write address latch, and the data latch. The write address latch stores the 4--bit write address generated at this time. In turn, the data bit associated with the 4-bit write address is set into the data latch. The address compare control circuit then generates an enable signal to the ad- dress comparator. Approximately eight bit times later, the address comparator receives a 4-bit address from the read address counter to its A inputs that is identical to the address from the write address latch that is applied to its B inputs. At this time, the A=B output from the comparator is applied to the diagnostic flip-flop. When the next output clock signal from the APLL circuit is applied to the diagnostic flip- flop, a compare enable signal from the flip-flop is applied to the data com- pare logic No. 1 circuit to perform a compare of the data bit stored in the data latch against a data bit out of transition decoder No. 1. Since the two data bits have the same 4-bit ad- dress, the data bits are identical in a no-error condition. Therefore, when the bits are not identical, an error signal is developed and applied to the composite diagnostic logic.

5-432. Diagnostic transition decoder No. 2 and diagnostic data output buffer No. 2 duplicate the function performed by transition decoder No. 1 and data output buffer No. 1. The diagnostic circuits generate a series of output data bits that are the complement of the data bits out of the functional circuits. When the two data bits are not complementary, the data compare logic No. 2 circuit generates an error input to the composite diagnostic logic circuit.

5-433. The output clock- timing signals from the APLL circuit are monitored by the timing activity detector. The detector is a retriggerable multivibrator that is held in conduction by the timing signals. When the output clock-signals are missing, the multivibrator's duty cycle expires and a low-level error signal is applied to the composite diagnostic logic. The data output drivers circuit contains a diagnostic circuit that also produces an error signal to the composite diagnostic logic circuit when the circuit malfunctions.

5-434. The composite diagnostic logic circuit has four diagnostic error in- puts. When any one of the four inputs indicates an error condition, a card error signal is generated on the positive stuff request (DPSTXX-) line to the OEG card. When the self-test mode is initiated, self-test signal ST- causes a data no-compare condition to exist at the data compare logic No. 1 circuits, which, in turn, force the composite diagnostic circuit to generate signal DPSTXX-. When the DISPLAY RESET switch on the front panel is pressed, error reset signal DERRS- is applied to reset the diagnostic circuits to their normal operation. Signal DERRS- is also applied when the SELF TEST switch on the front panel is re- leased.

5-435. DETAILED CIRCUIT DISCUSSION.

5-436. Input-Output Buffer Function. The incoming channel data pulses (DTIX-) are clocked through data input buffer U1-8 and are applied serially to data elastic storage register U3, U4. The data are clocked through the buffer and into the storage register by gated clock signals DGCXX. The gated clocks increment write address counter U5, which, in turn, produces the sequential 4-bit write addresses that are applied to the data elastic storage register. The 4- bit read addresses that select the locations from which the data are read out are produced by read address counter U2.

Read address counter U2 is incremented by the read clock pulses from inverter U19-6 in the APLL circuit. The data pulses from the elastic storage register are serially clocked through AND gates U9-8 and U9-11 and OR gate U9-6 to shift register U14 in the transition decoder No. 1 circuits.

5-437. The transition decoder No. 1 circuits decode each set of 3-bit transition codes into the original data transition that occurred in the far-end multiplexer. The overall result is that data output buffer U1-5 generates re- constructed data pulses that are identical to those originally applied to the far-end multiplexer. The 3-bit code is loaded serially into 3-bit shift register U14 and is clocked out as a 3-bit parallel output. Bit 1 read out of Q2 of U14 is the transition code and is always a one each time a transition occurs. This bit is applied through AND gate U20-11 and inverter U19-10 as an enable input to pin 13 of AND gate U24- 12. Bit 2, which identifies when the transition occurred, is a one when the transition occurred in the first half of the timing pulse or bit 2 is a zero when the transition occurred in the second half of the timing pulse. The bit 2 (Q1) output from U14 is applied to one input of exclusive OR gate U21- 11. The bit 3 (QO) output from U14 indicates that the transition is a positive-going (one) signal or a negative- going (zero) signal. The QO output is applied directly to the D input of data output buffer U1-5.

5-438. The second input to exclusive OR gate U21-11 is a timing signal from U18-7 in the APLL circuit. This clock signal is applied at the same clock rate as the clock signal applied to U14-10. The clock signal applied to pin 2 of AND gate U24-12 is twice the frequency of the clock signal applied to U14-10. When bit 2 is a one, indicating a first half transition, AND gate U24-12 generates a positive-going clock pulse to data buffer U1-5 in the first half cycle of the timing as shown in (G) of figure 5-34. When bit 2 is a zero, indicating a second half transition, AND gate U24- 12 generates a positive-going clock pulse to data buffer U1-5 in the second half cycle of the timing as shown in (I) of figure 5-34.

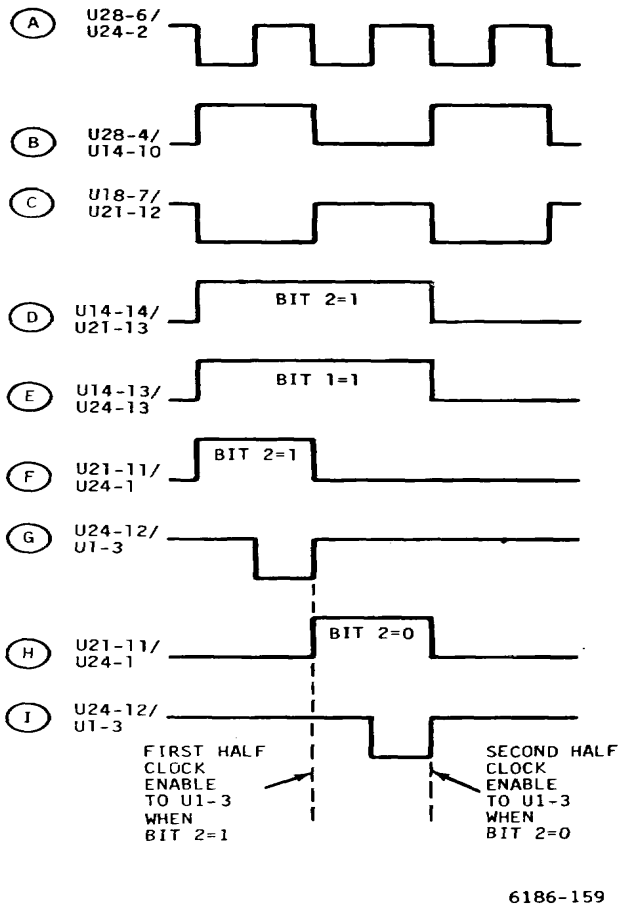


Figure 5-34. TD Card, Pulse Transition Code - Waveform Diagram

5-439. Each time a clock pulse is applied to U1-5, the bit applied to the D input from the QO output of U14 causes complementary output signals DATOUT and DATOUT- to be generated. Signals DATOUT and DATOUT- are applied through polarity switch S5 to the inputs of amplifiers Q1 and Q2 in the output drivers circuit. The function of switch S5 is to change the phase relationship of the two data output pulses to meet different system equipment configurations. Transistor ^{Q3} is a constant current source for amplifiers Q1 and Q2. The amplifiers, in turn, drive push-pull emitter-followers Q4 through Q7. Setting switch S6 to the balanced (B) position connects break- down diodes VR1 and VR4 (3.3 vdc) in parallel with breakdown diodes VR2 and VR3. These two breakdown diodes are inserted in the base circuits of Q4 through Q7 in the balanced output con- figuration to produce +3.0-volt channel data out signals DOXX and DOXX-. In the unbalanced configuration, switch S6 in the U position disables VR1 and VR4 so that VR2 and VR3 produce a $\pm$6.0-volt DOXX output signal. In the unbalanced mode, switch S6 also grounds the DOXX- output.

5-440. APLL Circuit. The count eight output from read address counter U2 is the variable input to phase comparator U29. The count eight output from write address counter U5 is inverted through inverter U6-12 and applied to the reference input of U29. The functional operation of the APLL circuit is the same as that described for the APLL circuit in the SB card. There is one major exception; only switch S4 is required to set up the selected clock bit rate for a given channel application. Switch S4 has three positions to cover the bit rates of 75, 100, 150, 200, 300, and 400. The three switch positions are associated with the Q0, Q1, and Q2 out- puts of counter U27 in the APLL circuit. Selection of any one of the three switch positions permits clock signals to be generated from the APLL circuit within a frequency range that permits the APLL circuit to maintain the proper phase relationship between the write and read clock pulses. The clock pulses applied through switches S4 and S2 are applied to inverter U28-6 and flip-flop U18-7. The clock pulses applied through inverter U28-6 are applied to AND gates U24 in the two transition decoder circuits. Flip-flop U18-7 produces half- rate clock pulses to OR gate U21 in the two transition decoder circuits. The half-rate clock pulses from the flip-flop are also applied to inverters U19- 6, U28-1, and U28-10. The clock pulses through inverters U28-4 and U28-10 clock the shift registers in the two transition decoder circuits. The clock pulses applied through inverter U19-6 are the read clock pulses that increment the read address counter.

5-441. Diagnostic Circuits. The diagnostic address compare function is initiated when word 24 bit 0 signal DW240X is applied through inverters U6-2 and U6-4 to latch U8. The next read clock pulse from the APLL circuit clocks flip- flop U12-9, which, in turn, clocks an enable signal from flip-flop U12-6 to address comparator U7. At the same time, signal DW240X applied through inverter U6-2 is also applied to clock the present 4-bit write address into write latch U10. Signal DW240X is also applied through inverter U6-4 to set the data bit associated with the 4-bit write address into data latch U11-6. When the read address from U2 applied to the A inputs of U7 matches the write address applied to the B inputs, the A=B output is produced and applied to flip-flop U11-10. The next read clock pulse clocks the Q output from Ull-9 low and presets flip-flop U12-6 high to inhibit U7. The Q output from U11-10 enables one input of AND gate U8-8. At the same time, the data bit from shift register U14-14 is identical to the data bit out- put from flip-flop U11-6. In this circuit configuration, Ull-6 is performing a latch function. When both data bits are identical, the inputs to exclusive OR gate U13-8 are the same, thus producing a low inhibit signal to one in- put of AND gate U8-8.

Therefore, in a no-error condition, a high from U8-8 to the K input of flip-flop U17-10 causes the output from U17 to remain high, indicating a no-error condition to OR gate U23-8. Activity detector U22-6 is a retriggerable multivibrator that is held in conduction until the A=B signals from U7, that are applied through U11-10, are missing. When the duty cycle of U22-6 expires, the output goes low and presents an error input to OR gate U23-6 in the composite diagnostic logic.

5-442. The functional transition decoder and the data output buffer No. 1 circuits are duplicated by the diagnostic transition detector and data output buffer No. 2 circuits. The du- plicate circuits basically consist of U15, U26-6, U26-9, and U18. The output of diagnostic flip-flop U18-9 is the complement of the data bit from flip-flop U1-5 in the functional circuits. The complementary outputs are applied to exclusive OR gate U13-6, which produces a high output in a no-error state. An error condition exists when the in- puts to U13-6 are the same. This causes a low output from U13-6 to be applied to flip-flop U17-6, which, in turn, clocks a low error signal input to OR gate U23-8 in the composite diagnostic logic.

5-443. Activity detector U22-10 is held in conduction by the read clock pulses from the APLL circuit. When the read clock pulses are missing, the duty cycle of U22-10 expires and a low-level error signal is applied to OR gate U23-6 in the composite diagnostic logic. Latch U20-6 applies a low-level error signal to OR gate U23-8 in the diagnostic composite logic when a high-level error condition is generated from transistor Q10 in the data output drivers circuit. A fault in the circuit causes an unbalanced voltage output from emitter- followers $Q4$ through $Q7$. The unbalanced condition forces either Q8 or Q9 into conduction and, in turn, forces Q10 into cutoff. When Q10 cuts off, its output goes high and is applied through inverter U28-12 as a low-level set input to latch U20. Any low error input to OR gate U23-8 causes a card error signal to be generated from inverter U28-8 on the positive stuff re- quest (DPSTXX-) line.

5-444. <u>VOICE DECODER (VD) CARD.</u>

5-445. GENERAL. The VD card is a channel option card that may be used to service one output channel of voice data. The VD card function is basically the complement of the VE card function performed in the multiplexer. Functionally, the VD card demultiplexes one channel of digitized voice data out of the high-speed serial data stream from the far-end multiplexer. These data are converted from a synchronous digital data format into the original analog (voice) waveforms that were applied to the multiplexer channel input. The block diagram discussions are based on the block diagram shown in figure 5-35. The detailed circuit discussions are based on the VD card logic diagram in the circuit diagrams manual.

5-446. BLOCK DIAGRAM DISCUSSION.

5-447. Functional Circuits.

5-448. The incoming digital channel data pulses (DTIX-) are clocked serially into a 3-bit shift register by gated clock signals DGCXX. The three outputs of the shift register are applied to the decoder logic circuit, which is looking for a condition wherein all three outputs being sampled are either ones or zeros. Three consecutive pulses that are either ones or zeros indicate the presence of high amplitude audio signals or high frequency audio signals encoded in the data message format. Each time three consecutive pulses being sampled are of the same polarity, a boost enable signal is generated and applied to the slope control circuit.

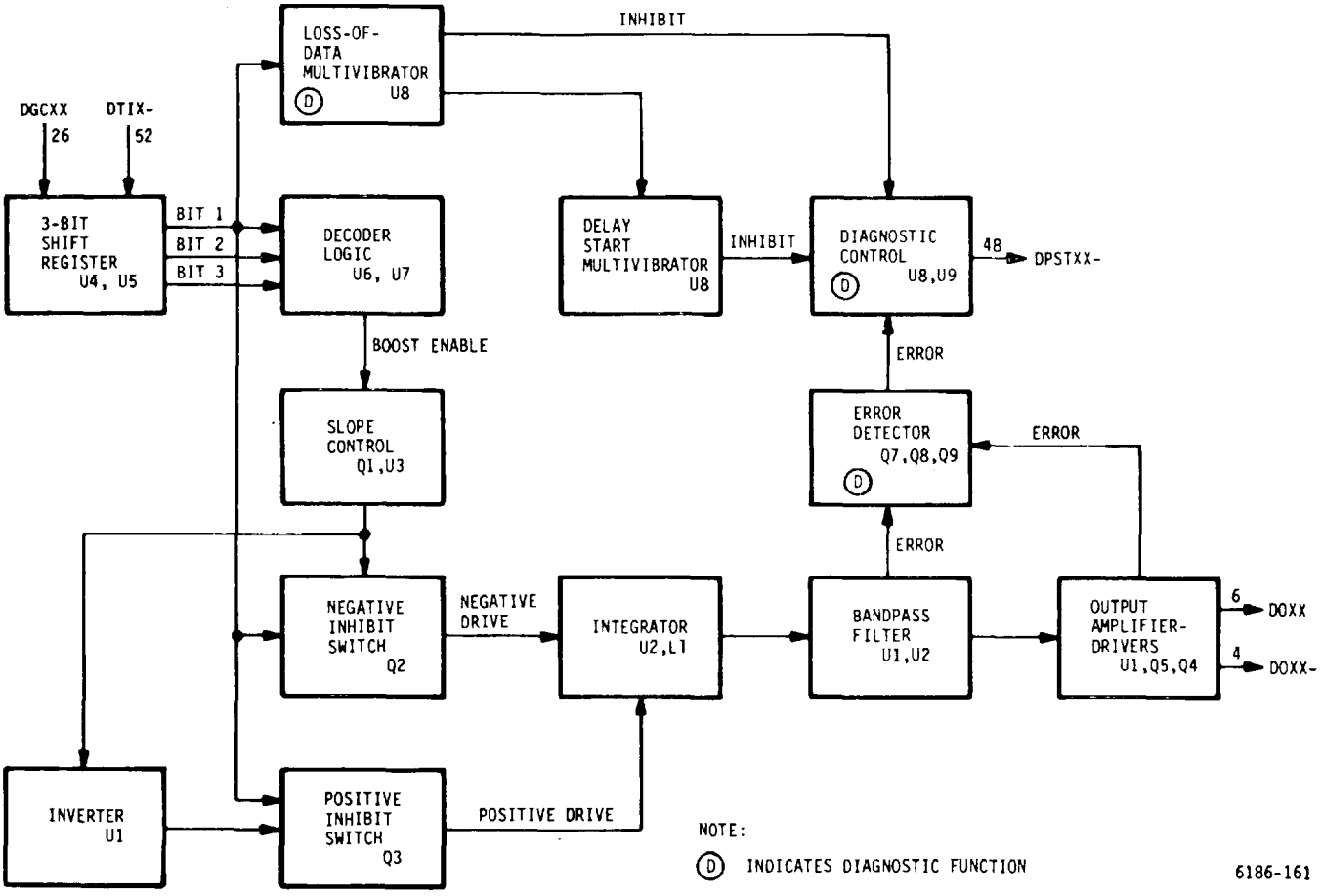


Figure 5-35. VD Card - Block Diagram

This boost enable signal is generated to increase the drive voltage to the integrator circuit and achieve the response necessary to faithfully reproduce the analog signal from the decoded digital pulses.

5-449. The slope control circuit generates the drive voltage that determines the slope of the integrator output signal. The negative drive voltage from the slope control is applied to an inverter and to the negative inhibit switch. The inverted output from the inverter is applied as a positive drive voltage to the positive inhibit switch. The polarity of the bit 1 (one or zero) signal applied to the two switches determines which switch is enabled to apply either the negative drive or the positive drive signal to the integrator. The integrator, in turn, responds to the applied drive voltage and produces the reconstructed analog signal that is applied to a bandpass filter circuit.

5-450. When the decoder logic generates the boost enable signal, the active negative or positive drive signal applied to the integrator increases in amplitude to produce a sharper slope for the drive signal applied to the integrator. The integrator output, in turn, has a sharper rising or falling slope that enables the reconstructed analog signal voltage to increase at a greater rate. Once the boost requirement is satisfied, the boost enable output from the logic decoder output returns to its normal decreased drive state until the next series of three ones or zeros is applied 'from the 3-bit shift register.

5-451. Figure 5-21 illustrates the relationship of the data pulses to the reconfigured analog signals. The figure also shows the filtered analog signal superimposed over the reconstructed analog signal output from the integrator. The filtered analog signals from the bandpass filter circuit are applied to the output amplifier-drivers circuit. The output amplifier-drivers circuit, in turn, amplifies and produces the balanced voice channel data output signals DOXX and DOXX-.

5-452. Diagnostic Circuits. The error detector circuit samples voltage levels from the bandpass filter and the output amplifier-drivers circuit. The circuit configuration is such that a failure in one area causes most of the circuitry to saturate in one direction. When a circuit is faulty and a saturation condition occurs, an error signal is applied to the diagnostic control circuit. The diagnostic control circuit, in turn, generates card error signal on the positive stuff request (DPSTXX-) line unless an inhibit signal is applied to it from the loss-of-data multivibrator or from the delay start multivibrator. The loss-of-data multivibrator is a retriggerable one-shot multivibrator that is held in conduction by the incoming data pulses. When the data pulses are missing, the multivibrator duty cycle expires and an inhibit signal is produced to prevent the generation of an erroneous card error signal. The delay start multivibrator generates an inhibit signal to the diagnostic control circuit for 2.7 seconds when the VD card is initially energized. The inhibit signal prevents an erroneous card error signal from being generated when the equipment is first turned on and when data and timing signals are absent.

5-453. DETAILED CIRCUIT DISCUSSION.

5-454.Functional Circuits.

5-455. The incoming channel data pulse DTIX- are applied through inverter U7-4 to 3-bit shift register U4-6, U4-10, U5-10.The data bits are clocked into the shift register by gated clock signals DGCXX applied through inverter U7-6 to the shift register. The data bits (bit 1) in the shift register are applied through inverter U7-2 to the base circuits of negative inhibit switch Q2 and positive inhibit switch Q3. When the output of the inverter is low, Q2 is enabled and effectively grounds the negative output from slope control U3-10 to the negative input (pin 7) of U2-10. The condition allows the positive drive voltage from slope control amplifier U3-12 to drive integrator U2-10. In turn, a high output from U7-2 enables positive inhibit switch Q3 and effectively grounds the positive output from slope control amplifier U3-12 to the negative input of integrator U2-10. In turn, this condition allows the negative drive voltage from slope control U3-10 to drive integrator U2-10. Therefore, the output from U2-10 varies in relationship to the polarity of the drive voltages applied to input pin 7 from U3-10 or U3-12.

5-456. The Q and Q outputs from the 3-bit shift register are applied to AND gates U6-6 and U6-12 in the decoder logic. When the three Q outputs or the three Q outputs are all high, one of the two AND gates is enabled and produces a signal through inverter U7-12 that biases Q1 off in the slope control circuit. This condition drives the voltage applied to pin 7 of U3-10 more positive. In turn, the output from U3-10 goes more negative and the output from U3-12 goes more positive. Therefore, the positive or negative drive applied to pin 7 of U2-10, in turn, causes the integrator output voltage to vary with an increased (positive-going or negative- going) slope effect on the reconstructed analog signal being developed. As soon as the decoder logic detects the condition wherein the three bits being monitored are not all zeros or ones, Q1 is biased back into conduction, reducing the dc bias level to pin 7 of U3-10.

The result is a decreased drive voltage to integrator U2-10, thus decreasing the slope of the analog signal being reconstructed.

5-457. Bandpass filter circuit U2-12, U1-10 forms a bandpass filter that re- moves the high-frequency quantizing noise present at the output of U2-10. The 3-dB bandpass of the bandpass filter is from 140 to 3500 Hz. The response of this bandpass filter is that of a low-pass elliptic filter followed by a Butterworth bandpass filter. The set- ting of amplitude control R36 is factory preset to produce a +7-dBm output for a -16-dBm input. The reconstructed analog voice signals are applied through out- put amplifier U1 to push-pull driver circuit Q4, Q5. The voice output signals are developed as channel data out- put signals DOXX and DOXX- from the 600-ohm output of audio transformer T1.

5-458. Diagnostic Circuits.

5-459. Transistors Q7 and Q8 are normally cut off and Q9 is conducting. When an error condition is detected, either Q7 or Q8 is forced into conduction and, in turn, Q9 is biased into cutoff. When Q9 is cut off, an enable signal is applied to one input of AND gate U9-12. When the three inputs to U9 are high, the low output from U9 is applied through OR gate U9-6 and inverter U9-8 to generate a card error signal that is applied on the positive stuff request (DPSTXX-) line to the OEG card. When the incoming data are missing, loss-of-data multivibrator U8-6 produces a low inhibit output to AND gate U9-12. This circuit prevents an erroneous card error from being generated by loss of data. Multivibrator U8-6 is a retriggerable one-shot multi- vibrator that is held in conduction by the incoming data pulses. Once the pulse inputs are removed, the multi- vibrator duty cycle expires and generates the inhibit (low) output. Delay start multivibrator U8-9 is triggered on for 2.7 seconds by the low Q output from Q8-6 when the equipment is first turned on to prevent an erroneous diagnostic indication to be generated from the VD card.

5-460. SEQUENCER (SEQ) CARD.

5-461. The seq card used in the demultiplexer is the same card type as that used in the multiplexer. The seq card requires no functional modifications for use in the demultiplexer. The seq card logic diagram and the block diagram in figure FO-3 identify the in- put and output signals that are applicable to the multiplexer function, and those that are applicable to the demultiplexer function. The signals pre- fixed by a D are applicable to the de- multiplexer, and those prefixed by an M are applicable to the multiplexer. Those signals not prefixed by a D or an M are used in both the multiplexer and the demultiplexer. There is one exception; maximum channel number signals CHMAXO through CHMAX3 are used by the seq card only in the multiplexer and not in the demultiplexer.

5-462. Functional operation of the logic circuits on the seq card in the demultiplexer is the same as that de-scribed for the seq card in the multiplexer, with one difference. When the equipment is initially turned on or frame synchronization has been lost, the frame synchronization circuits on the FS card generate and supply frame sync signal DSYNC- to the seq card. Signal DSYNC- is produced on the FS card as part of the resynchronization function that involves the GC/DM and seq cards. Signal DSYNC- is applied through inverters U4-2, U4-12, OR gate U15-11, and inverter U4-8 to preset port scan counter U2, U3 to a count of five. The count four input to U2 is held high at this time by signal DSYNC- applied through inverter U4-2. At the same time, flip-flops U21-5 and U21-9 in the end-of-scan signal generator circuits are cleared. Write port scan counter U9, U22 is preset to a count of three by the low output from inverter U4-10 applied through OR gate U15-8 and inverter U24-12 to the preset input of U9, U22.

The count three is produced by the high inputs to the count one and count two preset inputs on U9 from inverter U4-2. The circuits just de- scribed are reset to ensure that the next end-of-scan timing signals are produced at the proper time when the next A=B signal is generated from ports- in-use comparator U34.

5-463. GATED CLOCK/DATA MUX (GC/DM) CARD.

5-464. The GC/DM card used in the de- multiplexer is the same card type as that used in the multiplexer. The GC/ DM card requires no functional modifications for use in the demultiplexer. As described in the following discussion, all the circuits on the GC/DM card are not used in the demultiplexer. The GC/ DM card logic diagram identifies the input and output signals that are applicable to the multiplexer function, and those that are applicable to the demultiplexer function. The signals prefixed by a D are applicable to the demultiplexer, and those prefixed by an M are applicable to the multiplexer. Signals not prefixed by a D or an M are used in both the demultiplexer and the multiplexer. The following detailed circuit discussion supplements the GC/ DM card theory of operation in para- graph 5-306.

5-465. In the format generation function, word counter preset signal DWPR- is applied to inverter U15-8 when the equipment is initially turned on or frame synchronization has been lost. Signal DWPR- is produced on the FS card as part of the resynchronization function that involves the seq and GC/DM cards. The signal is applied through inverter U15-8, U13-6, OR gate U4-6, and inverter U13-2 to preset count 12 into word counter U5, U14. When the next end-of-scan signal DEOS2B- is applied to the GC/DM card, word counter U5, U14 is incremented to produce word count 12 to read only memory (ROM) U20. In turn, U20 generates bit 12 of the DNAC, DNSC, and DPSC signals to the FS card at this time. Count 12 is also applied through word count signals DWCO through DWC4 to the OEG card at this time.

5-466. In the gated clock generation function, gated clock signals DGCO1 through DGC15 are applied to the de- multiplexer channel cards. Overhead count signals DOHO through DOH3 apply overhead address signals to the display card and the OEG card. In turn, de-multiplexer channel address binary signals DCHA1 through DCHA8, which select the channel to be serviced at a given time, are supplied from the seq card.

5-467. The data multiplexer functional circuits on the GC/DM card are not used in the demultiplexer function. Functional operation of the diagnostic circuits on the GC/DM card in the demultiplexer is the same as that in the multiplexer.

5-468. OVERHEAD ENABLE GENERATOR (OEG) CARD.

5-469. The OEG card used in the demultiplexer is the same card type as that used in the multiplexer. The OEG card re- quires no functional modifications for use in the demultiplexer. As described in the following circuit discussion, all the circuits on the OEG card are not used in the demultiplexer. The OEG card logic diagram identifies the input and output signals that are applicable to the multiplexer function, and those that are applicable to the demultiplexer function. The signals prefixed by a D are applicable to the demultiplexer and those prefixed by an M are applicable to the multiplexer. Those signals not prefixed by a D or an M are used in both the multiplexer and the demultiplexer.

5-470. In the demultiplexer, the negative stuff multiplexers are not used.

Positive stuff multiplexers No. 1 (U3) and No. 2 (U4) are only used in the diagnostic function for routing demultiplexer channel card errors to the display card. Positive stuff request signals DPSTO1 through DPST15 contain the diagnostic error status of the channel cards in the demultiplexer. The error signals applied to U3 are serially multiplexed into positive stuff acknowledge signal MPSA- that is applied to the display card. Overhead address signals DOHO through DOH3 from the GC/DM card contain the 4-bit channel addresses that select the one channel card diagnostic input that is applied to multiplexer U3 during each minor frame period.

5-471. Operation of the end-of-scan generation circuits and the word 24 generation is the same as that described for the OEG card in the multiplexer. The system clock signal circuits that generate system clock signals MRIO1- through MRI08- are not used in the de-multiplexer application. System clock activity detector U12 monitors demultiplexer input system clock signal RI from the FS card and generates error signal DLOT- when the signal is missing.

5-472. FRAME SYNC (FS) CARD.

5-473. GENERAL. The FS card is a demultiplexer common card that performs a timing function and an overhead function. A frame synchronization function is performed to synchronize the demultiplexer timing generation circuits with the incoming data stream timing. A stuff command decode function on the FS card decodes one of the three stuff command codes (negative stuff, positive stuff, or no action) contained in the overhead message during each minor frame period.

5-474. BLOCK DIAGRAM DISCUSSION.

5-475. The overall simplified block diagram discussion for the FS card divides the circuits into two major circuit groupings: the parallel sync acquisition circuits and the serial sync acquisition and sync maintenance circuits. Functionally, the sync acquisition circuits establish frame synchronization when the equipment is initially energized and reestablishes frame synchronization when a loss of frame synchronization is detected during normal operation. The frame sync maintenance circuits continually monitor for frame synchronization during normal operation. The functions performed by these circuits are keyed to the stuff command code contained in bit 0 of words 1 through 23 of the overhead message as described in the following paragraphs.

5-476. Overall FS Card Discussion (Figure FO-6). The parallel sync acquisition circuits establish frame synchronization when the equipment is initially energized and when frame synchronization is lost during operation. The input data pulses (DATA) are clocked through the input data shift register by its own externally applied timing signals (TIM) to the variable length shift register (VLSR). The VLSR temporarily stores 10 consecutive incoming data words and applies one bit at a time from each word (same bit number in each word) to the three code comparator circuits. Each of the three code comparators per- forms an A=B compare search for the first 11 bits in one of the three stuff command codes contained in words 1 through 11 in the incoming overhead data message. The 11th bit (B11) is applied on- line (not stored) to an input on each of the three code comparators.

5-477. Before frame synchronization is obtained, signals Bl through B10 can be in any, bit location within each of the 11 data words being sampled. The fixed B input to each code comparator circuit represents the first 11 bits of the stuff command code with which it is associated. These codes are described in paragraph 5-14. At the time that a compare is made in one of the three code comparators, B1 through B11 will contain bit 0 of words 1 through 11. At this time, the parallel sync control circuits are activated.

The parallel sync control circuits, in turn, generate de-multiplexer frame sync signal DSYNC-, parallel sync enable, and one of the enable signals (PSC, NSC, and NAC). Signal DSYNC-, which lasts one data bit time, is generated to initiate demultiplexer timing signals so that bit 0 of word 12 in each of the stuff code commands (DPSC, DNSC, and DNAC) is applied to the FS card at the same time that bit 0 of word 12 in the incoming data stream (MDS-) occurs. Signal PSC enable, NSC enable, or NAC enable and the parallel sync enable signals enable the serial sync acquisition function in the serial sync acquisition and sync maintenance circuits. Signal DSYNC- is also applied as a reset signal to the three bit error counters in the serial sync acquisition and sync maintenance circuits.

5-478. In bit 0 of words 1 through 11, the appropriate stuff code command has been determined and an enable signal has been applied to the appropriate bit error counter. Therefore, when signal DSYNC- is initiated and the timing circuits in the demultiplexer circuit are synchronous with the incoming data stream, only one of the three code comparator-error detectors in the serial sync acquisition and sync maintenance circuits is enabled to perform a valid serial compare of bit 0 in words 12 through 23 (B12 through B23). When proper frame synchronization is obtained, the appropriate (positive stuff, negative stuff, or no action) code comparator-error detector should detect less than three errors while monitoring bit 0 in words 12 through 23. If three or more errors are detected, an error reset signal is generated to restart the parallel sync acquisition function. When frame synchronization is maintained through word 23, word 28 signal W28 removes the parallel sync enable signal and produces demultiplexer frame sync signal DFS from the control circuits. At this time, enable signal PSC, NSC, or NAC applied to the selected error counter is also removed.

5-479. Signal DFS indicates that the sync acquisition function is complete and the serial sync acquisition and sync maintenance circuits are performing the frame sync maintenance function. In the frame sync maintenance function, bit 0 in words 1 through 23 of each minor frame is compared against the same bit in each of the three stuff command codes applied from the GC/DM card. The serial overhead message in bit 0 of words 1 through 23 of the incoming data (MSD-) is applied to the three active code comparator-error detector circuits. At the same time, one of the three stuff code commands generated in the GC/DM card is applied to each of the three circuits. When frame synchronization is proper, one of the three bit error counters contains an error count of seven or less and enables a count up output through an OR gate to the error up/down counter. In normal operation, the other two bit error counters associated with the two stuff commands not in a given overhead message produce a maximum error count output. All three bit error counters must contain an error count of eight or more during a given minor frame period to produce a count down input through the OR gate to the error up/down counter. The up/down counter prevents a loss-of-frame status when a limited number of overhead data bits is missing or incorrect in the compare function. At the end of each minor frame period, word 29 signal W29 resets the bit error counters to a count of zero for the next compare function performed in the next minor frame period.

5-480. The error up/down counter is initially set to a count of five at the end of the sync acquisition phase. The maximum count retained in the counter is a count of five. When a count up signal is applied to the counter during word 28 of each minor frame period, the counter only counts up when it contains a count between one and four.

In turn, the count decrements one count each time a count down signal is applied during word 28 when the counter contains a count between 1 and 5. When the counter counts down to zero, the count 0 signal is applied to the control circuits. The control circuits, in turn, remove signal DFS and initiate demultiplexer loss of frame signal DLOF that is applied to the ERD card. When signal DFS is removed, the inhibit signal to the parallel sync acquisition circuits is removed and that function is activated to reestablish frame synchronization.

5-481. Signal DFS is applied as an en- able signal to the channel output data shift register while frame synchronization is maintained. The channel out- put data shift register, in turn, generates four identical channel data outputs (DTI1 through DTI4) that apply the channel data to each of the de- multiplexer channel cards. When frame synchronization is lost, the data out- puts are inhibited.

5-482. The PSE and NSE flip-flops pro- duce negative or positive stuff enable signal DNSE or DPSE to identify the stuff command code contained in the minor frame being monitored. When the error count in the positive stuff code bit error counter is less than eight, the PSE flip-flop produces signal DPSE during word 28. Signal DPSE indicates the presence of a positive stuff command that is applied to the ERD and GC/ DM cards. When the error count in the negative stuff code bit error counter is less than eight, the NSE flip-flop produces signal DNSE during word 28 to indicate the presence of a negative stuff command. When both counters contain error counts of eight or more, both output signals are low during word 28 to indicate the presence of a no-action stuff command.

5-483 Parallel Sync Acquisition Circuits Block Diagram Discussion (Figure 5-36). The input data pulses (DATA) applied to the data receiver are conditioned into TTL level pulses and applied to the data flip-flop. In turn, the incoming timing pulses (TM) are conditioned in the timing receiver and applied to the data flip-flop, channel data output shift register, and inverter U63. Inverter U63 produces the RIO and RIO- system clock signals used in the FS card. The data pulses clocked through the data flip-flop are applied to the channel data output shift register and to the data shift register. When frame synchronization is established, demultiplexer frame sync signal DFS is applied as an enable signal to the channel data output shift register. This prevents erroneous channel data signals DTI1- through DTI4- from being applied to the channel cards.

5-484. Sequential data outputs SD2, SD3, and SD3- from the data shift register are applied to the VLSR. The VLSR, which temporarily stores 10 consecutive data words to provide a 10-word delay, generates parallel data inputs Bl through B10. The 10 parallel data bits are applied to three code comparator circuits. The SD3- data output from the data shift register is applied in real time (no delay) as data input Bll to the three code comparator circuits at the same time that Bl through B10 are applied in parallel. The VLSR is clocked by sys- tem clock signal RIO- so that one set of 10 bits in 10 sequential data words is applied to the three comparators at the system clock rate. For example, bit 5 in words 1 through 11, bit 6 in words 1 through 11, bit 7 in words 15 through 25, etc, are each applied during one RIO time to the comparator circuits. A separate block diagram discussion of the VLSR functional circuits is contained in paragraphs 5-487 through 5-501.

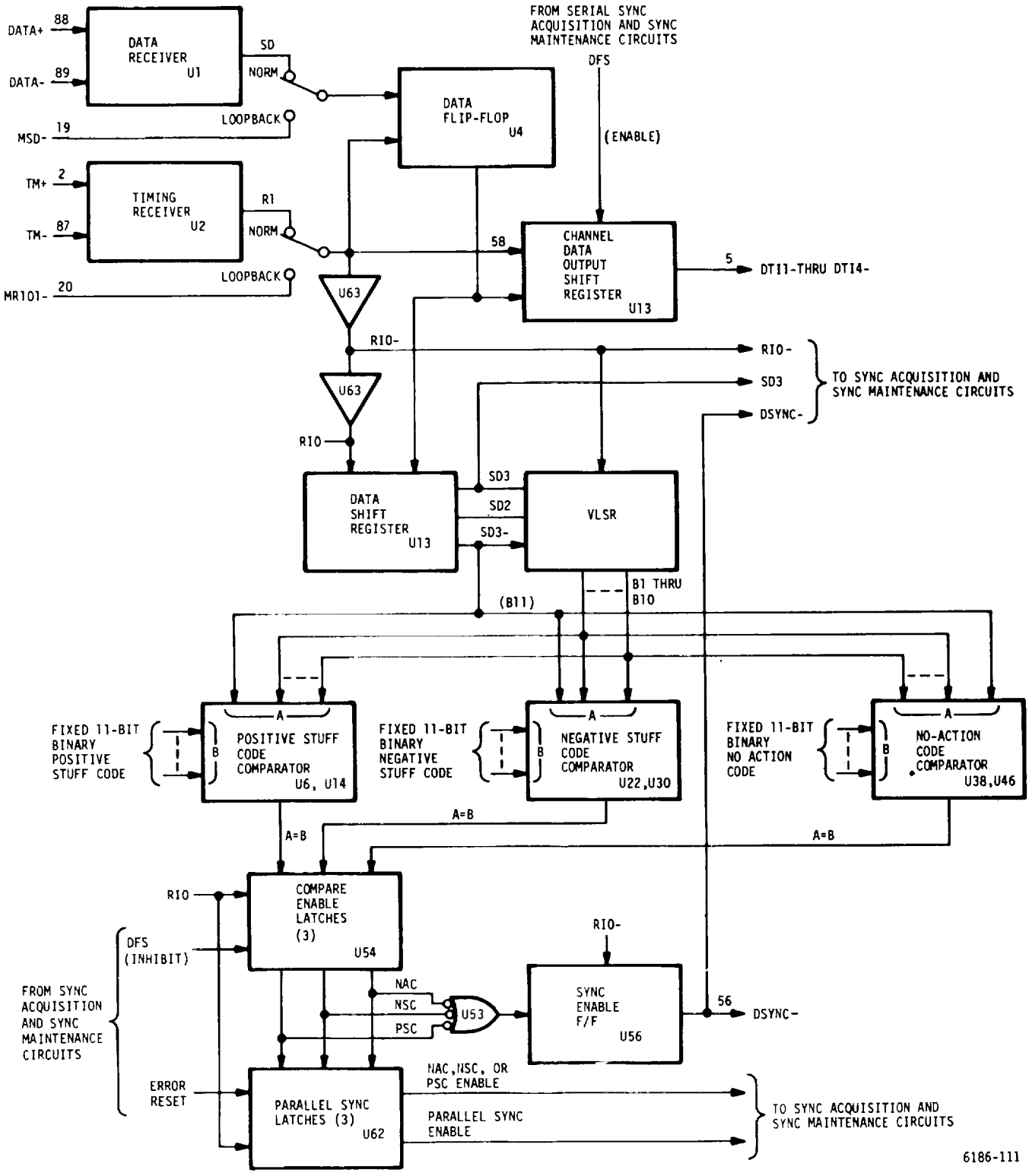


Figure 5-36. FS Card, Parallel *Sync Acquisition Circuits - Block Diagram*

5-485. Each of the three code comparators has a fixed 11-bit binary code that represents the first 11 bits of one of the three stuff commands that can be applied to the comparator. The fixed 11-bit code is applied as the B input to each comparator and is compared against the Bi through Bll inputs applied to the A inputs of all three comparators. An A=B output from one of the three comparators is applied to the com- pare enable latches when a compare is made during word 11. A compare is made when B1 through Bll are bit 0 of overhead words 1 through 11.

5-486. One of the three compare en- able latches is set to produce signal NAC, NSC, or PSC enable when the appropriate A=B signal is applied from one of the three code comparators. The output signal is applied through an OR gate and is then clocked through the sync enable flip-flop as frame sync signal DSYNC- for one RIO clock period. The appropriate NAC, NSC, or PSC signal is also applied to one of the three parallel sync latches to produce the NAC, NSC, or PSC enable signal and the parallel sync enable signal. Once the overall frame synchronization is established, signal DFS holds the compare enable latch circuits inhibited. When the serial sync acquisition portion of the sync acquisition function performed by the serial compare circuits in the serial sync acquisition and sync maintenance circuits during words 12 through 23 is not satisfactory, an error reset signal from those circuits clears the parallel sync latches and the parallel sync acquisition function is repeated during the next minor frame period.

5-487. VLSR Concept Discussion. The VLSR provides a 10-word delay function so that one data bit in a given bit location in 10 consecutive words can be sampled in parallel. Therefore, each of the data bits sampled is separated from its adjacent bit, in time, by one data word time. The delay between consecutive words in a given application is equal to n+l, where n is a value between 15 and 31 bits. To meet the different equipment requirements, the VLSR provides the storage locations necessary for the 160 to 320 bits to service the 10 words. The VLSR has primary and odd- bit shift registers that provide the flexible storage requirements for the various system applications. The primary shift register is a 16 to 32-bit programmable shift register that per- forms a serial-in, parallel-out function. The parallel-out function produces in sequential rotation between 16 and 32 bits of data, one bit at a time, from the same bit location in each of 10 consecutive words. The odd-bit shift register provides one bit of data from the same bit location in each of 10 consecutive words. The primary shift register is used when the number of ports in use in a given system configuration is an odd number of ports (n+1 is even). When the number of ports in use is an even number of ports (n+1 is odd), both shift registers are used to process the data bits.

5-488. Figure FO-7 is a simplified block diagram of the primary shift register circuits that process the data bits in the first two words applied to the VLSR. R.A.M. No. 1 and storage register No. 1 basically form the shift register circuits that produce selected bits B1- and B2 that represent a given bit in words 1 and 2. R.A.M. No. 1 is a 64-bit storage device configured for four inputs, with 16 memory locations associated with each input. Data bits SD3 and SD2 are clocked in parallel into the R.A.M. from the data shift register in the parallel sync acquisition circuits. Data bits SD3 (bit 1) and SD2 (bit 2) are a pair of consecutive bits of the incoming data stream applied to the demultiplexer. This pair of data bits is clocked into inputs DO and D1 once every other RIO-time, or at a one-half clock rate (RIO/2). Each memory location is sequentially selected so that 32 data bits can be clocked into the 32 memory locations associated with inputs DO and D1 during 16 consecutive write enable times. Inputs DO and D1 store the same number of data bits during a given data word scan.

Since pairs of data bits are applied and stored at the one-half RIO rate, over a period of 16 write enable commands, the two inputs contain the maximum (n+1 = 32) consecutive data bits of a given data word. The logic application permits the VLSR to operate at a desirable slower rate that is one-half the rate (R_o) at which the incoming data stream is applied to the demultiplexer.

5-489. When the write sequence is generated, the four data bits being read out of four parallel memory locations in the R.A.M. are latched into the storage register just before the write function occurs in the R.A.M. Therefore, when the write enable signal occurs, the data bits read out of the memory locations associated with inputs D0 and D1 are written into the same memory locations associated with inputs D2 and D3. The memory locations associated with inputs D0 and D1 write in the incoming SD3 and SD2 data to the VLSR. This almost instantaneous write/read sequence causes the data bit written into the parallel memory location associated with input D0 to be delayed one data word time from the data bit being written into the equivalent data bit associated with input D2. In turn, the SD2 data written into the D1 memory location is delayed one data word time from the data bit written into the equivalent D3 memory location. As shown in figure FO-7, for example, the data bit in memory location 5 for input D0 is bit 9. In the next write cycle, bit 9 is read out and written in the same memory location (bit 9) for input D2. This is a 32-bit, or one word time, delay for an equipment application using an n+1 of 32.

5-490. During normal operation in a 32- bit word application, the 4-bit address is truncated after memory location 16 is addressed and the next memory location to be addressed is location 1. To show the versatility of the shift register, assume that a 24-bit word is used. Only the first 12 memory locations associated with the four data inputs DO through D3 are addressed. After memory location 12 is addressed, the 4-bit address is truncated and the next memory location ad- dressed is location 1. In this configuration, a 24-bit delay exists between the data bit for a given memory location associated with inputs DO and D2. There- fore, the data in the parallel memory locations associated with inputs DO and D2 or D1 and D3 are always delayed one word time (24 bits) apart. The truncation occurs when the 4-bit address is the same binary code that is applied to the address comparator using ports- in-use signals DPUB1 through DPUB4. The A=B compare signal from the address comparator resets the 4-bit counter output to zero when N+l is an even number.

5-491. The four parallel data bits applied through storage register No. 1 to the A and B inputs of data selector No. 1 are always from the same row of memory locations (DO, D1, D2, and D3) in the R.A.M. In turn, the A and B inputs are alternately selected at the RIO rate. Therefore, the outputs from both B1 and B2 will be a sequential readout in the same order in which serial data bits were originally applied to the data shift register in the sync acquisition circuits. Also, the bit delay between the bits in B1 and B2 are always one word time apart. For example, while the B1 outputs are bit numbers 1, 2, 3, 4, 5, 6, 7, the B2 outputs are bit numbers 1, 2, 3, 4, 5, 6, 7. This illustrates the 32-bit delay when the equipment is configured for a 32-bit data word.

5-492. The 3Q and 4Q outputs from the storage register are applied in parallel to DO and D1 on R.A.M. No. 2 in the VLSR. The procedures are repeated again in R.A.M. No. 2 and storage register No. 2 to establish B3 and B4 outputs and provide an additional two-word (words 3 and 4) delay.

The procedure continues through R.A.M. No. 5 to obtain the de- sired B1 through B10 outputs that form the complete 10-word delay.

5-493. Figure 5-37 shows the odd-bit shift register and the primary shift register in an odd-bit application. The operation of the primary shift register in this equipment configuration is the same as described previously, with one exception. When the address comparator makes a compare, the A=B signal presets the primary shift register to a count of one instead of zero. Note that the address comparator has only the four MSB's of the ports-in-use signals (DPUB1 through DPUB4) applied to select the count that causes the 4-bit address counter to truncate. Therefore, a binary count of 1111 applied to the address comparator could be part of binary count 31 or 32. When the 4-bit address counter is preset to a count of zero, the truncation occurs after 16 addresses and access to 32 data bit locations in the R.A.M. have been performed. This would be satisfactory for a 32-bit application, but not for the maximum 31-bit application in this equipment. In turn, presetting the address counter to a count of one limits the maximum truncation to occur after 15 addresses and access to 30 data bits to the R.A.M. have been performed. After the A=B condition is obtained in the odd-bit con- figuration, the primary shift register operation is delayed for one RIO time while one odd data bit is processed as described in the following paragraph.

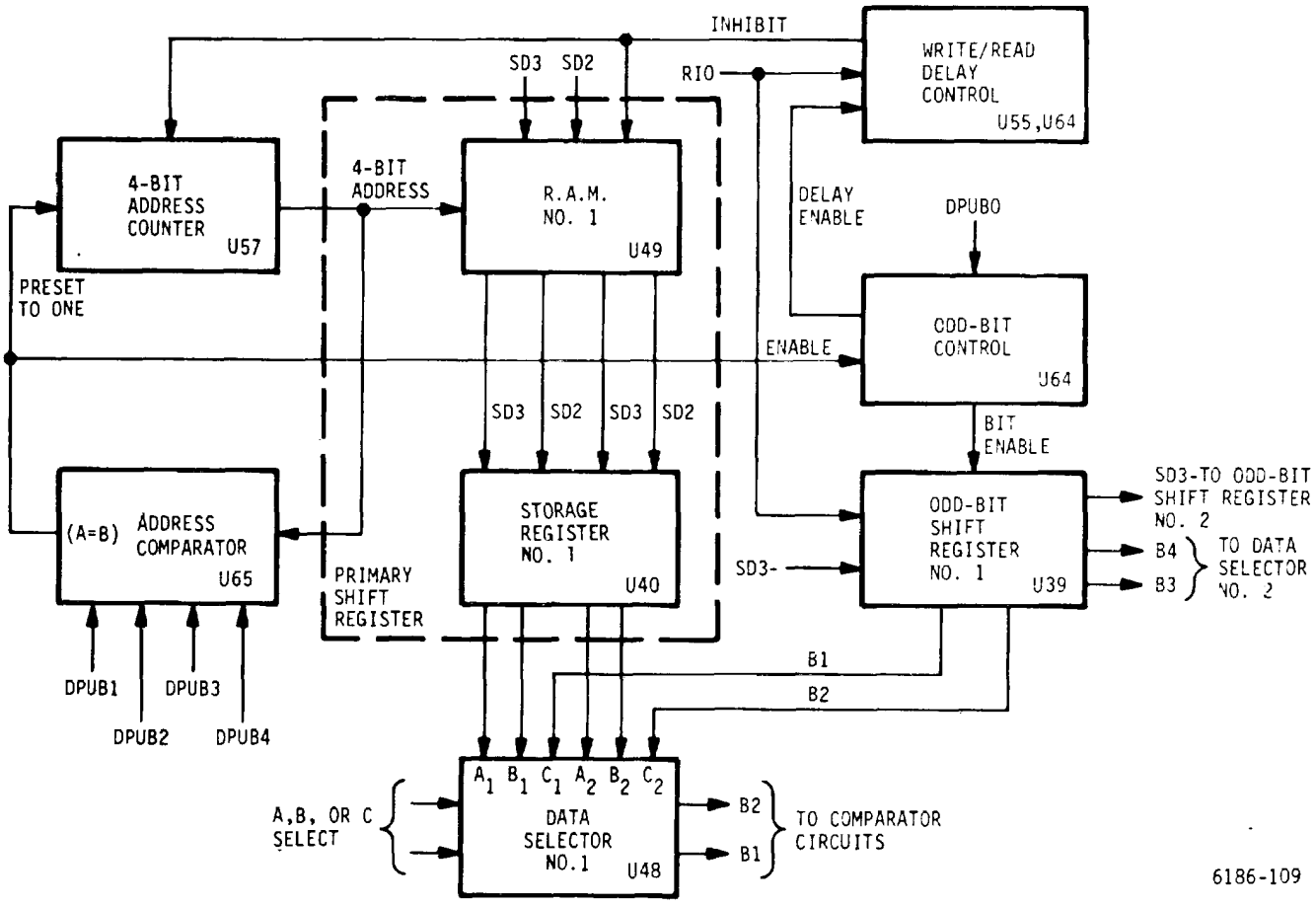


Figure 5-37. FS Card, Primary and Odd Bit Shift Registers - Block Diagram

5-494. The data outputs from the primary shift register for an even number of bits are processed through the A and B inputs of the data selector at the system RIO rate. After the last programmed data output is processed, the A=B signal from the address comparator is applied as a preset-to-one signal to the 4-bit address counter and as an en- able signal to the odd-bit control circuit. When LSB signal DPUBO is a 1, representing an odd number (1, 3, etc), the odd-bit control is inhibited and the C input signal to the data selector is inhibited to program the VLSR for operation in the even-bit mode. When LSB signal DPUBO is a 0, representing an even number, the odd-bit control circuits are enabled when the enable signal is applied from the address comparator. At this time, a delay enable signal applied to the write/read delay control circuit inhibits the 4-bit address counter and the R.A.M. read and write controls for two RIO clock times. This condition effectively delays the first write enable input to the R.A.M. for one RIO time. (The write enable is normally every other RIO time.)

5-495. At the same time that the delay enable signal is generated, the bit enable signal is applied to the odd-bit shift register, one data bit (SD3-) is written into the register, and the stored data bits in the register are serially clocked one step. At the same time, the C select signal enables the B1 and B2 data bits from the shift register to be routed through the C inputs of the data selector to the code comparator circuits. After the two RIO times expire, the inhibits to the 4-bit counter and R.A.M. are removed and the even data bit process in the primary shift register is repeated.

5-496. The preceding paragraphs describe the basic equipment operation of the primary and odd-bit shift register circuits. The following discussion illustrates the timing relationships required when both shift registers are used to service a data word containing an odd number of data bits. In this example, the primary shift register that services data words containing 16 data bits is described first, followed by the primary shift register and odd-bit shift register that service data words containing 17 data bits. In the even-bit mode servicing 16 data bits, part A in figure 5-38 shows the primary shift register waveforms. Note that the R.A.M. write enable signal is generated once every two RIO clock times and the timing sequence is not altered when the data word bit count is completed and the A=B signal truncates the 4-bit address counter to start servicing the next data word. The timing waveforms in part A of figure 5-38 show that eight write enable signals are generated during one word time equivalent to 16 data bits. Each write enable writes one pair of SD3 and SD2 bits into the R.A.M. In turn, eight SD3 and eight SD2 data bits are read out of data selector output B1, therefore providing 16 consecutive data bit out- puts for each 16 data bit inputs.

5-497. The waveforms in part B of figure 5-38 represent the primary and odd- bit shift register in a configuration that services data words containing 17 data bits. Note that eight write enable signals are still being generated during one word time for the R.A.M. In turn, 16 data bits associated with the eight write enable signals are still being generated. The half-rate clock output is inhibited for one RIO time after the A=B signal is generated. It is during this delayed one-half rate clock time that the odd-bit enable clock signal is generated and the odd bit of data (SD3-) is placed in series with the SD3 and SD2 data bits. This application provides 17 consecutive data bit outputs for each 17 data bit inputs in the data selector output.

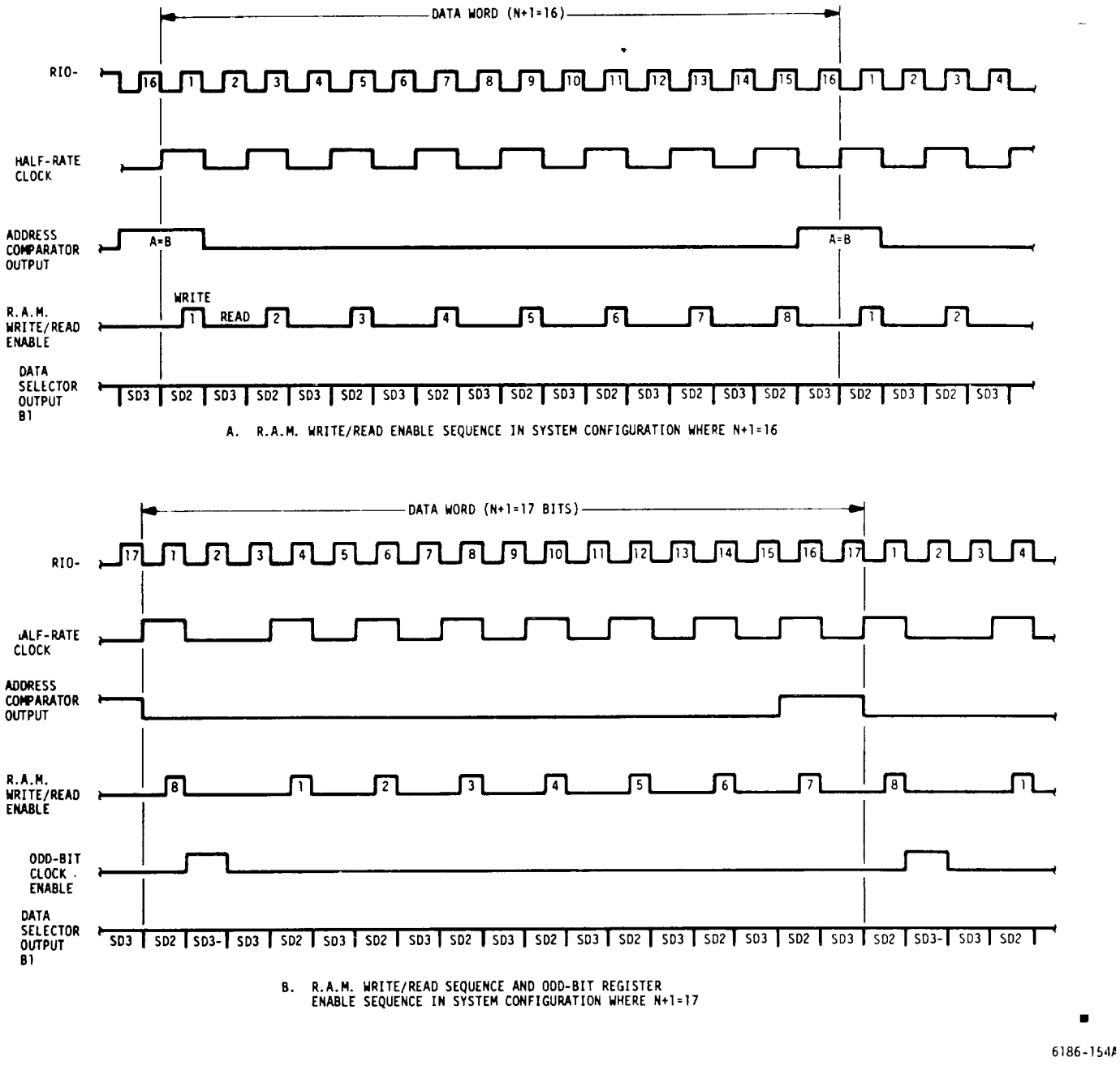


Figure 5-38. FS Card, Data Selector Outputs - Waveform Diagram

5-498. VLSR Block Diagram Discussion (Figure FO-8). In the following block diagram discussion of the VLSR, the circuits configured to process data words with an even number of bits are described first. After this discussion, the circuits configured to process the data words with an odd number of data bits are described to show the insertion of the odd bit of data in the parallel readout of bits 1 through 10 from the VLSR.

5-499. When the LSB of the ports in use signal (DPUBO) from the seq card is a 1, the VLSR operates in the mode that processes an even number of data bits when n+l is an even number (18, 20, 24, etc). At this time, the odd-bit circuits are inhibited. The half-rate clock generator is clocked by system clock signal RIO- and produces the half-rate clock signals applied to the 4-bit ad- dress counter and the parallel storage registers in the primary shift register. When the count (4-bit address) from the counter reaches the count contained in signals DPUB1 through DPUB4 applied to the address comparator, an A=B condition is generated to produce the signal that presets the 4-bit address counter out- put to a count of zero. For example, an RIO of 2400 kHz produces 4-bit ad- dress signals to R.A.M.'s No. 1 through No. 5 at a rate of 1200 kHz.

5-500. The five R.A.M.'s in the primary shift register are identical. Each R.A.M. performs a read and write function for two pairs of parallel SD2 and SD3 data inputs. Each of the four data inputs has a maximum of 16 memory locations in a R.A.M. to process up to 16 odd- or even-numbered data bits in a given data word application. In normal operation, the first pair of SD2 and SD3 is combined and becomes output B1 and the second pair of SD2 and SD3 is combined and becomes output B2 from the VLSR. When the half-rate clock-signal from the half-rate clock generator is applied, the 4-bit address counter is incremented one count and the next sequential address is applied to the five R.A.M.'s. At this time, the R.A.M.'s have read signals applied. When the half-rate clock signal is generated, the storage register latches the four data outputs from the R.A.M. An instant later, the write enable signal-is applied to the R.A.M. and the parallel SD2 and SD3 data bits applied to the DO and D1 inputs are written into the same address that was just read. In turn, the SD2 and SD3 data bits latched into storage register locations 1D and 2D are applied to the second set of D2 and D3 inputs of the same R.A.M. and are written in the equivalent memory locations. This operation is serially per- formed on SD2 and SD3 data bits applied to the other R.A.M.'s in the VLSR. Each of the data bits latched into the storage registers is also applied to the A1, B1, A2, or B2 input of a data selector. There are five data selectors in the VLSR, each generating two bits of the 10-bit parallel output (B1 to B10) to the stuff command code comparators. The A and B select signals applied to the data selector are programmed to alternately select A1 and B1 inputs for out- put signal B1, and A2 and B2 inputs for output signal B2. Each output is enabled for one system clock RIO time. The result is that consecutive data bits for a given data word configuration appear at the B1- output and consecutive data bits, delayed one data word, are produced from the B2 output.

5-501. When the LSB input of ports-in- use signal DPUBO from the seq card is a zero, the VLSR operates in the mode that processes an odd number of data bits when n+l is an odd number (19, 21, 25: etc). At this time, the circuits that generate the odd bit are enabled to process the odd data bit that is added in series with the data bit output from the primary shift register. The circuits specifically associated with the odd-bit logic are identified on the block diagram in figure FO-8 by heavy lines. The odd-bit function is enabled when the 4- bit address counter produces the maxi- mum count necessary to generate an A=B output from the address comparator. The AND gate produces an enable signal to the odd-bit control circuit when the A=B and the half-rate clock- signal are present. The odd-bit control circuit generates an inhibit signal that delays the next generation of the R.A.M. read and write signals for two RIO times while the odd data bit from each odd bit shift register is generated. During the RIO time that is inhibited in the primary shift register function, the odd-bit address select flip-flop produces a clock signal that clocks in the data bit (SD3-) applied to odd-bit shift register No. 1.

At the time that signal SD3- is clocked into odd-bit shift register No. 1, the four bits of data in each of the three registers are shifted one bit. At this time, the half-rate clock- signal and the odd-bit enable signal are applied to the A and B ad- dress inputs of the five data selectors. The C1 and C2 inputs are enabled so that the parallel B1 through B10 outputs contain a parallel readout of the odd data bit. In the next RIO time, the primary shift register is enabled and processes the next consecutive sets of data bits whose total is an even number of bits between 16 and 32.

5-502. Serial Sync Acquisition and Sync Maintenance Circuits Block Diagram Discussion (Figure FO-9). In the sync acquisition function, signal DSYNC- resets the three bit error counters to zero. At the same time, the parallel sync enable signal is applied to one input of the AND gate in the input circuit of the frame sync flip-flop. The enable signal remains until signal DFS is generated as described in the following paragraph. The data in bit 0 of words 12 through 23 in data input SD3 from the parallel sync acquisition circuits are clocked through the data-in flip-flop to the three code comparators. Bit 0 is selected by a combination of clock signal RIO and demultiplexer end-of-scan signal DEOS2 that enable an AND gate to clock the data-in flip-flop. The over- head data pulses (bit 0) are also applied as overhead data signals DOD- to the ERD card.

5-503. When parallel sync acquisition is obtained, signal DSYNC resets the three bit error counters to zero and only one of the bit error counters is enabled by signal PSC enable, NAC en- able, or NSC enable. Starting with bit 0 of word 12 of the incoming data, the selected bit comparator compares bit 0 in data words 12 through 23 with the equivalent bits applied in signal DPSC, DNAC, or DNSC. When proper frame synchronization is achieved, the 12 bits sampled should compare. When the comparator detects three or more errors during words 12 through 23, the associated error counter generates an error reset signal that is applied through OR gate U60 to the parallel sync acquisition circuits. This condition initiates another parallel sync acquisition function and inhibits the start of the sync maintenance function. At the same time, the parallel sync enable signal applied to the AND gate is removed and the frame sync flip-flop cannot generate signal DFS. When two or less errors are counted during words 12 through 23, the error reset signal is not generated and the input to the, AND gate remains enabled. When word 28 timing signal DW28 is applied to the AND gate, the frame sync flip-flop is set, signal DFS is generated, and the parallel sync acquisition function is inhibited. Timing signal DW2429 during words 24 through 29 prevents a further count from the three bit error counters after word 23. In turn, timing signal DW29- resets the error counter outputs to zero.

5-504. The presence of signal DFS indicates that the sync acquisition function is complete and the sync maintenance function is being performed. During sync maintenance, each of the three code comparators is active and continually performs a serial compare of the incoming data in bit 0 of words 1 through 23 with the equivalent bits in the appropriate DPSC, DNAC, and DNSC inputs to each code comparator. At this time, the three bit error counters are also enabled. During any given minor frame period, the incoming data contain any one of the three stuff command codes. Therefore, by the-time word 24 occurs, two of the bit error counters are saturated and indicate eight or more errors.

The bit error counter associated with the code comparator that is monitoring the active stuff command code being applied indicates between zero and seven errors when proper synchronization is present. When this condition is met, a low-level signal applied to OR gate U58 causes a high-level count up signal to the error count up/down binary counter during word 28. When all three bit counters contain counts of eight or more errors, all inputs to the OR gate are high and a low-level count down signal is applied to the binary counter.

5-505. The error up/down binary counter is initially enabled by signal DFS when frame sync acquisition is obtained. At this time, the counter output is preset to a count of five. During word 28, the applied count up or count down signal applied through the OR gate is clocked into the error up/down binary counter. The counter has a maximum count limit of five and can only count upwards in the count up mode when its output is between one and four. Therefore, the maximum number of successive count down signals required to initiate a loss of frame condition would be five. When the counter reaches a count of zero, the count 0 causes the loss of frame flip-flop to generate demultiplexer loss of frame signal DLOP when the next end of scan signal DEOS2- occurs. The count 0 also causes signal DFS from the frame sync flip-flop to go low and remove the inhibit to the parallel sync acquisition circuits so that another parallel sync acquisition search is performed.

5-506. During normal operation, the count eight outputs from the positive stuff and negative stuff error counters are used to identify the stuff command code contained in the overhead message being monitored. When one of the two bit error counters has an error count between zero and seven, the associated positive stuff or negative stuff command flip-flop output is set by word 28 signal DW28 to produce a high-level DNSE or DPSE signal. In turn, the bit error counter output that contains a count of eight sets the associated flip-flop to produce a low-level DPSE or DNSE signal. When both counters contain a count of eight, the outputs from the two flip-flop are low. A high-level DPSE signal is applied to the ERD and GC/DM cards when a positive stuff command is decoded or a high-level DNSE signal is applied when a negative stuff command is decoded. A no-action code is indicated when signals DPSE and DNSE are low.

5-507. The word reset flip-flop generates the demultiplexer word counter reset when signal DSYNC- is applied. The signal is applied to the GC/DM card as a synchronous timing signal that causes bit 0 of word 12 to be generated at the same time bit 0 of word 12 of the incoming data occurs.

5-508. Diagnostic Block Diagram Discussion (Figure 5-39). Two diagnostic error signals can be generated by the circuits on the FS card: frame sync diagnostic error signal FSD- and loss of frame sync diagnostic error signal LBS-. Signal FSD- can be initiated by the VLSR circuits during the frame acquisition period of operation or by the stuff command code compare circuits during the frame sync maintenance period of operation. In the frame synchronization period of operation, the word counter in the VLSR diagnostic circuits is incremented each time the A=B signal is generated from the address comparator in the VLSR circuits. The word counter is configured to generate a TC output every 10 counts. Ten counts are obtained by the TC output presetting the counter to six, which is the time it takes a pair of SD2 and SD3 data bits to be processed through the VLSR and returned to the diagnostic circuits. A TC condition is obtained after 10 counts so that the TC output signal clocks latches No. 1 and No. 9. When clocked, the latches contain the pair of SD2 and SD3 data bits applied to the input of the VLSR (R.A.M. No. 1).

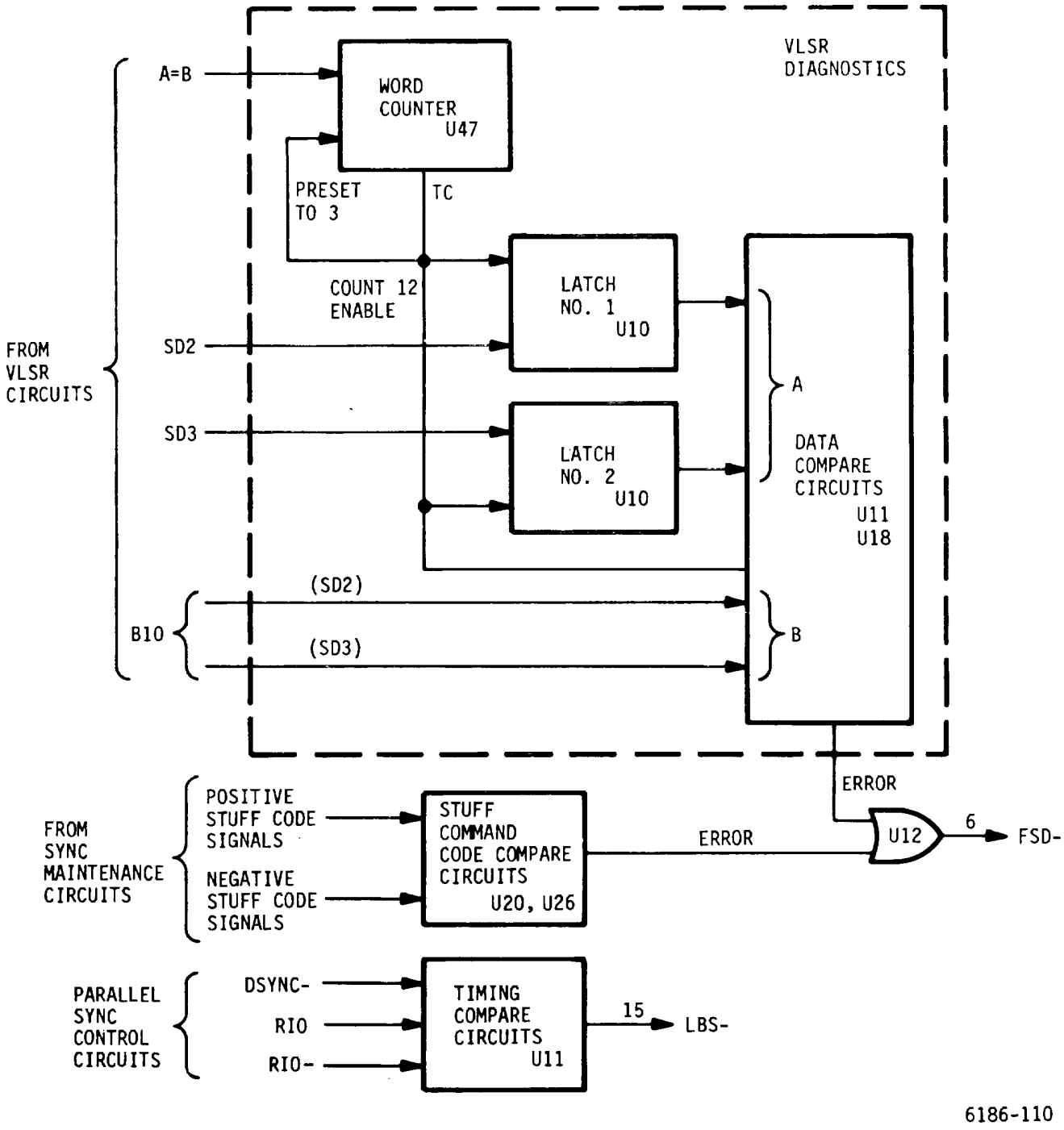


Figure 5-39. FS Card, Diagnostic Circuits - Block Diagram

When the next TC time occurs, the B10 set of SD2 and SD3 bits is applied back to the data compare circuits, where the two bits are compared with the two SD2 an SD3 bits in the two latch circuits. In a no-error condition, a compare condition is obtained.

In an error condition, the compare condition is not obtained and an error signal is applied through an OR gate to produce signal FSD- that is applied as an error input to the display card.

5-509. The stuff command code compare circuits effectively compare the positive stuff code and negative stuff code signals being generated in the sync maintenance circuits. An error condition exists when both stuff codes are detected within the circuits at the same time. During any one minor frame period being monitored, only one stuff command will be in the overhead message. When an error is detected, a diagnostic error signal is applied through an OR gate as signal FSD-.

5-510. The second diagnostic error signal, LBS-, is generated when demultiplexer frame sync signal DSYNC- is generated and the signal is not in synchronization with the parallel sync control circuits.

5-511. DETAILED CIRCUIT DISCUSSION.

5-512. The logic diagram associated with this detailed circuit discussion is contained in the circuit diagrams manual. The input data pulses (DATA+ and DATA-) are applied through switches S1 and S4 to data receiver U1, where the data pulses are conditioned to a TTL logic level compatible with the logic on the FS card. DATA switch S4 in the input circuit of U1 is set to the 75 or 6K (ohms) position as required by the circuit configuration. The function of DATA switch S1 is to change the phase relationship of the inputs to meet different system equipment configurations.

5-513. The input timing pulses (TM+ and TM-) associated with the input data are conditioned to a TTL logic level in timing receiver U2. The conditioned timing pulses from the circuit are applied through LOOPBACK switch S3 to clock data flip-flop U4. When switch S3 is in the NORM position, the incoming data and timing signals from U1 and U2 are applied to data flip-flop U4. When the switch is in the LOOP position, the data and timing signals from the multiplexer portion of the same multiplexer set are applied to the data flip-flop for test purposes. The data and timing from the multiplexer in the loopback configuration are usable only when the multiplexer and demultiplexer in a multiplexer set are configured the same; i.e., for duplex operation.

5-514. The incoming data are clocked through flip-flop U4-6 and the data channel output shift register formed by flip-flops U4-9, U5-5, and U5-9. The shift register function is inhibited when signal FS (DFS) applied to U5-10 is low. Signal FS is low when the demultiplexer frame synchronization is not established. The data output from the shift register is applied through four parallel inverters U3 to produce parallel output signals DTI1- through DTI4- that are the data inputs to the active channel cards in the demultiplexer. The data output from flip-flop U4-6 is also applied to data shift register U13, which produces signals SD2 and SD3 that are used in the frame synchronization function. U13 contains quad flip-flop circuits that are configured as a serial-in, parallel-out shift register. Signals SD2 and SD3 are sequential data bit outputs wherein SD2 is a data bit delayed one RIO time and SD3 is a data bit delayed two RIO times.

5-515. Signals SD2 and SD3 from U13 is applied as an input to R.A.M. No. 1 (U49) in the VLSR that is used in the parallel sync acquisition function, and as inputs to U10 in the diagnostic function. Signal SD3 is also applied as input Bll to the three command code comparators (U14-1), and as an input to data-in flip-flop U61 in the parallel and serial sync acquisition function. In the following discussions, processing of the incoming data in the parallel sync acquisition circuits is described, and then processing of data in the serial sync acquisition and sync maintenance circuits is described.

5-516. In the parallel maintenance function, each data bit in 10 consecutive data words is monitored for the presence of one of the three stuff command codes contained in the bit 0 positions of the first 10 words of the incoming message format. At the time that the VLSR is enabled, the circuits on the FS card do not know which words they are monitoring in the incoming message format. The first words monitored could be any bit sequence within any 10-word sequence. The VLSR, in effect, serially processes, at word level, 10 consecutive words while per- forming a parallel search of each bit location in each word. Each R.A.M. in the VLSR holds two sets of data bits that are the equivalent of two consecutive data words containing between 16 and 32 data bits. In one word time, each data bit in each of the two sets stored in each of the R.A.M.'s is scanned in parallel, one bit at a time. After the equivalent of one data word is scanned, the bits in each data word location (DO, D1, D2, D3) are shifted (B1 becomes B2, B8 becomes B9, etc) and the next parallel search is performed. This process continues until a compare is made as described in the following paragraphs.

5-517. The odd-bit shift register circuits in the VLSR are disabled when the LSB (DPUBO) of the applied 5-bit ports- in-use signals is a one, representing an odd number. The low signal out of inverter U36-4 holds odd-bit flip-flop U64-5 in a preset condition and the signal makes the LSB of the preset countered in 4-bit address counter U57 a zero. With flip-flop U64-5 held in a high state, half-rate flip-flop U56-5 increments the counter to generate a different address to the five R.A.M.'s (U49, U41, U33, U25, and U17) every other RIO time. When the counter output reaches a count that compares with the count pro- vided to address comparator U65 by signals DPUB1, DPUB2, DPUB3, and DPUB4, the ad-dress comparator generates an A=B signal that presets the output count of counter U57 to 0000. The A=B signal from comparator U65 determines the number of addresses applied to the R.A.M.'s. To service 32 bit locations in the R.A.M.'s, an A=B signal after a count of 16 is required; to service 20 bit locations, a count of 10 is required. Half-rate flip- flop U56-5 is toggled by RIO- to produce the half-rate clocks to counter U57 and the half-rate write enable signals to AND gate U55-11.

5-518. Each R.A.M. services two pairs of data inputs (SD3, SD2). Each data bit is temporarily stored in a memory location for one data word time (between 16 and 32 bit times). During each word time, a review of data bits equivalent to one word length is written into each set of R.A.M. memory locations. The result is data bits for one word being shifted serially to the adjacent R.A.M. memory locations. Each pair of parallel outputs (SD3, SD2) in each R.A.M. being serviced is applied as inputs to a 6-bit storage register (U40, U32, U24, or U9). The high enable signal from U56 to AND gate U55-11 is also applied as the latch signal to the four storage registers (U40, U32, U24, and U9). At this time, the four data bit outputs from the R.A.M.'s are latched into the registers. One-half RIO time later, a high RIO is applied to the second input of AND gate U55-11 and a low-level write enable is applied to each R.A.M. to initiate the next write function.

5-519. The data bits latched into the four storage registers (U40, U32, U24, and U9) are applied to the Al, A2 (SD3) and B1, B2 (SD2) inputs of data selectors U48, U31, U23, U16, and U8. The B select input to each data selector is held at a low level by the Q output from odd-bit address flip-flop U64-9. The A input of each data selector is alternately enabled at the system clock rate by Q output (half-rate clock-) from half-rate generator flip-flop U56-6.

This condition presents the SD3 and SD2 data bits as outputs B1 through B10 that are applied in parallel to the three stuff command code comparators. In a given word time, the number of sequential bits applied as a B output is equal to n+l between 16 and 32 bits.

5-520. When signal DPUBO is a zero, rep- resenting an even number of ports in use, the LSB preset input to 4-bit address counter U57 from inverter U36-4 is a count of one. Also, the preset signal applied to flip-flop U64-5 is effectively removed by the high-level signal from U36-4. This configuration enables the odd data bit functional circuits in the VLSR. In this configuration, the primary shift register continues to operate as described previously, but the initial write/read sequence is delayed one RIO time for the processing of the odd data bit as described in the following paragraph.

5-521. When a compare is made in ad- dress comparator U65, the A=B signal presets 4-bit address counter U57 to a count of one and also applies an enable signal to one input of AND gate U55-8. This occurs when signal RIO- is present. At the next RIO time, both inputs to AND gate U55-8 are high and flip-flop U64-5 output is low and its -6 output is high. This inhibits half-rate flip-flop U56-5 from generating a write en- able signal, during the next RIO- time, to the R.A.M.'s. In turn, the high U64-6 output allows the following RIO signal to set odd-bit address flip-flop U64-9 so that the next RIO- signal clocks the SD3- data into odd-bit shift register U39. At the same time, the data bits in shift registers U39, U15, and U7 are shifted one position, and the A input to each data selector is high to enable the 1C3 and 2C3 data paths in each of the five data selectors. The action enables the odd-bit data in the 10 words (B1 through B10) to be applied through the data selectors (U48, U31, U23, U16, and U8) to the three stuff command code comparators (U6, U14, U22, U30, U38, and U46).

5-522. The A and B select inputs (labeled A0 and A1 on logic) to the five data selectors are paralleled. The select input signal combinations to select the pairs of SD2, SD3, or odd-bit data are listed below. The data se-lectors are sampled at the RIO rate and are sequenced so that B1 through B10 provide a parallel set of data bits contained in 10 consecutive words. For example, assuming that B1 represents bit 3 in a given word, signals B1 through B10 represent the third data bit in 10 consecutive words being monitored. Time- wise, signal B10 represents the first word applied to the VLSR and is the first word being monitored; B1 is the last word applied to the VLSR in the 10-word sequence and is the 10th word of the group being monitored. Note that odd-numbered signals (B1, B3, B5, B7, and B9) are barred signals and even-numbered signals (B2, B4, etc) are unbarred. This condition is caused by inversion of the SD2 and SD3 signals in the R.A.M. outputs. In the loopback action involved, the even-numbered data bits are subject to double inversion to produce unbarred output signals.

Select Inputs A1	A0	Active Data Selector Input and Output
L	L	A1 & A2
L	H	B1 & B2
H	L	(not used)
H	H	C1 & C2

5-523. Since the operation of the three code comparator circuits is identical, only the operation of positive stuff code comparator U6, U14 is described.

The fixed 11-bit command code applied to the B inputs of each comparator is shown on the logic diagram in the circuit diagrams manual. The odd data bit numbers (1 through 9) programmed into the code comparator are the reverse of the bit numbers listed on the code diagram (0 is 1 and 1 is 0). This is to compensate for the barred odd-numbered signals applied to five of the A inputs to the code comparator. When a compare is made, the A=B signal from the code comparator is applied to one of the compare latches in U54. When a compare is made, one of the outputs from U54 is applied to OR gate U53 and to one input of parallel sync latch U62. In turn, the output from OR gate U53 is applied to sync enable flip-flop U56 and to one input of AND gate U55. When the next RIO- signal occurs, AND gate U55 latches U62 so that a signal is applied through OR gate U53 as the parallel sync (PS) signal. The parallel sync signal is routed through OR gate U52 to disable latch U54 by holding it in a reset state. The signal is also routed as an enable signal to one input of AND gate U60 in the serial sync acquisition circuits. When flip-flop U56 is clocked by the next RIO- signal, demultiplexer sync signal DSYNC- is generated for one bit time. At the time that latch U62 is latched, the appropriate NAC enable, PSC enable, or NSC enable signal is applied as an enable signal to one input of an AND gate (U60-8, U59-8, or U59-12) associated with the appropriate bit error counter in the serial sync acquisition circuits. The appropriate enable signal is selected by the signal applied through latch U54 from the comparator that generates the A=B signal.

5-524. Once signal DSYNC- is generated, the timing circuits in the demultiplexer are synchronized with the incoming data timing and the overhead stuff codes contained in bit 0 of the incoming data message should form a compare with the equivalent bits in one of the three stuff command codes generated on the GC/DM card and applied to the FS card. This is checked in the serial sync acquisition and sync maintenance circuits,

5-525. At the time that the parallel sync acquisition circuits generate signal DSYNC-, word reset flip-flop U61-9 generates demultiplexer reset signal DWPR- that is routed to the GC/DM card to preset the word counter. While signal DWPR- is being generated, the output from OR gate U51-4 generates a reset signal that resets the three bit error counters (U42, U43, and U44). When the circuits operate in the sync maintenance mode, the reset signal from OR gate U51- 4 is also generated when signals DEOS2- and DW29- are applied to AND gate U50-4 at the same time. Word 24 through 29 signal W2429 is applied through OR gate U36-6 to prevent the three bit error counters from further counts in the data word after word 23 in each minor frame period.

5-526. Data bits SD3 from U13-7 are clocked into data-in flip-flop U61-5 by end-of-scan signal DEOS2 and system clock RIO-. When the demultiplexer is in frame synchronization, the data bits (SD3) clocked through U61 are bit 0 of each applied data word. The serial SD3 data bits clocked through U61-5 are applied in parallel to one input on three exclusive OR gates U45. Each of the three exclusive OR gates receives one of the three serial sets of stuff command codes (DPSC, DNSC, and DNAC) from the GC/DM card. When the bits do not compare, the appropriate OR gate generates a high-level error signal (clock) during bit 0 to appropriate error bit counter U42, U43, or U44. The data check in the serial sync acquisition function starts with bit 0 of data word 12. The output from data-in flip-flop U61-6 is applied as demultiplexer overhead data signal DOD- to the GC/DM card during bit 0 of each data word.

5-527. Only one bit error counter (U42, U43, or U44) output is enabled during the serial sync acquisition function.

The bit counter output associated with the AND gate (U59-12, U59-8, or U60-8) that is enabled by the parallel sync signal from latch U62 is the active counter. At this time, the other two counters are counting the errors, but the two AND gates receiving the error counters are inhibited by low-level inputs from latch U62. Should the bit error counter (U42, U43, or U44) that is activated reach an error count of three, the AND gate (U59-12, U59-8, or U60-8) is enabled by the sync enable signal and the count one and count two inputs from the bit error counter. The low output from the enabled AND gate is applied through OR gate U60-12 to one input of AND gate U28. When demultiplexer end-of-scan signal DEOS2 occurs, the output from U28 sets flip-flop U26, which, in turn, clears latch U62. Latch U62 then forces the output of OR gate U53-8 to go high, which causes the out- put of OR gate U52-4 to go high, enabling latch U54. This action permits the parallel sync acquisition circuit to effectively start another parallel sync acquisition search during word 1 of the next minor frame.

5-528. When the serial search during words 12 through 23 is successful, the output from the enabled AND gate (U60-8, U59-8, or U59-12) remains high and the reset function described previously is inhibited. When word signal DW28 is generated, AND gate U60-6 in the input circuit of frame sync flip-flop U29 has high enable signals FS- from the Q out- put of U29 and a high enable parallel sync (PS) signal from OR gate U53. When word signal W28 occurs up/down counter U37 is preset to a count of five. At the same time, the high output through inverter U36-12 sets U29 to produce de- multiplexer frame sync signal DFS when U29 is clocked by signal DEOS2-. Signal DFS places an enable input to AND gates U34 and U59 in the inputs to error up/ down binary counter U37. Signal DFS also forces OR gate U52 to inhibit latch U54 by holding U54 in a clear state. Signal FS from flip-flop U29-7 disables AND gate U60 to prevent error up/down counter U37 from being reset in the frame sync maintenance function. Signal DFS- also holds flip-flop U26 in a clear state, which, in turn, causes U26 to apply a constant (clear) signal that disables latch U62. At this time, the FS card switches from the frame sync acquisition function to the frame sync maintenance function.

5-529. In the frame sync maintenance function, bit 0 in each word of the in- coming data (SD3) is monitored during words 1 through 23. During word 28, the outputs of the three bit error counters are monitored through OR gate U58-8. In this mode of operation, all three bit error counters are operational and the output from each one supplies an error count to a decode circuit consisting of two AND gates, one OR gate, and one inverter. Each decode circuit, in turn, supplies a low-level error signal to OR gate U58-8 when the counter contains an error count that is eight or higher. Seven or less errors detected during the check of bit 0 in words 1 through 23 is acceptable. Therefore, in proper operation, two of the decoder circuits apply low inputs (high error counts) to OR gate U58-8, and the third input from the decoder circuit associated with the error bit counter that is monitoring the appropriate stuff command codes is a high input (less than eight errors) to the OR gate.

5-530. In normal operation, the output from OR gate U58-8 is applied through inverter U35-2 to the input of AND gate U34-6 that is connected to the count up input of error up/down counter U37. The output from OR gate U58-4 is also applied to AND gate U59-6 that is connected to the count down input of U37. Therefore, when an error count of less than eight is monitored during words 1 through 23 of a given minor frame, a count up signal is applied to AND gate U34-6. In turn, more than seven errors cause a count down signal to be applied to AND gate U59-6.

Word signal W28 causes the appropriate AND gate to be enabled and the AND gate applies a count up or count down signal to U37 during word 28. The error up/down counter is initially set to a count of five, and as long as it contains a count of five, AND gate U28-8 inhibits AND gate U34-6 so that the maximum count in U37 is held to five. When U37 contains a count between one and four, a count up signal can be applied through AND gate U34-6 to make U37 count up. In turn, each count down signal applied through AND gate U59-6 decrements the count in U37 by one. When the count is decremented to a zero count and word signal W28 occurs, loss-of-frame flip-flop U29-9 is clocked by signal DEOS2- and demultiplexer loss of frame sync signal DLOF- is generated. At the same time, frame sync flip-flop U29-6 is also clocked and signal DFS goes low and inhibits AND gates U34-6 and U59-6 in the in- puts to U37. When signal DFS goes low, the output from OR gate U52-4 goes high and releases the inhibit condition (clear) to latch U54. The output from U29-7 goes high and removes the inhibit (clear) on flip-flop U26. These actions enable the parallel frame sync acquisition functions/circuits.

5-531. Positive stuff command flip-flop U27-6 or negative stuff command flip- flop U27-8 provides signal DNSE or DPSE to the ERD card and the GC/DM card to indicate that the minor frame being monitored contains a positive stuff, negative stuff, or no-action code. When both signals are low, the no-action command code is indicated. When a positive stuff code is successfully monitored (error count less than eight) the count eight (Q3) output from error bit counter U44 is low. This causes U27-8 to produce DPSE when signal DW28 occurs during word 28. In turn, a negative stuff code circuit produces signal DPSE when a negative stuff code is successively decoded and contains less than eight errors.

5-532. Diagnostic Circuits. Frame sync diagnostic signal FSD- is generated when an error signal is applied to OR gate U12-4 from the VLSR diagnostic circuits or when an error signal is applied to OR gate U12-4 from the stuff command code compare circuits. Word counter U47 in the VLSR diagnostic circuits is clocked by the half-rate clock- signal from flip-flop U56-6. The word counter is incremented one count when it is clocked and signal A=B is applied from comparator U65. Each time the word counter reaches a full count of 15, it generates a terminal count (TC) output that is applied to AND gate U53-12. The TC output also resets the counter to a count of six. The preset to a count of six causes the counter to produce a TC output after a count of 10. AND gate U53-12 is enabled during the write cycle of the VLSR. When a TC is generated, a clock signal is generated to flip-flops U10-6 and U10-8 that function as a latch circuit. At this time, the SD2 and SD3 data bits being applied to R.A.M. No. 1 in the VLSR are locked into the two latches. Therefore, when the two data bits (SD2 and SD3) are processed through the shift register and applied back to exclusive OR gates U18-3 and U18-11, a reverse compare should be present to place high inputs to OR gate U19. The reverse compare is a deliberate mismatch of the signals applied to the two exclusive OR gates. The data outputs from the two latches are inverted while the B10 data bits applied to the two exclusive OR gates are of the opposite polarity when the VLSR is in a no-error condition. Therefore, in an error condition, one of the exclusive OR gates has a compare that is applied through OR gate U19-6 to flip-flop Ull. The flip-flop, in turn, produces a high output to OR gate U12-4 to produce signal FSD-.

5-533. AND gates U28-3, U20-10, U20-4, U20-1, and U20-13 monitor the frame sync maintenance circuits and cause frame sync diagnostic error signal FSD- to be generated when the circuits are in an error condition.

In a no-error condition, signals PSE and NSE applied to AND gate U28-3 are never present (high) at the same time. In turn, the signals applied to the other AND gates are con- figured so that any one of the AND gates should never be enabled in a no-error condition. For example, any two of the ENA3, EPS3, and ENS3 signals should never be low at the same time.

5-534. Loss of frame sync diagnostic signal LBS- is generated when demultiplexer frame sync signal DSYNC- is generated out of sequence. In a no-error condition, AND gate U12-10 is not enabled when signal DSYNC- is generated. When AND gate U12-10 is enabled, loss of frame sync signal LBS- is generated from flip-flop Ull when the next RIO-signal is generated.

5-535. ERROR RATE DETECTOR AND REMOTE ALARM (ERD) CARD.

5-536. GENERAL. The ERD card is one of the common card types in the demultiplexer. Two functions are performed in the ERD card: a timing function that generates the minor frame count signals used in the demultiplexer timing functions, and an error rate detection function that lights the LINK ERROR RATE indicator when the occurrence rate of errors detected in the incoming serial data stream exceeds a predetermined threshold. The functional circuits on the ERD card are divided into the minor frame generation circuits shown in figure 5-40, the error rate detection circuits shown in figure FO-10, and the error reset and self-test circuits shown in figure 5-41. The logic diagram for the ERD card associated with the detailed circuit discussion is contained in the circuit diagrams manual.

5-537. BLOCK DIAGRAM DISCUSSION.

5-538. Minor Frame Generation Concept. The 5-bit minor frame count is in bit 0 of words 24 through 28 in the overhead message format. In some system applications, it is possible that, over a given period of time, a given number of data bits in the incoming message may be erroneous as a result of environmental and electrical transient interferences. Distorted or missing data bits could result in erroneous minor frame counts and could cause errors in the demultiplexer timing function. The minor frame numbers in the overhead messages are always applied in a predetermined order. Therefore, it is practical to identify a minor frame count in one overhead message and then synthetically generate error-free minor frame counts in the demultiplexer that are identical to the subsequent minor frame counts which should exist in the subsequent incoming messages. The minor frame generation circuits perform this function. The circuits scan the incoming message and establish synchronization to a 5-bit minor frame count during word 28. Once synchronization is established, the minor frame count generated on the ERD card is used in the demultiplexer circuits. A comparator circuit continually compares the minor frame count generated in the ERD card with the minor frame count in the overhead message. Through application of a confidence counter-comparator circuit, the circuits are programmed to detect a nominal amount of differences (no compares) without trying to resynchronize the minor frame count generated in the ERD card. It is probable that a nominal amount of no compares may be caused by transient problems rather than by a true loss of synchronization. When the number of no compares exceeds a predetermined figure, a resynchronization function is performed to synchronize the demultiplexer frame count to the frame count in the incoming message.

5-539. Minor Frame Generation Circuits (Figure 5-40). The incoming demultiplexer overhead data bits (DOD-) are continually applied to the overhead shift register, the minor frame comparator, and the counter control circuit.

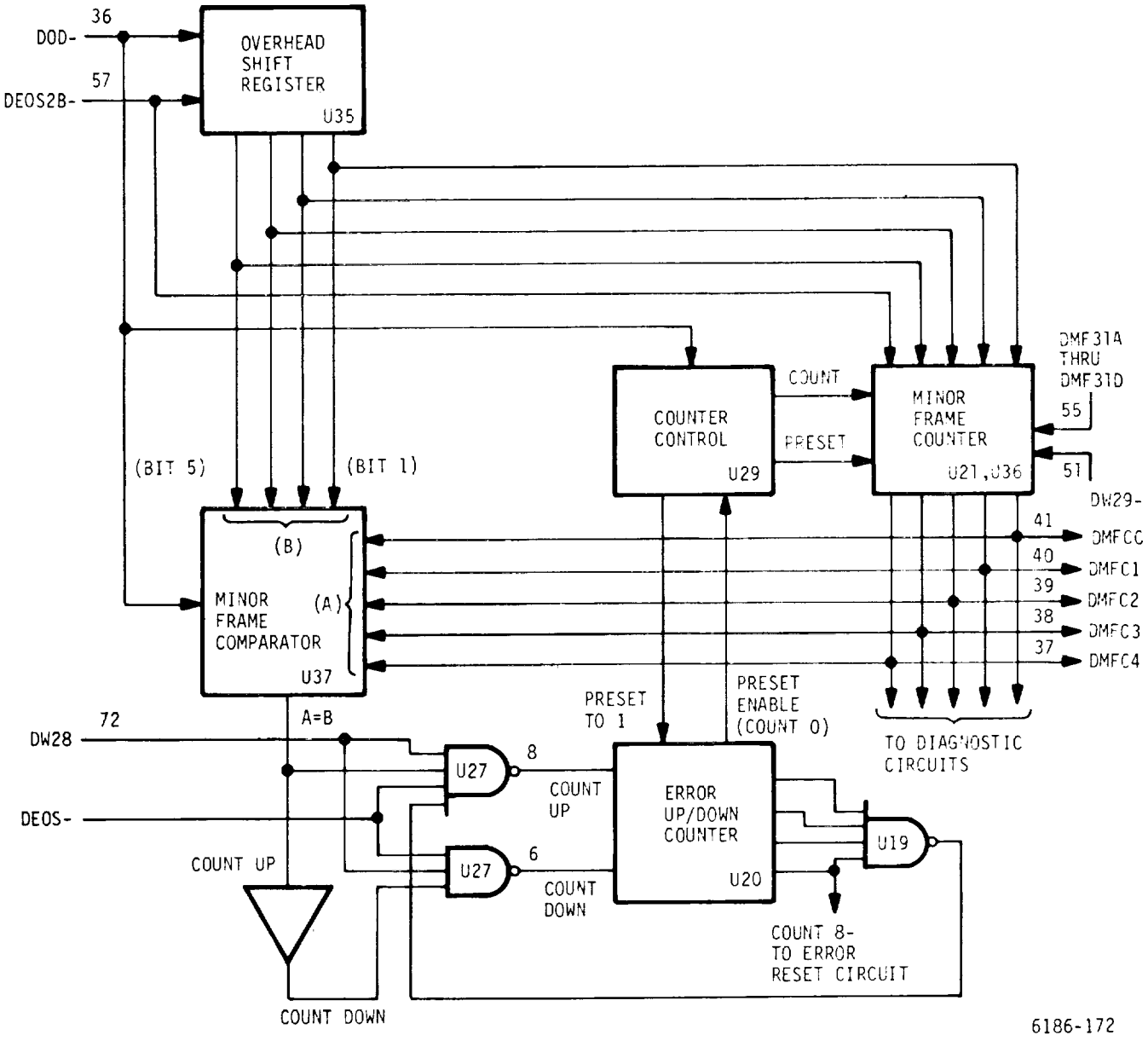


Figure 5-40. ERD Card, Minor Frame Generation Circuits - Block Diagram

In turn, the 4-bit output (bits L through 4) from the overhead shift register plus on-line signal DOD- (bit 5) are applied to the B inputs of the minor frame comparator. Bits 1 through 4 are also applied to the preset inputs of the minor frame counter. Bit 5 is applied to the counter through the counter control circuit. The 5-bit minor frame count output signals (DMFCO through DMFC4) from the minor frame counter are applied to the A inputs on the minor frame comparator. The minor frame comparator continually compares the two 5-bit inputs, and when they are identical, an A=B signal is generated and applied to enable AND gate U27-8 and inhibit AND gate U27-6 in the input of the error up/down counter.

The minor frame count in the overhead data bits is contained in words 24 through 28. There- fore, an A=B output can only be obtained during a compare in word 28. An output from the minor frame comparator can only be accepted by the AND gates in the input of the error up/down counter during the time that word 28 signal DW28 and end-of-scan signal DEOS2B- are applied to the AND gates. Therefore, when a compare is made during word 28, an A=B (high) output becomes a count up input to the error up/down counter. When a no-compare exists during word 28, the absence of the A=B signal is a count down input to the counter. When the error up/down counter is decremented to produce a count zero, a preset enable signal is applied to the counter control. The counter control, in turn, presets the existing minor frame count (during word 28) in the overhead shift register into the minor frame counter to reestablish synchronization. The minor frame counter continues to generate sequential minor frame counts DMFCO through DMFC4 until another preset enable signal is generated by the error up/down counter.

5-540. When the equipment is initially energized, the minor frame count in the 5-bit overhead register does not match the minor frame count from the minor frame counter. Therefore, each output from the minor frame comparator during word 28 decrements the error up/down counter until a preset enable signal (count zero) is generated and applied to the counter control circuit, which, in turn, causes the minor frame count from the overhead register to be pre- set into the minor frame counter. Therefore, the two minor frame counts applied to the minor frame comparator at the next compare time should be the same. In the synchronous condition, the error up/down counter is incremented until it contains a maximum count of 15. When a count of 15 is reached, AND gate U19 inhibits a further count up condition. In normal operation, the error up/down counter should maintain a count greater than eight. When the count decreases to a count of seven, the count 8- signal is routed to the error reset circuits, which, in turn, generate a demultiplexer error reset signal. When the counter output reaches zero, the resynchronization of the minor frame counter is performed.

5-541. Error Rate Detector (ERD) Circuits (Figure FO-10). The ERD circuits monitor the rate at which data bit errors occur in the incoming high-speed serial data stream. When the detected error rate exceeds a predetermined threshold, the ERD circuits cause the front panel LINK ERROR RATE indicator to light. Detection of data bit errors requires a knowledge of what sense (1 or 0) the data bits should be, as well as what sense the data bits actually are. Of all the data bits entering the demultiplexer, only the correct sense of selected overhead bits in the three stuffing codes is known. Therefore, error rate measurement is accomplished by using a statistical sampling approach in which the rate of errors occurring in the overhead data bits is considered to be representative (within statistical limits) of the error rate occurring among all data bits received. More specifically, errors detected in overhead data bits 1 through 23 by the FS card are used by the ERD card for error rate measurement purposes. Three sets of error counts from the FS card are applied during word 28 to the three error count (1, 2, and 4) selectors on the ERD card. At the same time, the decoded stuff command code (positive, negative, or no action), represented by the presence or absence of signals DNSE and DPSE, selects one set of error counts to be applied through the three error count selectors to the overhead error counter. When signal DPSE is applied error count signals DEPSO, DEPS1, and DEPS2 are applied to the preset inputs of the overhead error counter.

Signal DNSE causes error count signals DENSO, DENS1, and DENS2 to be applied to the counter. The absence of both signals DPSE and DNSE during word 28 causes signals DENAO, DENA1, and DENA2 to be applied to the counter. Word 28 signal DW28 presets the selected error count (between zero and seven) into the over- head error counter. The outputs from the three selector circuits are inverted; therefore, in a no-error condition, three ones are applied to the overhead error counter. The count eight preset input to the counter is always high (connected to +5 volts).Therefore, a no-error condition presets a count of 15 into the counter and causes the terminal count (TC) output to go high and present a count up input to the error up/down counter.

5-542. An error count of seven from the three selectors to the overhead error counter appears as three zeros so that the next preset count into the counter is a count of eight. As a result, seven count down pulses are produced while the next seven DEOS2B- signals increment the overhead error counter output to produced the TC out- put. Therefore, in all conditions, the overhead error counter produces one count down pulse for each error count applied to the three selectors for the given stuff command being monitored.

5-543. AND gate U16-8 in the count up input of the error up/down counter is enabled by count up signals from the divide-by-16 threshold counter and by the overhead error counter, signal DEOS2B-, and an enable signal from AND gate U16-6. When the error up/down counter contains a count of 15, AND gate U16-6 inhibits AND gate U16-8 to hold the maximum counter output to 15. AND gate U17 in the count down input of the error up/down counter is enabled by count down signals from the divide-by-16 threshold counter and by the overhead error counter, signal DEOS2B-, and an enable signal from AND gate U23. When the counter contains a count of zero, AND gate U23 inhibits AND gate U17 until a count of one or more is present in the counter. In normal operation, when a sufficient number of error bits is detected and the error up/down counter is decremented to a count of three or less, AND gate U24-10 generates a link error signal to the remote alarm circuits and to the front panel.

5-544. The error rate threshold circuits establish the bit error rate that can be tolerated in a given number of data bits before a link error condition is indicated by lighting the LINK ERROR RATE indicator on the front panel. Four error rate threshold switches on the ERD card provide for the selection of one of four threshold levels. The switches are marked $10^{-1,}$ $10^{-2,}$ $10^{-3,}$ and 10^{-4} and correspond to a threshold level of one error in 10 bits, one error in 100 bits, one error in 1000 bits, or one error in 10, 000 bits. In normal operation, the divide-by-16 threshold counter divides down the pulses from the selected threshold input. Each output pulse from the counter is a count up enable pulse that is applied to AND gate U16-8 in the count up input to the error up/down counter. When a pulse is not generated, the output from the counter is a count down enable signal to AND gate U17 in the count down input to the error up/down counter. When a count up enable is applied to AND gate U16-8 at the time that a TC count is present from the overhead error counter, a count up pulse increments the error up/down counter if the counter output is less than 15. In turn, a count up enable from the divide-by-16 threshold counter applied at the time that a TC count is not present from the overhead error counter will nullify one count down pulse by a low-level inhibit applied through inverter U3 to AND gate U17. Therefore, when the count from the error up/down counter is less than 15, each count up pulse from the divide-by-16 threshold counter causes one count up to be accomplished, or the count up pulse effectively nullifies one count down pulse from being applied to the counter.

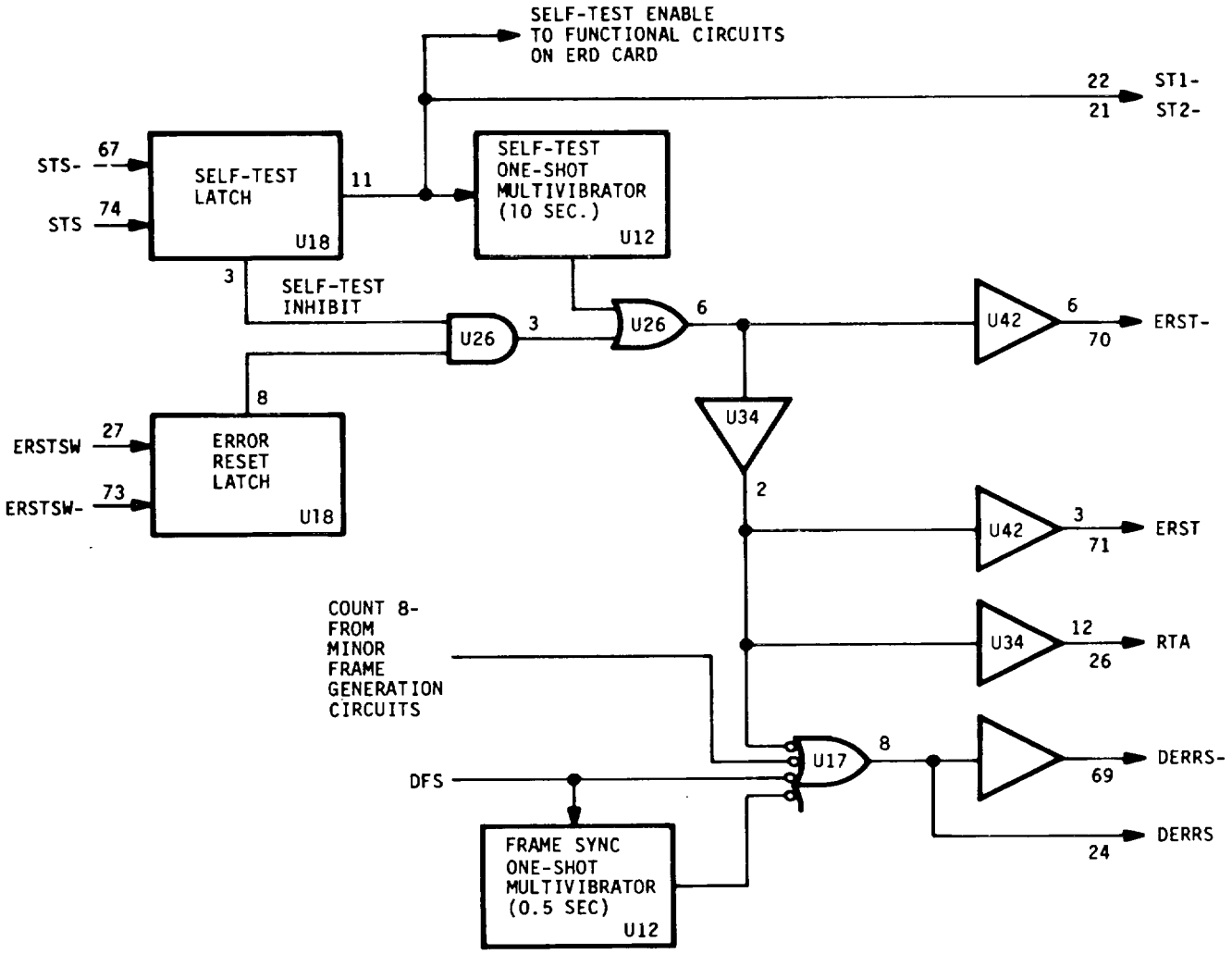
It should be noted that a count up enable from the divide-by-16 threshold counter occurs once for each 16, 160, 1600, or 16, 000 overhead data bits as determined by the setting of the error rate threshold switches. The 16-bit interval corresponds to a switch setting of 1 error per 10 bits; the 160-bit interval corresponds to a switch setting of 1 error per 100 bits, etc. Thus, for example, if the error rate threshold switches were set for 1 error in 10 bits and no errors were being detected, the error up/down counter would be incremented only once per 16 over- head data bits. The apparent difference between the 1-in-10 error rate threshold selected by the switches, and the 1-in-16 rate for incrementing the error up/ down counter is due to the statistical nature of the error rate measurement approach. Statistically, measuring zero errors in 16 bits provides approximately 80 percent confidence that the error rate among all received data bits is no worse than 1 in 10. Similarly, one bit of detected error during a 16-bit interval indicates an error rate of 1 in 10 at a confidence level of approximately 50 percent. Therefore, when a given error rate switch setting is selected, and the front panel LINK ERROR RATE indicator is out, the operator can be approximately 80 percent confident that the overall error rate of the incoming data stream is no worse than the threshold value selected.

5-545. Error Reset and Self-Test Circuits (Figure 5-41). The error reset function in the multiplexer set is initiated when the front panel DISPLAY RE-SET switch is pressed. At this time, error reset switch signal ERSTSW- is applied to the ERD card, which sets the error reset latch. If the front panel SELF TEST switch is set to the off (down) position, AND gate U26-3 is enabled and causes error reset signals ERST- and ERST, and reset temperature alarm signal RTA to be generated to re- set their associated diagnostic circuits to their off positions. Signals ERST- and ERST reset the diagnostic circuits on the multiplexer cards and signal RTA resets the temperature alarm circuit on the front panel. The reset signal through OR gate U17 develops error reset signals DERRS and DERRS- that reset the diagnostic circuits on the demultiplexer cards. The error reset latch is reset by signal ERSTSW- when the front panel DISPLAY RESET switch is released.

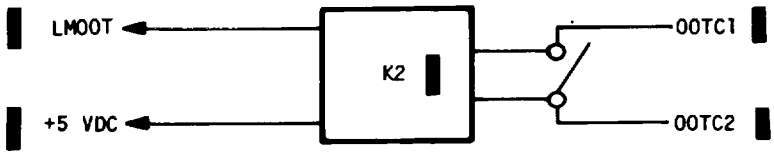
5-546. When the front panel SELF TEST switch is set to the on (up) position, self-test switch signal STS- is applied to the ERD card, setting the self-test latch. At this time, self-test signals ST1- and ST2- are produced to set the diagnostic circuits on all the cards in the multiplexer set to their self-test mode. When the SELF TEST switch is set to the off (down) position, self-test one-shot multivibrator U12 is triggered on for approximately 10 seconds to hold the logic circuits in a reset condition until the diagnostic circuits have time to resettle to the no-error state.

5-547. Loss of frame synchronization causes demultiplexer frame sync signal DFS to go low. This condition produces error reset signals DERRS and DBRRS- from OR gate U17. At the same time that signal DFS goes low, frame sync one-shot multivibrator U12 is triggered on for approximately 0.5 second. The resulting delay inhibits the diagnostic circuits while the demultiplexer attempts to reestablish frame synchronization.

5-548. Remote Alarm Circuits (Figure 5-41). Six remote alarm circuits on the ERD card provide operational status signals to the REMOTE ALARM connector on the rear panel. The six signals can be routed to a remote location for monitoring purposes. Five of the six signals are generated by energizing an associated remote alarm relay (K1 through K5) to provide a closed-loop condition when an error condition exists.



A. ERROR RESET AND SELF-TEST CIRCUITS



B. TYPICAL REMOTE ALARM CIRCUIT

6186-173A

Figure 5-41. ERD Card, Error Reset, Self-Test, and Remote Alarms Relay Circuits - Block Diagram

The sixth remote alarm relay (K6) is normally held open in an energized condition and provides a closed-loop condition when the power supply is shut down. The six remote alarm relays and their associated outputs are listed below with associated functional descriptions.

Relay No.	Signal Output	Cause
K1i	FAILC1/FAILC2	Card failure (FAIL) diagnostic signal from display card
K2	OOTC1/OOTC2	Out-of-tolerance (LMOOT) diagnostic signal from display card
K3	LERRC1/LERRC2	Link error rate signal for link error rate circuits on ERD card
K4	LOFBC1/LOFBC2	Demultiplexer loss-of-frame B (DLOF) signal from FS card (a latched condition)-
K5	LOFAC1/LOFAC2	Loss of frame A sync (DFS) signal from FS card
K6	PSFC1/PSFC2	Power supply fail (PSFR) error signal from power supply

5-549. Diagnostic Circuits. The minor frame generation circuits that produce the minor frame counts are duplicated by the diagnostic circuits shown in figure 5-42. The minor frame counts generated in the diagnostic circuits are applied to a diagnostic comparator that also has the functional minor frame counts being applied. When the circuits are in a no-error condition, the minor frame counts should compare and produce an A=B output from the comparator to the diagnostic flip-flop circuit. The A=B output from the diagnostic comparator occurs at the time that end-of-scan signal DEOS2B- is applied to the diagnostic flip-flop. Therefore, each A=B condition causes a high (no error) signal from the flip-flop. When an error is present and the A=B signal is not generated, a low is applied to the K input of the flip-flop, causing loss of minor frame error signal LOMFC- to be generated.

5-550. DETAILED CIRCUIT DISCUSSION.

5-551. Minor Frame Generation Circuits. Overhead data pulses DOD- are clocked into overhead shift register U35 by signal DEOS2B-. In turn, four parallel data bits from U35 are applied to the B inputs of minor frame comparator U37. The fifth bit input to pin 3 of U37 is on-line signal DOD- from inverter U44-6. When the equipment is initially turned on, minor frame counter U21, U36 produces a 5-bit minor frame count that is applied to the A inputs of U37. At this time, the two sets of minor frame counts applied to U37 do not compare. The output from U37 is an inhibit to AND gate U27-8 and an enable to AND gate U27-6. Therefore, a given series of signals DEOS2B- and word count DW28 cause the outputs from AND gate U27-6 to decrement up/down counter U20 until count zero is produced. Count zero is applied to preset flip-flop U21-6. When U21-6 is preset, U21-7 goes low and presets counter U36. At this time, during word 28, the minor frame count in U35 is preset into U36. This action synchronizes the minor frame count output from U36 to the minor frame count output from U35.

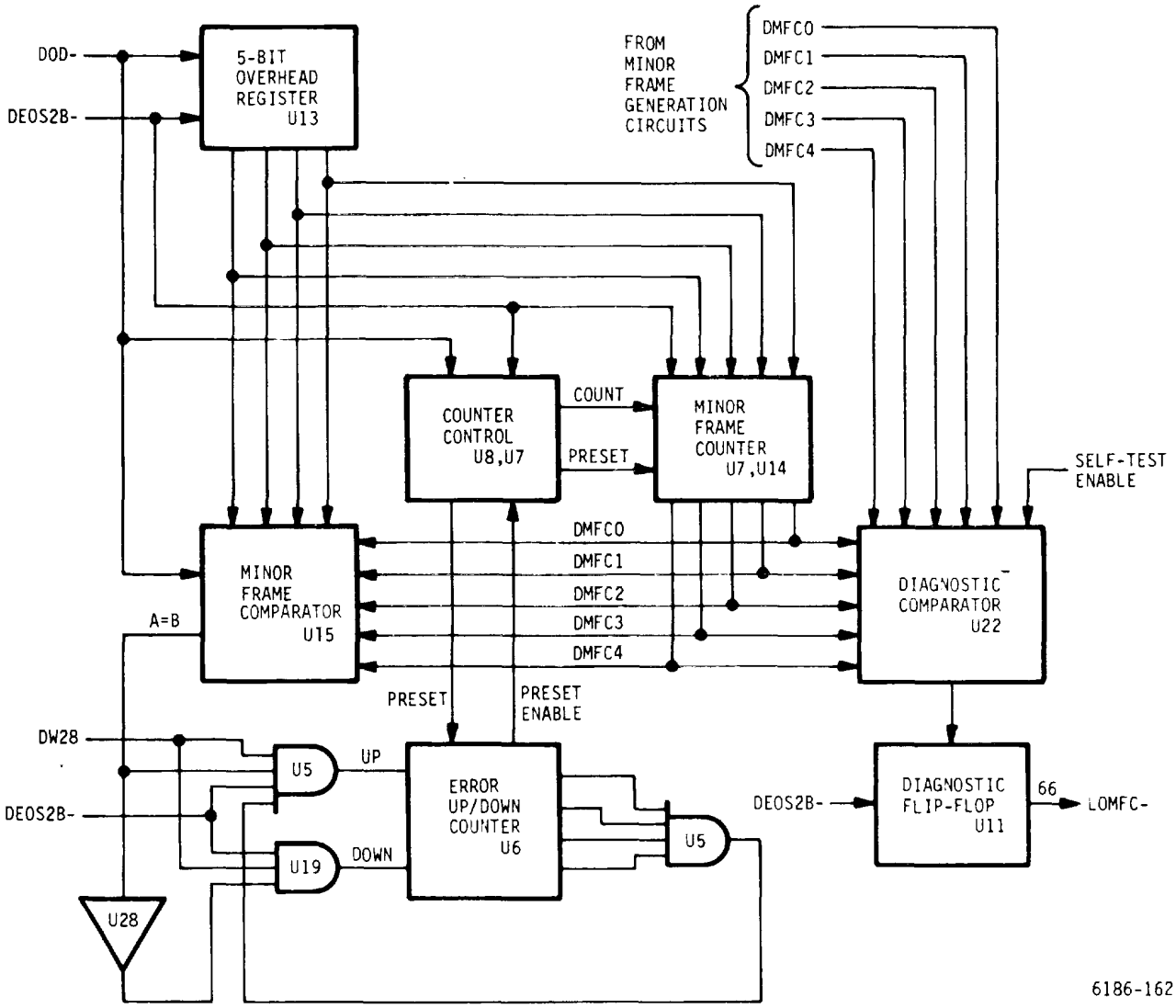


Figure 5-42. ERD Card, Minor Frame Generation Diagnostic Circuits - Block Diagram

U36 to the minor frame count output from U35. At this time, a count up (A=B) output is produced by U37.

5-552. A count up input enables AND gate U27-8 during word 28 when signal DEOS2B- is present and increments the count in U20. Up/down counter U20 can be incremented for a maximum count of 15. At count 15, AND gate U19-8 is enabled and produces an inhibit input to AND gate U27-8 as long as count 15 is in the counter. A random pattern of compares and no-compares in U37 causes the error up/down counter to count up and down as determined by the A=B output from U37. This function ensures that the 5-bit minor frame counts being generated from U36 are synchronous with the minor frame counts in the incoming overhead data. The error up/down counter permits random no-compares to occur between the two minor frame counts compared in U37 without interrupting the data flow. Most random no-compares are caused by transient problems associated with the incoming data pulses.

Assuming that the incoming minor frame count pattern is not deliberately changed, adequate count up sequences are developed between random no-compares to hold the count above zero in the error up/down counter so that consecutive minor frame counts can be properly generated from the minor frame counter.

5-553. Error Rate Detector (ERD) Circuits. The three divide-by-10 registers (U9, U2, and U1) are clocked by end-of-scan signal DEOS2B- during words 1 through 23. Each output from the three registers plus word 24 through word 29 signal DW2429- are applied to the input of one AND gate in threshold control logic U10. One error rate threshold switch is set to enable one of the four AND gates in U10. Enabling switch 10^{-1} effectively allows each DEOS2B- signal generated during words 1 through 23 to clock a count into divide-by-16 threshold counter U4. Switch 10^{-2} allows one out of 100 DEOS2B- signals to clock U4. Switch 10^{-3} allows one out of 1000 DEOS2B- signals to clock U4. Switch 10^{-4} allows one out of 10,000 DEOS2B- signals to clock U4. In turn, counter U4 clocks out one count up pulse for each 16 times it is clocked. Each time a terminal count of 15 is obtained, a count up enable pulse is applied from U4 to AND gate U16-8. At the same time, a count down inhibit pulse is applied through inverter U3-10 to AND gate U17-6. The time during which a TC count is not present, an inhibit count up signal is applied to AND gate U16-8 to prevent any count up from occurring, and the signal applied through inverter U3-10 is applied as a count down enable signal to AND gate U17-6.

5-554. The error counts produced on the FS card for the three stuff commands are applied to error count selectors U46 and U41 during word 28. Error count signals DEPSO, DEPS1, and DEPS3 are applied through the selectors to U33 when signal DPSE is applied to U46 and U41. When signal DNSE is applied to U46 and U41, signals DENS0, DENS1, and DENS3 are applied through the selectors to U33. When both signals are missing during word 28, signals DENAO, DENA1, and DENA3 are applied to U33. In a no-error condition, three ones are applied to the preset inputs of overhead error counter U33 during word 28. Since the MSB preset input to U33 is always high, a count of 15 is preset into U33. Therefore, the TC output of U33 goes high and applies a count up signal to AND gate U16-8 and a count down inhibit through inverter U32-10 to AND gate U17-6.

5-555. For each error count applied through the error count selectors to the preset input of overhead error counter U33, one count down pulse is effectively generated to AND gate U17-6 through inverter U32-10. Assuming an error count of four, a count of 11 is preset into counter U33 during word 28. (Input from U41 to U33 is low and all other inputs to U33 are high.) Therefore, four DEOS2B- signals are required to reach the TC count out of U33.

5-556. Each time AND gate U16-8 is enabled, the low output is applied as a count up pulse to counter U25. In turn, each time AND gate U17-6 is enabled, a count down pulse is applied to counter U25. AND gate U16-8 is enabled when a count up signal is applied from U4 and U33, the count in U25 is less than 15, and signal DEOS2B- is applied to the SB card. AND gate U17-6 is enabled when a count up signal is applied from U4 and U33, the count in U25 is not zero, and signal DEOS2B- is applied to the SB card. In an error environment, AND gate U24-10 produces a high error output when the count in U25 decreases to a count of three or less.

The high error output enables AND gate U23-8, causing link error rate signal LLER to be generated and light the LINK ERROR RATE indicator on the front panel. At the same time, remote alarm relay K3 energizes and initiates remote link error rate signals LERRC1 and LERRC2. The output from AND gate U24-10 applied to AND gate U23-3 is inhibited by the low-level ST1-signal applied to the second input to AND gate U23-3. AND gate U23-3 is used only in the diagnostic self-test function to test the ERD logic. When the count from U25'reaches zero, AND gates U24-10, U24-13, and U23-11 combine to produce an inhibit signal to AND gate U17-6. With AND gate U17-6 inhibited, no further count down occurs in U25.

5-557. Remote Alarm Circuits. The diagnostic circuits in the power supply generate power supply fail signals PSFR and -12 PSFR to energize remote alarm relay K6 when a power supply failure occurs. Energizing relay K6 generates a closed-loop condition through remote power supply fail signals PSFC1 and PSFC2. that are routed to the REMOTE ALARMS connector on the rear panel. The functional operation of each of the remote alarm relays K1 through K6 is basically the same. A card failure in the multiplexer set is applied as signal FAIL to relay K1. An out-of-tolerance condition in the multiplexer function is applied as out-of-tolerance signal LMOOT to relay K2. Relay K3 is energized when the count in the output of error up/down counter U25 decreases to a count of three. Relay K4 is energized by multiplexer loss-of-timing signal LOTRA- or by demultiplexer loss-of-timing signal DLOF. Relay K5 is energized by a loss of frame sync signal DFS.

5-558. Diagnostic Circuits. Shift register U13, counters U14 and U6, and comparator U15 form the diagnostic minor frame generation circuits that are identical to the functional minor frame generation circuits. The minor frame counts from both minor frame generation circuits are identical when the equipment is in a no-error condition. Therefore, diagnostic comparator U22 produces an A=B output that holds flip-flop Ull-6 output high. When an error condition exists, the minor frame counts applied to U22 do not compare and the A=B output is low. As a result, the output of Ull-6 goes low and generates loss-of- frame error signal LOMFC- the next time signal DEOS2B- occurs. In the self-test mode, flip-flop Ull-6 is held in the clear condition to generate signal LOMFC-.

5-559. When the SELF TEST switch on the front panel is set to the on(up) position, self-test signal ST1- goes low and sets latch U18-11, U18-3. The high signal from U18-11 enables one input of AND gate U23-3. At the same time, the low output from U18-3 clears U33, forcing error up/down counter U25 to count down and generate an error signal from AND gate U24-10 to AND gate U23-3. When AND gate U23-3 is enabled, rate detector diagnostic error signal DERD- is generated. At the same time, signals ST1- and ST2- are applied to all the cards in the multiplexer set to set all diagnostic circuits in the self-test mode. In the self-test mode remote alarm relays K1 through K6 are energized to produce error indications. When the SELF TEST switch is set to the off (down) position, signal STS is applied to reset latch U18-11, U18-3. The output from U18-3 goes high and enables AND gate U26-3 in the reset circuits. The low output from U26-3 causes error reset signals ERST-, ERST, DERRS, DERRS- and reset temperature alarm signal RTA to be generated and reset all the diagnostic circuits in the multiplexer set to their off state, assuming that the multiplexer set is in a no-error condition.

5-560. Power supply U48 produces a precision +5-volt output that is applied to the SB cards as a reference voltage for the APLL circuit.

SECTION V

DISPLAY CARD AND FRONT PANEL FUNCTIONAL OPERATION

5-561. INTRODUCTION.

5-562. Paragraphs 5-563 through 5-611 contain the block diagram discussion and the detailed circuit discussion for the display card. The block diagram discussion for the circuits mounted on the front panel is incorporated in the overall diagnostic block diagram discussion in section II, paragraphs 5-154 through 5-163. Paragraphs 5-612 through 5-614 contain the detailed circuit discussion for the circuits mounted on the front panel.

5-563. DISPLAY CARD.

5-564. GENERAL.

5-565. The display card contains logic circuits that monitor the diagnostic error signals from the diagnostic circuits on the common cards and channel (functional) cards in the multiplexer set. When an error condition is detected on the display card, the appropriate display signals are generated and applied to the front panel to activate the appropriate digital readout display and indicators as described in the following paragraphs.

5-566. As shown on figure 5-43, the function switch (MUX OFF/DEMUX OFF/ NORM) can be set to the MUX OFF position to inhibit the multiplexer diagnostics or to the DEMUX OFF position to inhibit the demultiplexer diagnostics. When both diagnostic functions are enabled, the switch is set to the NORM position.

5-567. In the following discussions, the diagnostic circuits on the display card that are active and monitor the diagnostic signals during normal operation are referred to as the primary diagnostic circuits. Diagnostic circuits on the display card that are only, active in the self-test mode of operation and test the primary diagnostic circuits are referred to as the secondary diagnostic circuits.

5-568. When a malfunction occurs in the multiplexer set, the faulty circuit may possibly force other circuits in the equipment to generate false error signals. The diagnostic circuits on the display card have an established order of priority for selecting the probable faulty source when more than one error condition is detected in the multiplexer set. The display card can monitor 21 error conditions, which are listed in their order of priority in table 5-6.

5-569. FUNCTIONAL BLOCK DIAGRAM DISCUSSION.

5-570. A diagnostic check of the active channel cards in the multiplexer is performed during word 24 by the multiplexer channel card error detector circuits. The status (error or no error) of each channel card is routed to the OEG card on the positive stuff re- quest line during word 24. At the OEG card, the signals are multiplexed into one data signal stream. The composite error signals are then applied as signal MPSA- to the multiplexer channel card error detector on the display card.

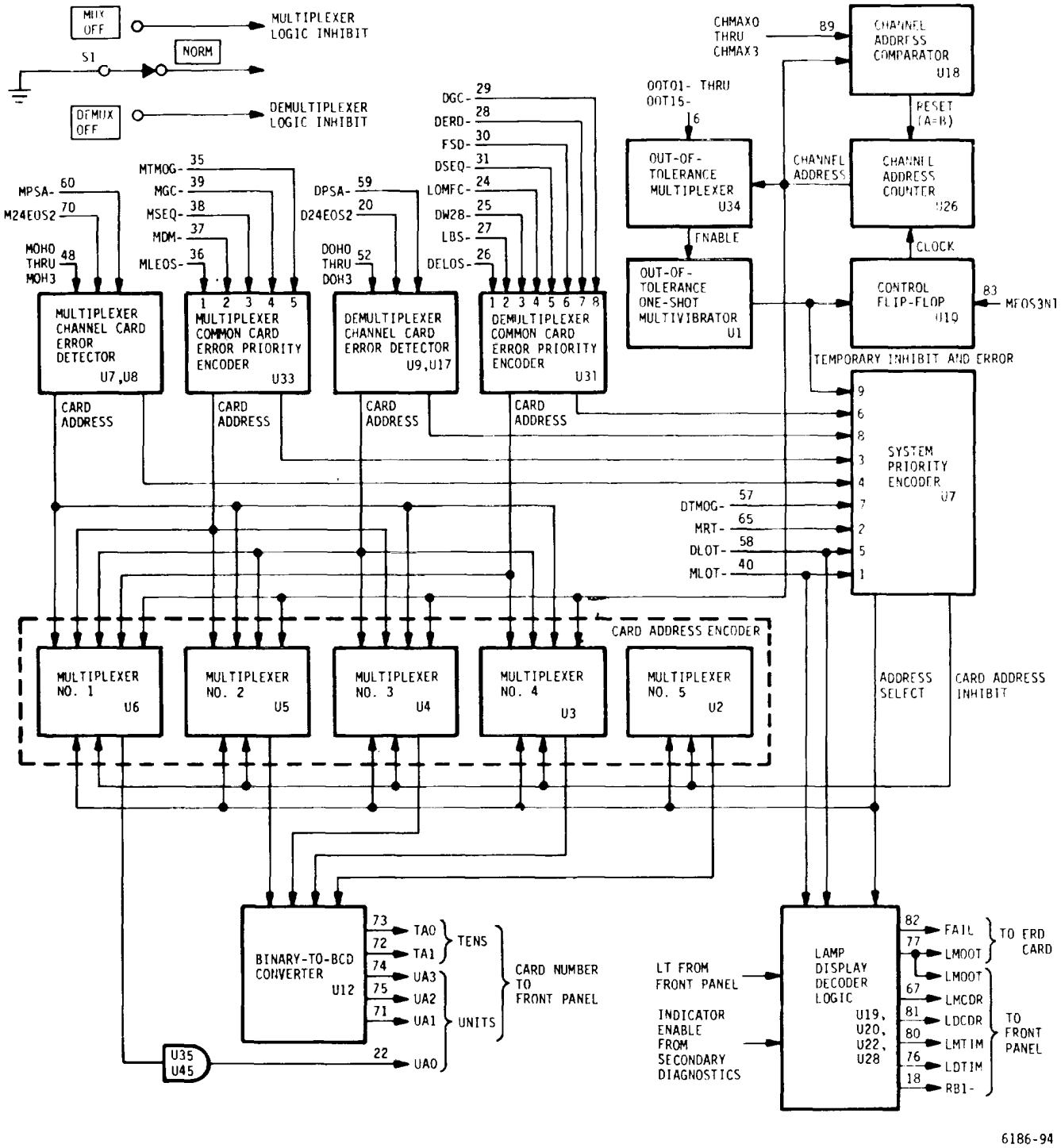


Figure 5-43. Display Card, Primary Diagnostics - Block Diagram

At the same time, the associated channel address for the channel being checked is multiplexed on the GC/DM card and is applied as overhead address count signals MOHO through MOH3 to the detector circuit. The detector circuit checks one channel status each time word 24 end-of-scan signal M24EOS2 is applied to the circuit. When a channel error is detected, an error signal is applied from the detector circuit to the system priority encoder for processing as de- scribed in paragraph 5-575.

Table 5-6.Diagnostic Display Priority

Order of Priority	Error Signal	Card Origin	Front Panel	
			Indicator	Numerical Display
1	MLOT-	RT	LOSS OF MUX TIMING	None
2	MRT-	RT	MULTIPLEXER CARD	16
3	MLEOS-	SEQ	MULTIPLEXER CARD	21
4	MDM-	GC/DM	MULTIPLEXER CARD	20
5	MSEQ-	SEQ	MULTIPLEXER CARD	21
6	MGC-	GC.DM	MULTIPLEXER CARD	20
7	MTMOG-	OEG	MULTIPLEXER CARD	19
8	MPSA-	RCB, VE, or TE/TR	MULTIPLEXER CARD	1 thru 15 (Note 1)
9	DLOT-	OEG	LOSS OF DEMUX TIMING	None
10	DLEOS-	SEQ	DEMULTIPLEXER CARD	21
11	LBS-	FSS	DEMULTIPLEXER CARD	16
12	DLW 28-	GC/DM	DEMULTIPLEXER CARD	20
13	LOMFC-	ERD	DEMULTIPLEXER CARD	17
14	DSEQ-	SEQ	DEMULTIPLEXER CARD	21
15	FSD-	FS	DEMULTIPLEXER CARD	16
16	DERD-	ERD	DEMULTIPLEXER CARD	17
17	DGC-	GC/DM	DEMULTIPLEXER CARD	20
18	DTMOG-	OEG	DEMULTIPLEXER CARD	19

Table 5-6. Diagnostic Display Priority (Cont)

Order of Priority	Error Signal	Card Origin	Front Panel	
			Indicator	Numerical Display
19	DPSA-	SB, TD, VD, or NBSB	DEMULTIPLEXER CARD	1 Thru 15 (Note 1)
20	OOTXX-	RCB	MULTIPLEXER CARD	16
21	(Note 2)	DISPLAY	MULTIPLEXER CARD	21
	Notes: **1. Error signal can be generated by any active channel in a configuration, using the RCB or TE/TR card in a multiplexer channel or the SB or TD card in a demultiplexer channel.** **2. Internal error signal developed by display card in self-test mode.**			

At the same time, each bit in the 4-bit channel address for the faulty channel is applied to one input on one of the multiplexers in the card address encoder.

5-571. The operation of the demultiplexer channel card error detector is basically the same as that described for the multiplexer channel card error detector in paragraph 5-570.

5-572. The multiplexer common card error priority encoder has a total of five card diagnostic error signals applied from the OEG, GC/DM, and seq cards. When two or more of the error signals are reported to the encoder, the error signal from the common card with the highest priority is processed. The priority encoder generates an error signal that is applied to the system priority encoder. The encoder also generates a card address for the selected card error that is applied to the inputs on the multiplexers in the card address encoder. The priority of the five signals monitored by the encoder are listed in order in the encoder blocks in figure 5-43.

5-573. The basic operation of the de- multiplexer common card error priority encoder is the same as that described in paragraph 5-572. The eight diagnostic error signals applied to the priority encoder are from the seq, FS, ERD, and GC/DM cards.

5-574. The out-of-tolerance multiplexer has an out-of-tolerance signal input from each active multiplexer RCB or TE/ TR channel card in the multiplexer set. When one of the out-of-tolerance signals (OOT01 through OOT15) is applied to the multiplexer, an enable signal is applied to the out-of-tolerance one-shot multivibrator. In turn, the multi- vibrator generates a temporary inhibit signal (approximately 1.5 seconds) to the control flip-flop to inhibit further clock signals from incrementing the channel address counter.

The temporary inhibit signal is also applied as an error signal to an input on the system priority encoder for processing. After the multivibrator's duty cycle expires, the channel address counter is permitted to continue counting. This circuit configuration permits the diagnostic function to detect and identify more than one channel out-of-tolerance condition over a given period of time. The maximum number of channel addresses that can be generated from the channel address counter is determined by the channel address comparator. The maximum number of active channels is applied to the channel address comparator through maximum channel number signals CHMAXO through CHMAX3 applied from the seq card. When the channel address output from the channel address counter is the same as the external channel address applied to the comparator, a reset (A=B) signal is generated from the comparator to the counter. The channel addresses from the counter are also applied to inputs on the card address multiplexers to identify the channel card location for a given out-of-tolerance condition. End-of-scan signal MEOS3N1 from the OEG card is applied to the control flip-flop to develop the clock signals that increment the channel address counter, one time during each word period.

5-575. The system priority encoder has nine inputs; each input has a priority status that is enforced when simultaneous error conditions are indicated at two or more inputs. An error signal to the priority encoder causes the encoder to produce a 3-bit address signal that is applied to the five card address multiplexers in the card address encoder and to the lamp display decoder logic. The assignments to the inputs on the priority encoder are shown on the block diagram (figure 5-43). An error signal (other than signal MLOT-) applied to the priority encoder causes the encoder to generate 3-bit address select signals to the card address multiplexers. This action selects the appropriate card address input on each of the card address multiplexers to produce the card address output that is applied to the binary-to-BCD converter. The 3-bit address select signals are also applied to the lamp display decoder logic to be decoded into the appropriate indicator enable signal associated with the card address being processed. When multiplexer loss-of-timing signal MLOT- is applied to the priority encoder, a card address inhibit signal is applied to the card address multiplexers so that a card address is not generated. The card address inhibit signal also causes the lamp display decoder logic circuits to decode signal LMTIM that is applied to the front panel to light the LOSS OF MUX TIMING indicator. No card address is generated for signal MLOT- because the signal indicates the absence of timing rather than a card malfunction. The same condition applies to demultiplexer loss-of-timing signal DLOT-, since no card address is associated with this error condition. All other error conditions applied to the system priority encoder have card addresses associated with error signals.

5-576. The card address outputs from the multiplexer and demultiplexer channel card error detectors and the card address outputs from the multiplexer and demultiplexer common card error priority encoders are applied to inputs on the card address multiplexers in the card address encoder. When a 3-bit address select signal from the system priority encoder is applied to each of the multiplexers, one channel address input (associated with the error condition reported) is enabled. The card address is then routed through the multiplexers in the card address encoder and is applied to the binary-to-BCD converter. The binary-to-BCD converter, in turn, converts the binary channel address into a BCD code that is applied to the digital readout circuits on the front panel.

The card address applied as tens address signals TA1 and TA0 and units address signals UA0 through UA3 is a number between 1 and 21 that responds to card locations 1 through 21 in the MULTIPLEXER (upper) card row or in the DEMULTIPLEXER (lower) card row in the multiplexer set.

5-577. The lamp display decoder logic circuit generates an enable signal that lights the appropriate indicator on the front panel associated with a given error signal. When multiplexer loss-of- timing signal MLOT- is applied to the decoder logic, the circuit generates signal LMTIM to the front panel to light the LOSS OF MUX TIMING indicator. When demultiplexer loss-of-timing signal DLOT- is applied to the decoder logic, the circuit generates signal LDTIM that lights the LOSS OF DEMUX TIMING indicator. All other error indications are processed from the 3-bit address select signals applied from the system priority encoder to the decoder logic. The decoder logic produces signal LMCRD, LDCRD, or LMOOT that light the MULTIPLEXER CARD, DEMULTIPLEXER CARD, or MULTIPLEXER OUT OF TOL indicator. Each time a card failure is decoded (LMCRD or LDCRD), and failure signal FAIL is generated and routed to the ERD card for use as a remote alarm. Multiplexer out of tolerance signal LMOOT is also routed to the ERD card for use as a remote alarm. When the LAMP TEST switch on the front panel is pressed, lamp test signal LT is applied to the decoder logic, which causes all the front panel indicators to light. When the equipment is in the self-test mode, an indicator enable signal from the self-test diagnostic logic causes the decoder logic to light all the front panel indicators when all the diagnostic circuits are functioning properly. If a diagnostic circuit associated with a given front panel indicator is malfunctioning during the self-test function, the decoder logic causes the associated front panel indicator to go out.

5-578. SELF-TEST BLOCK DIAGRAM DISCUSSION.

5-579. All of the diagnostic circuits on the cards in the multiplexer set are set to their error state when the SELF TEST switch on the front panel is set to the on (up) position. This causes all the diagnostic error inputs to the display card that are normally in the no-error state to become low-level error signals during the self-test mode. Therefore, the primary diagnostic circuits on the display card now detect a faulty card diagnostic circuit by the absence of an error condition on a given input. Each diagnostic input to the display card in the self-test mode is processed in the same priority order as that listed in table 5-6.

5-580. When a diagnostic circuit malfunction on a card is determined, the FAULT LOCATION display on the front panel of the multiplexer set shows a number between 1 and 21 and the MULTIPLEXER CARD on DEMULTIPLEXER CARD indicator is out to identify the faulty card location. When the cards have no faulty diagnostic circuits, a self-test function is performed on the primary diagnostic circuits of the display card as described in paragraph 5-584.

5-581. After the self-test function determines that all the diagnostic circuits on the cards are in a no-error condition, the secondary self-test diagnostic circuits test the primary diagnostic circuits on the display card. When a diagnostic circuit on the display card is determined to be faulty during the self-test function, the FAULT LOCATION display on the front panel shows 22 and the MULTIPLEXER CARD indicator goes out. When the circuits on the display card are determined to be in a no-error condition, the FAULT LOCATION display on the front panel shows 00 and all indicators are lighted.

5-582. The MUX OFF/DEMUX OFF/NORM switch on the display card is set to the NORM position when the multiplexer and demultiplexer are used in the multiplexer set.

The switch is set to the MUX OFF position when the multiplexer is not used or to the DEMUX OFF position when the demultiplexer is not used in the multiplexer set. The switch allows the diagnostic circuits associated with the multiplexer or the de- multiplexer cards to be bypassed, preventing faulty error indications when either the multiplexer or the demultiplexer is not used.

5-583. The operation of the primary diagnostic circuits on the display card in the self-test mode is the same as that described in the functional block diagram discussion, with one exception. The input circuits are biased so that a low-level error signal input is processed through the circuits as a no- error input and, in turn, a high-level input signal is processed through the circuits as an error input.

5-584. The secondary diagnostic circuits that supplement the primary diagnostic circuits in the self-test mode are shown in figure 5-44. The basic concept of the self-test function of the primary diagnostic circuits on the display card is that all the error signal inputs to the multiplexer and de- multiplexer self-test and function circuits are in a no-error condition. Thus, high-level enable signals are applied to two of the inputs to AND gate U22. In turn, when the primary diagnostic circuits are in a no-error condition, the output from the card address self-test OR function circuit is a low-level inhibit signal to one input of AND gate U22. If there is a faulty circuit in the primary diagnostic circuits on the display card, the output from the OR circuit goes high and enables AND gate U22. AND gate U22, in turn, generates a low-level error signal that initiates an error display as described in the following paragraphs.

5-585. Self-test signal ST2 is an enable signal to AND gate U22 when the equipment is in the self-test mode. When the equipment is not in the self- test mode, signal ST2 goes low and inhibits AND gate U22. This action, in turn, inhibits the secondary diagnostic function on the display card. An error condition detected by either the multiplexer or the demultiplexer AND gate circuits in the self-test mode generates a low-level inhibit signal to AND gate U22. This condition inhibits a high-level output from the OR gate circuit from enabling U22 when an error condition in the primary diagnostic circuits is detected on the display card. This configuration gives the secondary diagnostic circuits the lowest priority status in the self-test mode.

5-586. A self-test delay enable circuit on the display card provides a fixed delay time before the, self-test circuits are activated, preventing an erroneous indication from being generated at the time the SELF TEST switch on the front panel is set to the on (up) position. The outputs from the two shift registers in the circuit are held in the preset condition when signal ST2 is low. When the self-test mode is energized, signal ST2 goes high and enables the. shift registers. At this time, a 0 in the count 2 and count 3 outputs inhibits AND gate U36 and the multiplexer and demultiplexer channel card error detector-circuits in the primary diagnostic circuits. Since the functional operation of the multiplexer and demultiplexer shift registers is identical, only the multiplexer shift register is discussed in the following paragraph.

5-587. The first count is entered in the multiplexer shift register when word 24 end of scan signal M24EOS2 is applied as a clock pulse to the register during minor frame terminal count signal MMF31A-.

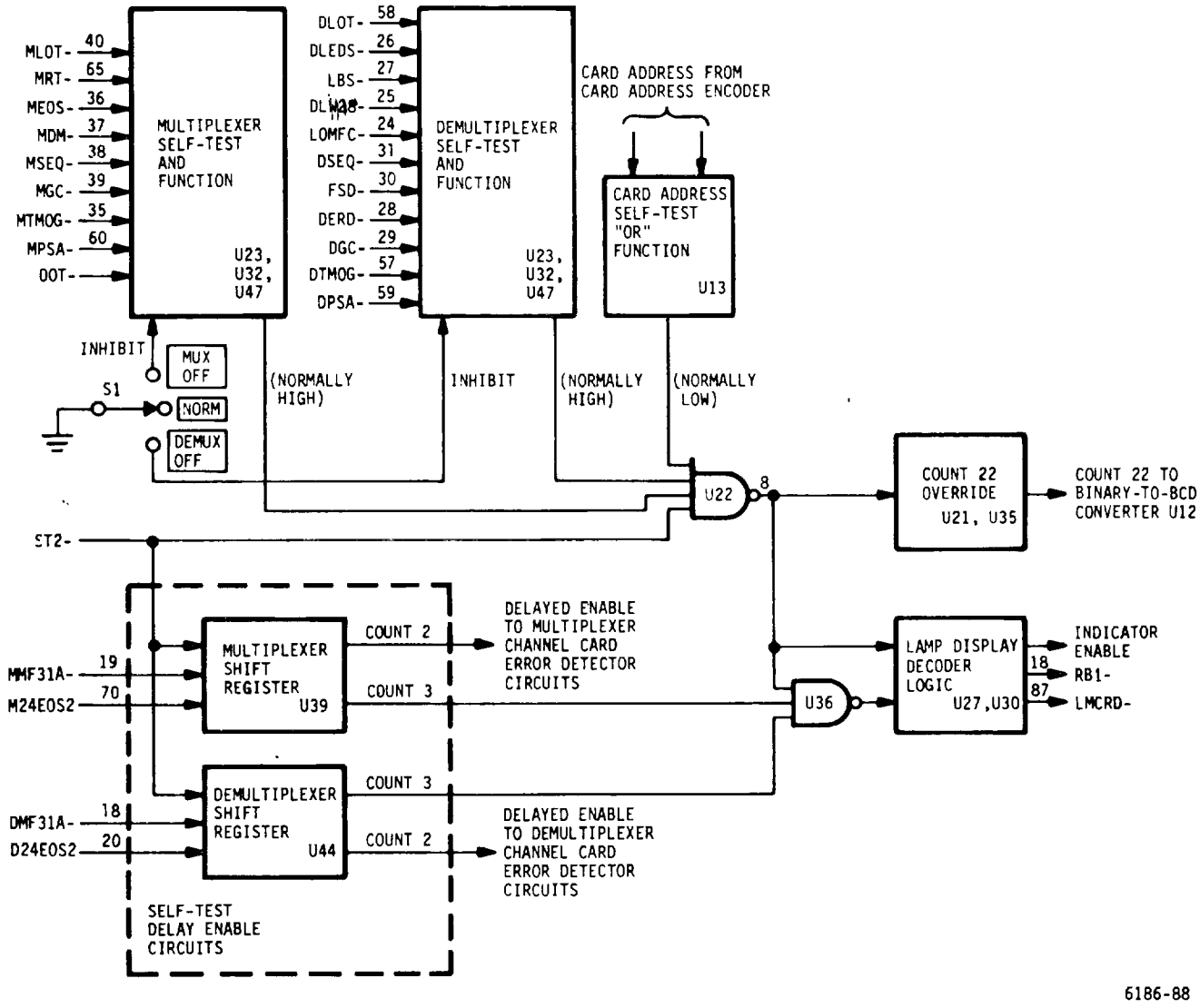


Figure 5-44. Display Card, Secondary Diagnostics - Block Diagram

At the end of the next word time (second clock), when signal M24EOS2 is produced, the shift register is clocked and count 2 becomes a 1. At this time, the multiplexer and demultiplexer channel card error detector cir- cuits are enabled. When the next (third clock) signal M24EOS2 occurs, the shift register is clocked again and count 3 becomes a 1. At this time, an enable is applied to one input of AND gate U36. Counts 2 and 3 from the shift registers remain high until completion of the self-test mode. When signal ST2 goes low, both shift registers are reset and counts 2 and 3 become 0 and AND gate U36 is inhibited. Logic circuits in the primary diagnostic circuits prevent the 0 from count 2 from inhibiting the multiplexer and demultiplexer channel card error detector circuits when the equipment is not in the self-test mode.

5-588. When the output from AND gate U22 is high (no-error condition), AND gate U36 is enabled. The low output from AND gate U36 is applied as an enable signal to the lamp display decoder logic that causes signal RBI- to be generated and applied to the front pan- el. In a no-error condition, signal RBI- causes the FAULT LOCATION display on the front panel to show 00. The lamp display logic decoder also generates an indicator enable signal to the front panel that causes all the indicators to light in a no-error condition.

5-589. When one or more of the applied error signals from the functional cards indicate a fault during the self-test mode, the self-test logic function that is performed is basically the same as described in the preceding paragraphs; with two exceptions. The primary diagnostic circuits cancel the 00 display function and the FAULT LOCATION display shows a defective card number between 1 and 21. Also, the appropriate MULTI-PLEXER CARD or DEMULTIPLEXER CARD indicator on the front panel goes out.

5-590. When all the functional cards are in a no-error condition and an error condition is detected in the diagnostic circuits on the display card, the output from the card address self-test OR function circuit goes high. Therefore, the output from AND gate U22 goes low. The low-level signal enables the count 22 override circuit so that the FAULT LO- CATION display on the front panel shows 22. Also, the low-level input to the lamp display decoder logic generates signal LMCRD that causes the MULTIPLEXER CARD indicator on the front panel to go out.

5-591. DETAILED FUNCTIONAL CIRCUIT DISCUSSION.

5-592. Each card diagnostic error signal applied to the display card, except the out-of-tolerance inputs, is applied to one input of an exclusive OR gate. The diagnostic error signals applied to the display card are high-level in- puts in the no-error condition and be- come low-level inputs in the error condition. Self-test signal ST2- is applied to the other inputs on the exclusive OR gates. In normal operation, signal ST2- applied to the display card is a high- level input. In the self-test mode of operation, signal ST2- becomes a low- level input. Each exclusive OR gate produces a low-level output signal when both inputs are the same: both inputs either high or low. The OR gate produces a high-level output signal when the two inputs are different: one high and the other low. In the following discussion, the circuits on the display card are described in their normal operating mode.

5-593. Multiplexer positive stuff acknowledge signal MPSA- from the OEG card conveys the diagnostic error status for one multiplexer channel card during word 24. In a no-error condition, signal MPSA- is high and becomes low in an error condition. Flip-flop U17-6 in the multiplexer channel card error detector circuit produces a clock pulse to counter U8 when low-level signal MPSA- and word 24 end-of-scan signal M24EPS2 from the OEG card are applied at the same time. At the time that counter U8 receives a clock pulse, the channel over-head address count signals (MOHO through MOH3) for the card being sampled is parallel loaded into U8. The overhead address loaded into U8 is applied to the 12 inputs of multiplexers U3 through U6 in the card address encoder circuit. The low output from U17-7 is applied as an error signal to system priority encoder U7. If there are no other error inputs with a higher priority being applied to encoder U7, the encoder produces the 010 address select signals that are applied to multiplexers U2 through U6.This address enables the T2 input of each multiplexer so that the dynamic and hard-wired card address at the 12 inputs of multiplexers U3 through U5 is applied to binary-to-BCD converter U12.

The output from multiplexer U6 is applied through AND gate U30-11 and inverter U45-8 to produce units address signal UA0 that is applied to the front panel. The other digits that form the card address applied to the front panel are units address signals UA1, UA2, and UA3, and tens address signals TA0 and TA1 from converter U12. The card ad- dress produced at this time represents the card location associated with the overhead address count (MOHO through MOH3) applied to counter U8. The binary coded decimal (BCD) outputs from the combination of inverter U45-8 and binary-to-BCD converter U12 are listed below. The number equivalent for each output is the number that is displayed on the front panel. Numbers not shown are created by the sum of the numbers listed below. For example, the number 9 requires signals UA0 and UA3. The number 19 requires signals UA0, UA3, and TA0.

Output Code	Number Shown on Front Panel	
UA0	1	
UA1	2	
UA0 + U A1	3	
UA2	4	Units
UA0 + UA2	5	
UA1 + UA2	6	
UA0 + UA1 + UA2	7	
UA3	8	
UA0 + UA3	9	
TA0	1	
TA1	2	Tens

5-594. One or more digits of the 010 3-bit select address signals from U7 are also applied to AND gates U32-6, U22-6, and U11-12, together with inverter U14-10 in the lamp display decoder logic circuits. In normal operation, the inputs to the four exclusive OR gates (U28) from inverter U27-8 are low and the outputs from inverter U27- 10 to five OR gates (U19, U11, and U20) are high. Therefore, the 3-bit address 010 from U7 inhibits AND gate U32-6 and enables AND gate U19-3. The low output from U19-3 is applied to OR gate U19-11, which, in turn, generates card fail signal FAIL that is applied to the Seq card to indicate a card failure for the remote alarms. A FAIL signal is not decoded for an OOTXX, DLOT-, or MLOT- signal. The output from AND gate U19-3 is also processed through OR gate U19-8 and exclusive OR gate U46-3 to generate multiplexer card error signal LMCRD, which lights the MULTIPLEXER CARD indicator on the front panel. The GS (pin 14) output from U7 is also applied to the decoder logic circuits as part of the decoder logic function. The output from U7-14 is low for each error signal applied to U7, except loss of timing signal MLOT-; for this one signal, the output from U7-14 is high. The GS output and the 3-bit address select signals from U7 to the decoder logic for each of the possible nine error input conditions are listed in table 5-7.

5-595. Demultiplexer positive stuff signal DPSA- is processed through flip- flop U17-10, and the associated channel overhead address count signals (DOHO through DOH3) are processed through counter U9 in the same basic sequence described previously for multiplexer signal MPSA- and the channel overhead address count signals (MOH0 through MOH3).

5-596. Multiplexer common card error priority encoder U33 monitors diagnostic error signals MLEOS-, MDM-, MSEQ-, MGC-, and MTMOG- from the multiplexer common cards. When a low-level error signal is applied through its associated exclusive OR gate, a low-level signal is applied to an input on U33. Outputs Y0 and Y2 from U33 contain the card address code associated with the specific error in- put. The Y0 and Y2 outputs are applied to the I_1 inputs of multiplexers U6, U5, and U4 in the card address encoder.

Table 5-7. Lamp Display Decoder Logic Outputs to Front Panel

Encoder U7						
	Output Pin					
Input Pin No.	9	7	6	14	Decode Output From Decoder Logic	Enabled Front Panel Indicator
5	1	1	1	1	LMTIM	LOSS OF MUX TIMING
4	0	0	0	0	LMCRD	MULTIPLEXER CARD
3	0	0	1	0	LMCRD	MULTIPLEXER CARD
2	0	1	0	0	LMCDR	MULTIPLEXER CARD
1	0	1	1	0	LDTIM	LOSS OF DEMUX TIMING
13	1	0	0	0	LDCRD	DEMULTIPLEXER CARD
12	1	0	1	0	LDCRD	DEMULTIPLEXER CARD
11	1	1	0	0	LDCRD	DEMULTIPLEXER CARD
10	1	1	1	0	LMOOT	MULTIPLEXER OUT OF TOL

The low-level GS output from U33 is the error input to system priority encoder U7.The error input to U7 is enabled if no error input having a higher priority status is applied to U7. The card address applied to the card address encoder is processed in the same manner as previously described.

5-597. Demultiplexer common card error priority encoder U31 processes error signals from the demultiplexer common cards in the same basic sequences de- scribed for multiplexer priority encoder U33. Encoder U31 uses three out- puts (Y0, Y1, and Y2) to provide output codes for the eight inputs applied to it. A logic decoder circuit in the out- put of U31 decodes any one of the eight error conditions to a card address of one of the four common cards being monitored.

5-598. In the out-of-tolerance error detection function, end of scan signal MEOS3N1 clocks flip-flop U10-9. Flip- flop U10-9, in turn, increments channel address counter U26. Counter U26 produces sequential channel addresses that select the inputs to address out-of-tolerance multiplexer U34. The channel address from U26 is also applied to channel address comparator U18. The maximum channel count from U26 is con- trolled by U18. When the channel ad- dress from U26 to U18 is the same as the channel address contained in maximum channel address signals CHMAX0 through CHMAX3 that are applied from the Seq card to U18, an A=B output from U18 re- sets the channel address counter. When out-of-tolerance signal OOTXX- is applied to a input on U34, a high is applied from U34 to AND gate U11-6. AND gate U11-6, in turn, applies a low trigger signal to enable one-shot multi- vibrator U1-9. The output from one-shot multivibrator U1-9 holds flip-flop U10 in a preset condition for approximately 1.5 seconds.

Each time U10 clocks U26, the low-level output from AND gate U19-6 inhibits AND gate U11-6 in the input circuit of one-shot multivibrator U1. The inhibit signal to U11 prevents U1 from being triggered on by a transition pulse at the time counter U26 is being clocked. When U1 is triggered on, the low-level output signal from U1 is also applied as an out-of-tolerance error signal to system priority encoder U7. An out-of-tolerance signal is processed through U7 and the card address encoder in the basic sequence as previously described.

5-599. Demultiplexer loss of timing signal DLOT- is applied through exclusive OR gate U38-8 and AND gate U16-11 to an input on system priority encoder U7. Demultiplexer OEG card diagnostic signal DTMOG- is applied through exclusive OR gate U42-11 and AND gate U16-8 to an input on U7.When either error signal is in an error state, the error signal is processed through U7 in the basic sequence previously described. Signal DLOT- is also applied, from AND gate U16-11, as loss-of-timing remote alarm signal DLOTRA- to the sequencer card to report a demultiplexer loss-of-timing condition.

5-600. Reference timer diagnostic signal MRT- is applied through exclusive OR gate U40-8 and AND gate U16-3 to an error input on system priority encoder U7. When the signal is in an error state, the error input is processed through U7 in the basic sequence previously described.

5-601. Multiplexer loss-of-timing signal MLOT- has the highest priority of all the error signals applied to system priority encoder U7. Signal MLOT- is applied through exclusive OR gate U42-8, AND gate U16-6, and inverter U15-4 to error input El on U7. In an error state, the high signal applied to E1 on U7 forces the GS output from U7 high. Signal MLOT- is the only error input to U7 that forces the GS output high. A high from the GS output is applied through inverters U15-12 and U15-2 to produce a high inhibit signal to multiplexers U2 through U6 in the card address encoder. This state produces all low inputs to binary-to-BCD converter U12 and inhibits a card address from being generated from U12 when a loss of timing occurs.

5-602. Lamp test signal LT is applied from the front panel to inverter U35-2 when the LAMP TEST switch on the front panel is pressed. This condition forces the decoder logic to generate the six enable signals to light all the indicators on the front panel.

5-603. Switch S1 on the display card is set to one of three positions. In the NORM position, the multiplexer and demultiplexer diagnostic circuits are enabled. In the MUX OFF position, only the demultiplexer diagnostic circuits are enabled. In the DEMUX OFF position, only the multiplexer diagnostic circuits are enabled. The diagnostic logic applications that enable or disable the diagnostic circuits are described in the following subparagraphs.

a. In the NORM position, the application of +5 volts enables the diagnostic circuits described in detail in subparagraphs b and c.

b. Setting switch S1 to the MUX OFF position applies an inhibit (ground) to AND gate U16-6 to inhibit the MLOT- input to the circuits. The inhibit from S1 also produces a high output from OR gate U36-12 that is applied to inverter U15-10.Inverter U15-10, in turn, produces a low inhibit signal to flip-flop U17-6 and a master reset (clear) to counter U8 in the multiplexer channel card error detector. The low inhibit signal from switch S1 is also applied through inverter U15-6 to inhibit multiplexer common card error priority encoder U33. The low inhibit input to AND gate U11-6 in the out-of-tolerance circuits disables the out-of-tolerance signals from out-of-tolerance multiplexer U34.

These inhibit conditions effectively disable all the multiplexer diagnostic error signals applied to the display card.

c. Setting switch S1 to the DEMUX OFF position applies an inhibit (ground) to AND gates U16-8 and U16-11 to inhibit the DLOT and DTMOG inputs to the display card. The inhibit produces a high output from OR gate U36-8 that is applied to inverter U15-8. Inverter U158, in turn, produces a low inhibit signal to flip-flop U17-10 and a master reset to counter U9 in the demultiplexer channel card error detector. The low inhibit signal from switch S1 is also applied through inverter U14-6 to inhibit demultiplexer common card error priority encoder U31. These inhibit conditions effectively disable all the demultiplexer diagnostic error signals applied to the display card.

5-604. DETAILED SELF-TEST CIRCUIT DISCUSSION.

5-605. Setting the SELF TEST switch on the front panel to the on (up) position applies self-test signal ST2- to the display card. This results in a change in the signal level applied to one input of each exclusive OR gate in series with each diagnostic error signal input to the card. In turn, the diagnostic error signals that are normally high in a no-error state are inverted to become low input signals in the no-error state during the self-test mode. Therefore, this switch to both inputs to each exclusive OR gate results in no change in the output from each OR gate, since both inputs to the OR gate retain the same relationship to each other. For example, in normal operation, exclusive OR gate U42-8 receives a high level loss-of-timing signal MLOT input and a high-level self-test signal ST2 input and the OR gates produces a low output. In the self-test mode, both input signals to the OR gate are low in a no-error condition and the OR gate output is still low. Therefore, the OR gate produces a low-level output in the operating mode and also in the self-test mode in a no-error state. Therefore, the operation of the functional circuits that process the signals applied through the OR gates is the same in the self-test mode as described previously. Also, in the self-test mode, all the out-of tolerance signals applied to the display card become high in a no-error condition.,

5-606 n the normal operating mode, multiplexer and demultiplexer shift registers U39 and U44 in the self-test delay enable circuit are held in a reset condition by the self-test low ST2- signal from inverter U45-4. Since the two shift registers are operationally alike, only the operation of U39 in the multiplexer function is discussed in paragraph 5-607.

5-607. Before a self-test function is initiated, the low Q1 output from shift register U39 is applied to exclusive OR gate U40-6. The output from U40-6, is a high-level input to OR gate U36-12. When the multiplexer diagnostic circuits are operational, all inputs to U36-12 are high to produce a low-level output. The low-level output is applied through inverter U15-10, producing a high-level signal to the clear input to flip-flop U17-6 and to the master reset on counter U8 in the multiplexer channel card error detector circuit. At the time that a self-test function is initiated, self-test signal ST2- goes low and results in a high input to one input of OR gate U40-6. In turn, the output from U40-6 goes low (output from Q1 on U39 to U40-6 is still low) and produces a high output from OR gate U36-12. The high-level signal applied from U36-12 through inverter U15-10 produces a low-level clear input to flip-flop U17-6 and a low-level master reset to counter U8.

Signal ST2- applied to OR gate U40-11 in the demultiplexer circuits results in an inhibit signal processed through OR gate U36-8 and inverter U15-8 to clear flip-flop U17-10 and master reset counter U9 in the demultiplexer channel card error detector circuit.

5-608. In the self-test mode, the initial low Q1 output from shift register U39 applied to exclusive OR gate U40-6 inhibits the multiplexer card diagnostic error function as described in paragraph 5-607. When self-test signal ST2is applied to the display card, the low-level inhibit signal to the master reset input is removed and counter U39 is enabled. At this time, the Q1 output from U39 is still low. The shift register is initially clocked when minor frame signal MMF31A is applied to a data input on U39 and word 24 end of scan signal M24EOS2 is applied to the clock input of U39. A high is clocked out of Q1 on U39 when the next (second) M24EOS2 signal is applied to the shift register. At this time, the output from exclusive OR gate U40-6 goes high and removes the clear signal from flip-flop U17-6 and the master reset from counter U8. A high is clocked out of Q2 on U39 when the next (third) M24EOS2 signal is applied to the shift register. The Q2 signal is applied through inverter U35-8 and OR gate U30-6 to enable one input of AND gate U36-6. At approximately the same time, the output from OR gate U30-8 in the demultiplexer function enables another input of U36-6.The third input to AND gate U36-6 from AND gate U22-8 should be high (no-error state) so that a low output signal from U36-6 is produced. The low signal from U36-6 to inverter U27-8 and OR gate U30-3 enables the operation of the lamp display decoder logic circuits for decoding error conditions detected in the self-test mode.

5-609. In the multiplexer secondary diagnostic check, the functional AND operation causes a low-level signal to be generated from AND gate U32-8 when all the multiplexer diagnostic error inputs to the display card are in a no-error state. At this time, the outputs from AND gates U47-6 and U47-8 are high inputs to AND gate U32-8. Also, the output from inverter U27-6 that monitors the out-of-tolerance circuits is a high input to AND gate U32-8. In turn, the low-level output from U32-8 is applied through OR gate U23-6 to place a high-level (no error) input to AND gate U22-8. The same basic sequence is performed by diagnostic AND gates U25-8, U46-6, U46-8, and U32-12 and OR gate U23-3 to place a high input to pin 12 on AND gate U22-8, representing a no-error condition of the demultiplexer circuits. The third input to pin 9 on AND gate U22-8 is signal ST2-, which is high in the self-test mode. The remaining input to pin 13 on AND gate U22-8 is applied from OR gate U13-8. When a no-error state exists in the secondary diagnostic circuits, the output from OR gate U13-8 is a low inhibit signal to AND gate U22-8, which then produces a high output. The operation of OR gate U13-8 is described in paragraph 5-610. When an error is detected in the secondary diagnostic circuits, the output from OR gate U13-8 goes high and enables AND gate U22-8. The low inhibit signal from U22 is applied to one input of AND gate U36-6 to force its output high. The high output from AND gate U36-6 is applied through OR gate U30-3 to place a high input on exclusive OR gate U46-3. Exclusive OR gate U46-3, in turn, produces multiplexer card error signal LMCRD that causes the MULTIPLEXER CARD indicator on the front panel to go out. The low output from U22-8 is also applied through inverter U35-12 to drive the outputs from inverters U21-4, U21-6, and U21-2 low. At the same time, the output from inverter U35-12 is also applied to the E input on binary-to-BCD converter U12 to drive all the outputs high. The result is a count 22 (UA1 and TA1 are high) to the digital display circuits on the front panel.

5-610. When all the diagnostic error inputs applied to the display card are in a no-error state, the outputs from multiplexers No. 2 through No. 6 in the card address encoder that are applied to OR gate U13-8 are high. In turn, the output from OR gate U13-8 to AND gate U22-8 at this time is a low inhibit signal. When the output from one of the multiplexers goes high as the result of a secondary diagnostic error, the output from OR gate U13-8 goes high and enables AND gate U22. The result is a count 22 and the MULTIPLEXER CARD indicator being lighted on the front panel.

5-611. Self-test signal ST2goes high when the SELF TEST switch on the front panel is set to the off (down) position. At the same time, error reset signals ERST and DERRS are applied from the ERD card to the display card. Signal ERST is applied through OR gate U36-12 and inverter U15-10 to clear flip-flop U17-6 and reset counter U18 in the multiplexer circuits. This function permits the diagnostic circuits on the multiplexer cards to reset before the normal diagnostic function is resumed. Signal DERRS performs the same operation on the demultiplexer diagnostic circuits (U17 and U9). Both reset signals are also applied to the display card when the DISPLAY RESET switch on the front panel is pressed.

5-612. FRONT PANEL DETAILED CIRCUIT DISCUSSION.

5-613. The following discussion is based on the front panel schematic diagram in the circuit diagrams manual. The FAULT LOCATION digital display consists of 7-segment optoelectronic display units U1 and U2. The displays are controlled by BCD-to-segment decoder/ driver units U3 and U4. In normal operation, the tens digital display (U1) is controlled by the outputs from driver U3, which, in turn, is controlled by tens address signals TA0 and TA1 from the display card. The units digital display (U2) is controlled by the outputs from driver U4, which, in turn, is controlled by units address signals UAO through UA3 from the display card. The combinations of digital displays that the signals develop are listed in paragraph 5-593. When LAMP TEST switch S3 is pressed, the output from inverter U8-12 goes low and enables the LT input on drivers U3 and U4. This condition produces a digital display of 88 from U1 and U2. Pressing the LAMP TEST switch also produces lamp test signal LT and causes a high level signal to be applied to inverters U8-2, U8-4, and U8-6 to energize relay K1 and light TEMPERATURE indicator DS11. When LAMP TEST switch S3 is released, signal LT is removed and all indicators return to their normal state. When the self-test mode of operation is initiated by setting SELF TEST switch S1 to the on (up) position, signal STS is applied to the ERD card to generate the self test signals to all cards. Ripple blanking input signal RBI- is generated on the display card and is applied to the RBI input of U3. This condition produces a digital display of 00 from U1 and U2, When SELF TEST switch S1 is on, a high input signal is applied to inverter U8-8 so that the output from U8-8 goes low and energizes latch temperature alarm relay K2. Relay K2, in turn, lights TEMPERATURE indicator DS11. Signal HOT- is applied to electro-optical isolator AT1 and to diode CR1 when the power supply overheats. Signal HOT- applied through diode CR1 energizes and latches relay K2 to light TEMPERATURE indicator DS11. In turn, AT1 is triggered into conduction to initiate signal IPSE that turns off the power supply when the TEMP SHUTDOWN jumper is installed on the front panel. Signal IPSE remains on until the POWER CONTROL ON/OFF switch S4 is set to OFF and then back to ON. When the TEMP SHUTDOWN jumper is not installed, an overtemperature condition does not shut down the power supply but the TEMPERATURE indicator lights. When the SELF TEST switch is set to the off position, or the lamp test switch is pressed and then released, reset temperature alarm signal RTA is applied through inverter U8-10 and unlatches relay K2 if it is in the latched state.

5-614. The lamp enable signals that light the other indicators on the front panel are described in paragraphs 5-146 through 5-153. No unusual or complicated circuits are involved with the individual indicators on the front panel.

SECTION VI

AC POWER DISTRIBUTION AND POWER SUPPLY ASSEMBLY FUNCTIONAL OPERATION

5-615. INTRODUCTION.

5-616. This section contains a block diagram discussion of the ac power distribution in the multiplexer set. This discussion, in paragraphs 5-618 and 5-619, also includes the input power circuit to the air cooling blower as part of the ac power distribution function. Paragraphs 5-620 through 5-645 contain the block diagram discussion and detailed circuit discussions for the power supply assembly (power supply).

5-617. AC POWER DISTRIBUTION.

5-618. The 115v ac power is applied through RFI filter A6 on the rear panel (figure 5-45) to circuit breaker CB1 on the front panel. When POWER CONTROL switch S4 is set to the ON position, the 115v ac is applied to the power supply and to EMI filters FL1, FL2. Interlock switch S1 is closed when the blower panel is mounted in place on the multiplexer set. When the blower panel is removed from the multiplexer set, S1 automatically opens and removes the input power. The EMI filters prevent any noise generated by the blower from reaching the logic circuits in the multiplexer set. Run capacitor C1 provides the phase shift to energize the Wye wound motor in the blower. Bleeder resistor R1 provides a discharge path for C1 when the blower panel is removed from the multiplexer set.

5-619. The power supply provides three regulated ($\pm$1.0 percent) dc voltages: +5 volts at 70 amperes full load, +12volts at 4 amperes full load, and -12volts at 4 amperes full load. When the POWER CONTROL switch on the front panel is set to the ON position, the power supply energizes and produces the three regulated dc voltages. The +5 volts lights POWER CONTROL indicator DS6 on the front panel. When anyone of the three dc voltages increases by more than 20 percent of the rated outputs, the power supply is automatically shut down and all indicators on the front panel are out except POWER SUPPLY ALARMS indicator DS10 on the front panel. When anyone of the three dc voltages decrease by more than 20 percent, the POWER SUPPLY ALARMS indicator on the front panel lights; the power supply does not shut down. When the temperature in the power supply exceeds 205°F (960C), thermostat switch S1 in the power supply closes to generate signal HOT- that energizes temperature alarm relay K2 on the front panel. When the relay is energized, the TEMPERATURE ALARMS indicator lights, the inhibit power supply signal IPSE is applied through the TEMP SHUTDOWN jumper to shut down the power supply, and overtemperature signals TEMPC1 and TEMPC2 provide a closed-loop condition to the REMOTE ALARM connector on the rear panel. Temperature alarm relay K2 is a latch relay that remains in the energized state until the POWER CONTROL switch is set to the OFF position and then back to the ON position. When the TEMP SHUTDOWN jumper is not installed, and an overtemperature condition exists, the power supply remains energized and the TEMPERATURE ALARMS indicator lights.

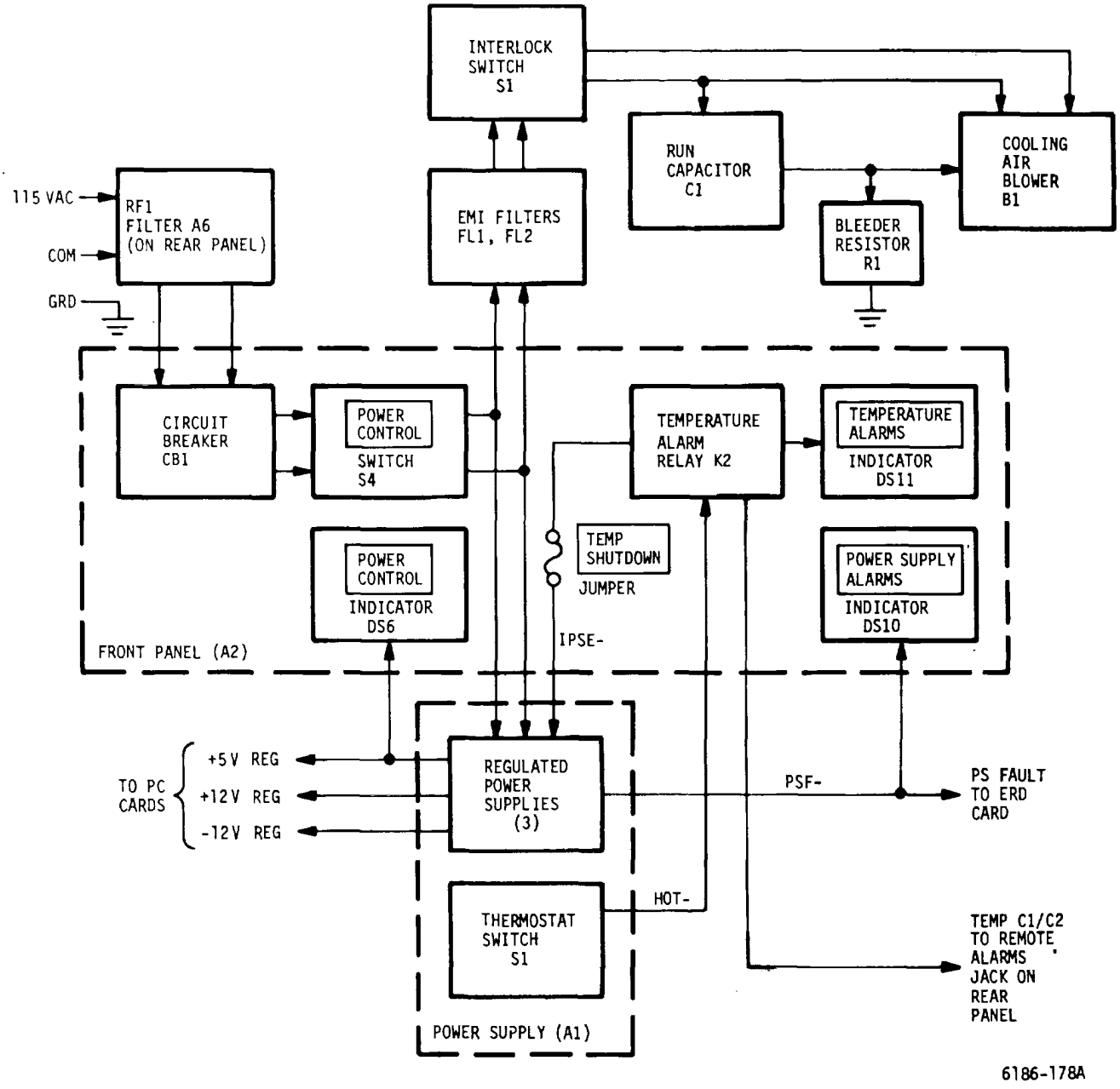


Figure 5-45. AC Power Distribution - Block Diagram

5-620. POWER SUPPLY.

5-621. GENERAL. In the power supply, electrical components are mounted directly on the power supply chassis, on the motherboard (A1), and on four plug-in cards. The four plug-in cards, ±12volt regulator card A1, +5-volt regulator card A2, ±12-volt driver card A3, and +5-volt driver card A4; all plug into the motherboard. The block diagrams associated with the block diagram discussion are shown in figures FO-11, 5-46, and 5-47. The following schematic diagrams in the circuit diagrams manuals are used in the detailed circuit discussions: power supply, ±12-volt regulator card, +5-volt regulator card, ±12-volt driver card, and the +5-volt driver card.

5-622. BLOCK DIAGRAM DISCUSSION.

5-623. The 115 vac input is applied to step-down transformer T6 and to the +150-volt power supply (figure FO-11). The +150-volt unregulated output from the +150-volt power supply is the source voltage for the five sets of switches in the outputs of the regulated power supplies. Step-down transformer T6 produces a 18.5-vdc output that is applied to the +12-volt and -12-volt power supplies. In turn, the two power supplies generate the +12V (c) and -12V (c) voltages that power the control and voltage regulator circuits.

5-624. The constant current generator provides a constant current source of 7.5 ma to the reference voltage generator. The reference voltage generator, in turn, produces a constant +4.77V reference (Ref) voltage that is applied to the clock generator, ±12-volt regulator circuit, +5-volt regulator circuits (4), and the +5 and ±12-volt over/under voltage detectors.

5-625. The 4.77 Ref and +12V (c) voltages are applied to the low-voltage detector circuit. The low-voltage detector circuit provides low-voltage protection for the power supply by shutting down the power supply when the ac source voltage decreases to 80 vac or less. When the incoming voltage decreases to 80 vac or less, an inhibit signal is generated to inhibit the +5volt power supply. Turning off the +5-volt power supply completely shuts down the power supply. When the input ac voltage increases to 100 vac or more, the inhibit signal is removed and the power supply becomes functional again. The +5-volt power supply generates the +5V (c) power required to operate the voltage regulator and clock generator circuits.

5-626. The +5-volt and ±12-volt over/under voltage detectors (figure 5-46) monitor the +5V Reg, +12V Reg, and -12V Reg outputs from the power supply and automatically shuts down the power supply when an over-voltage condition occurs. When an over-voltage condition occurs, the appropriate detector circuit produces a signal through CR2, CR4, or CR6 that causes the clock error control circuit to generate an inhibit signal to the clock generator. At the same time, a signal is also applied through CR1, CR3, or CR5 that causes the alarm generator circuit to generate a signal that, in turn, causes a drivers circuit to produce the local alarm and remote alarm signals. The local alarm signal lights the POWER SUPPLY ALARMS indicator on the front panel. The remote alarm signal is applied to the ERD card to initiate a power supply failure remote alarm signal. The clock generator circuit contains a 18-kHz oscillator that produces 18-kHz pulses through switch Q4 and two inverters to the B clock and A clock flip-flops. The B clock flip-flop produces 9-kHz B clock pulses through an inverter to the five voltage regulator circuits. In turn, the A clock flip-flop produces similar A-clock pulses to the five voltage regulator circuits. The A clock and B clock pulses are shut down when an inhibit signal from the clock error control circuit is applied to switch Q4.

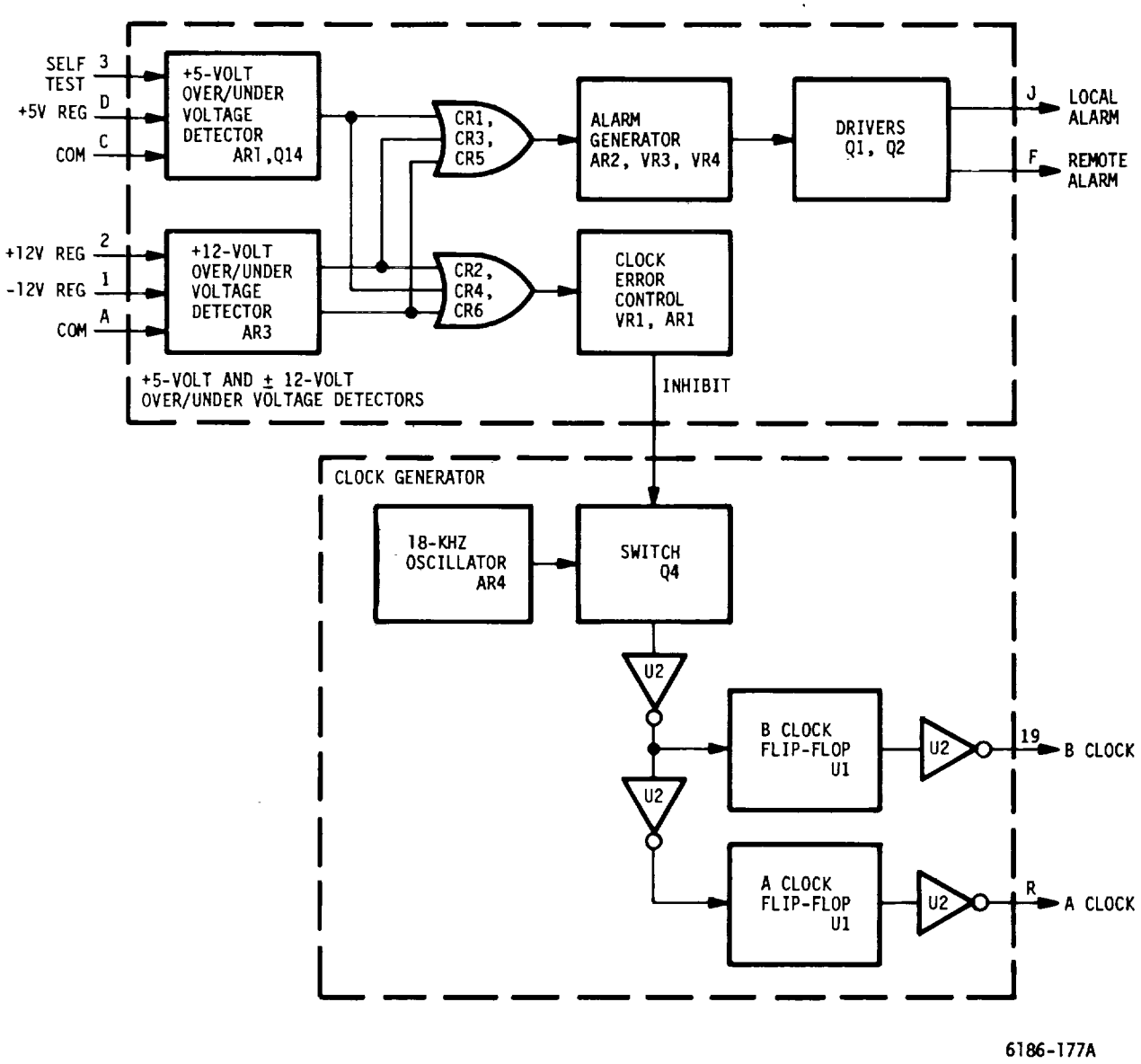


Figure 5-46. ±12-volt Regulator Card, Clock Generator and Over/Under Voltage Detector Circuits - Block Diagram

5-627. Basically, the four identical +5-volt regulator circuits are similar to the ±12-volt regulator circuit discussed in this paragraph. Therefore, the +5-volt regulator circuits are not discussed in detail in the block diagram discussion. The ±12-volt regulator circuit (figure 5-47) monitors the +12V Reg and -12V Reg outputs and generate control signals as necessary to regulate the two outputs within ±1.0 percent of +12 and -12 volts. The two voltages are applied to a voltage comparator. An increase in either voltage causes the output voltage from the voltage comparator to the error amplifier to increase. A decrease in either voltage causes the output voltage from the voltage comparator to the error amplifier to decrease. An increase in voltage to the error amplifier causes a higher (more positive) threshold voltage to be applied to the high-speed comparator.

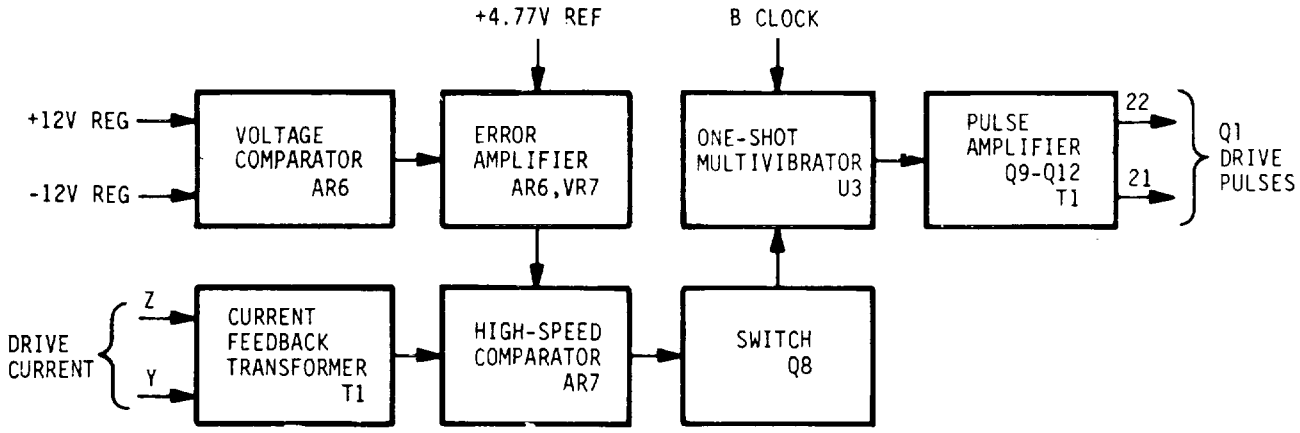


Figure 5-47. ±12-Volt Regulator Card, ±12-Volt Regulator Circuit - Block Diagram

A decrease in voltage to the error amplifier causes a less positive threshold voltage to be applied to the high-speed comparator. At the same time, drive current from the switch drivers is applied through the current feedback transformer as a dc ramp (sawtooth) voltage to a second input on the high-speed comparator. When the amplitude of the dc ramp voltage reaches the threshold level applied from the error amplifier a control pulse is generated to turn or. switch Q8. In turn, switch Q8 resets a one-shot multivibrator when it is turned on. The one-shot multivibrator is triggered on by the B clock signal from the clock generator. The time that the multivibrator is allowed to conduct determines the width of the drive pulses generated by the pulse amplifier. The conduction time of the multivibrator is determined when switch Q8 is turned on. Figure 5-48 shows that a narrow pulsewidth is used to decrease the output voltage level and a wider pulsewidth is required to increase the output voltage level. Normally, a decrease in the output voltage level indicates an increased current power requirement. Therefore, a wider pulsewidth is required to provide the increased energy requirements. In turn, a decrease in current requirements require a narrower pulsewidth to provide the less energy requirements. The pulse output from the one-shot multivibrator is amplified through the pulse amplifier as the Q1 drive pulses that are applied to the ±12-volt driver card.

5-628. The drive pulses from the ±12volt regulator circuit are applied through the ±12-volt driver card (A2) to drive the ±12-volt switches. Each time the switches are pulsed, energy is coupled through a transformer to the ±12-volt rectifier circuits that produce a dc input to the ±12-volt filter circuit. The outputs from the filter circuit are the +12V Reg and -12V Reg outputs that are applied to power the logic circuits in the multiplexer set.

5-629. The +5-volt regulator card contains four identical regulator circuits that are operated in parallel to generate the drive pulses for the four sets of switches.

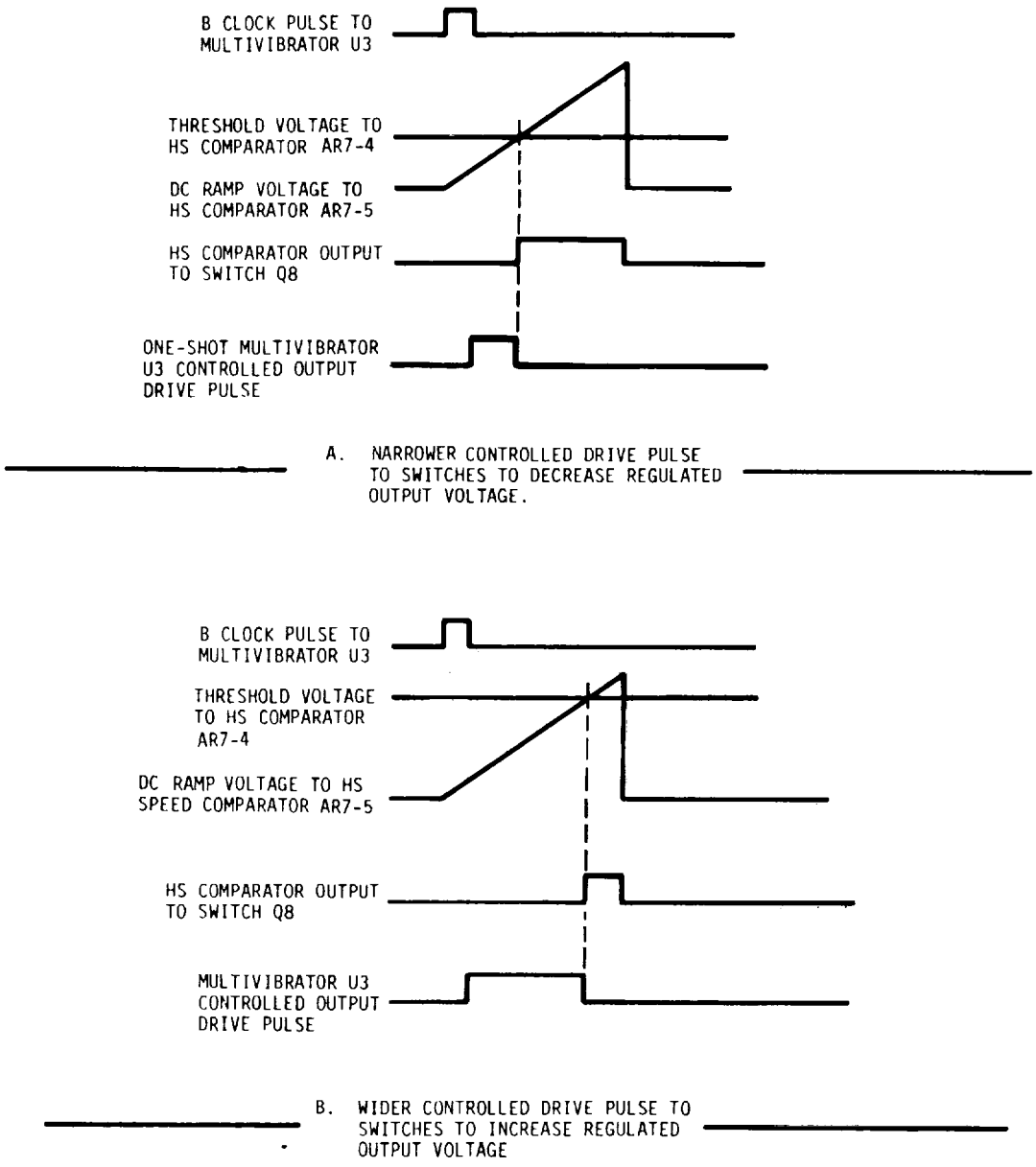


Figure 5-48. ±12-Volt Regulator Circuit-Waveform Diagram

Each switch, in turn, generates equal amounts of energy that is coupled to its associated rectifier circuit. The four dc outputs from the rectifier circuits are connected in parallel and applied to the one +5-volt filter circuit. The output from the filter circuit is the +5V Reg output that is applied to power the logic cir- cuits in the multiplexer set.

5-630. DETAILED CIRCUIT DISCUSSION.

5-631. The incoming 115-volt ac source power is applied to the +150-volt power supply and to stepdown transformer T6 as shown on the overall power supply schematic. The +150-volt power supply consists of full-wave rectifier CR1 through CR4, filters L4 and L5, and capacitors C18 and C19. The unregulated +150-volt output from the power supply is applied to one side of transformers T1 through T5 to provide the driving power for switches Q1 through Q10. In turn, the +150-volt common (return) from the opposite end of T1 through T5 is applied to the switch circuits through +12-volt driver card A3 and +5-volt driver card A4. Stepdown transformer T6 produces a 18.5 vac input to full-wave rectifier circuits CR1 through CR4 on mother board A1. Diodes CR2 and CR4 and capacitor C2 produce the +12V (c) output and diodes CR1 and CR3, together with capacitor C1 produce the -12V (c) output. These two dc voltages provide power to the clock generator and the control circuits.

5-632. As shown on the +12-volt regulator card schematic, the constant current generator circuit consists of current amplifier Q3 and breakdown diodes VR5 and VR6. Potentiometer R18 is factory set to provide a fixed bias voltage to amplifier AR5-12. Amplifier AR5-12, in turn, produces the constant +4.77V Ref output that is applied to AR2-10 in the +5-volt power supply and to AR6-10 in the ±12-volt regulator circuit. The +4.77V Ref is also applied to the +5-volt regulator circuit on +5-volt regulator card A2.

5-633. The +5-volt power supply consists of amplifier AR2-10, switch Q7, breakdown diode VR8, and amplifier Q5, Q6. Amplifier AR2-10 and switch Q7 form a low input voltage protection circuit for the overall power supply. When the incoming 115 vac decreases to 95 vac or less, the inverting input to AR2-7 decreases and the output from AR2-10 to Q7 goes more positive. Switch Q7 is driven into conduction and effectively shorts out the voltage across breakdown diode VR8. This condition biases Q5 and Q6 into cutoff. When Q5 and Q6 are cutoff, the absence of the +5V (c) output shuts down the overall power supply. When the incoming ac voltage increases to 100 vac, the output voltage level from AR2-10 decreases, switch Q7 is biased off, and Q5, Q6 again conduct to produce the +5V (c) output. When the +5V (c) output is generated, the overall power supply circuits are energized and return to normal operation.

5-634. The -12-volt over/under voltage detector circuit consists of comparator AR3-10, CR4, and CR3. The +12-volt over/under voltage detector circuit consists of comparator AR3-12, CR5, and CR6. Comparator ARl-12, CR1, and CR2 make up the +5-volt over/under voltage detector circuit. The outputs of the three comparators are connected through CR2, CR4, and CR6 to breakdown diode VR1 in the inverting input of comparator AR1-10. When the -12V Reg output increases to -14.4 volts, the output of AR3-10 increases to cause current to flow through VR1. This condition places a high in- put to AR1-7 to produce a low output at AR1-10. The low output from ARl-10 shuts off switch Q4. This inhibits the generation of the A clock and B clock signals to disable the overall power supply regulated outputs.

When the +12V Reg output increases to +14.4 volts or the +5V Reg output increases to +6 volts, the same procedure is repeated through diode CR2 or CR4 to cause switch ^{Q4} to be shut off and disable the clock generator.

5-635. In the under voltage condition, the output voltage level from AR3-10 decreases when the -12V Reg output de- creases to -10.8 volts. This condition causes current to flow through CR3 to place a negative potential on the inverting input of AR2-1. This causes the voltage level from AR2-12 to increase and bias Q1 into conduction and cutoff $^{Q2.}$ As a result, Q1 produces the low- level local alarm signal (PSF-) and Q2 produces the high-level remote alarm signal (PSFR). Potentiometer R27 is factory set to establish the bias on voltage for AR2-12 for an under- voltage condition. When the +12V Reg output decreases to +10.8 volts or the +5V Reg output decreases to +4.5 volts, the same procedure is repeated through diode CR1 or CR3 to force AR2-12 to bias Q1 into conduction and cutoff Q2 to produce the two alarm signals.

5-636. When the temperature in the power supply increases to 205°F, thermostat switch S1 on the power supply chassis closes. When S1 closes, a signal ground (HOT-) path to the front panel is completed and causes over temp signal (IPSE-) to be generated by the circuits on the front panel. The over temp signal is applied to the power supply as an inhibit signal to the negative input of AR1-10. This inhibit signal causes AR1-10 to bias switch Q4 into conduction and disable the clock generator and shut down the overall power supply. The over temp signal from the front panel holds the power supply in the shut down condition until the POWER CONTROL ON/OFF switch on the front panel is set to-the OFF and then back to the ON position. Removing the TEMP SHUTDOWN jumper on the front panel inhibits the generation of the over temp signal to shut down the power supply when an over-temperature condition exists.

5-637. When the SELF TEST switch on the front panel is set to the ON position, the self-test signal is applied to the power supply. The self-test signal biases on Q14 in the input circuit of AR1-12. When Q14 is on, an under volt- age condition is simulated and ARl-10 causes the local and remote alarm signals to be generated until the self- test signal is removed from the input of Q14.

5-638. The 18-kHz output from 18-kHz oscillator AR4 in the clock generator is applied to switch Q4. Switch Q4 in turn, is switched on and off at the 18-kHz rate. The pulses from Q4 are applied through inverter U2-11 to inverter U2-3 and the B clock flip-flop U1l-5. The B clock flip-flop, in turn, produces 9-kHz, B clock pulses to one-shot multivibrator U3-10 in the +12-volt regulator circuit. The B clock signals are also applied to the +5-volt regulator circuits on card A2. The 18-kHz pulses are routed through inverter U2-3 to A-clock flip-flop Ul-9 (figure 5-49) to produce the 9-kHz clock pulse's.

5-639. In the following discussion, the -12V Reg output is assumed to be decreasing to a less-negative voltage level. The same function also represents the condition where the +12V Reg output decreases to a less-positive voltage level. The decreasing -12-volt input to AR6-1 causes a lower output from AR6-12 that is applied to AR6-7. The non-inverting input to AR6-6 is connected to the +4.77V Reg voltage. The inverting input receives the negative- going input and causes the output voltage from AR6-10 to increase. Thus the output voltage from AR6-10 applied to AR7-4 becomes a higher threshold voltage level for the stage.

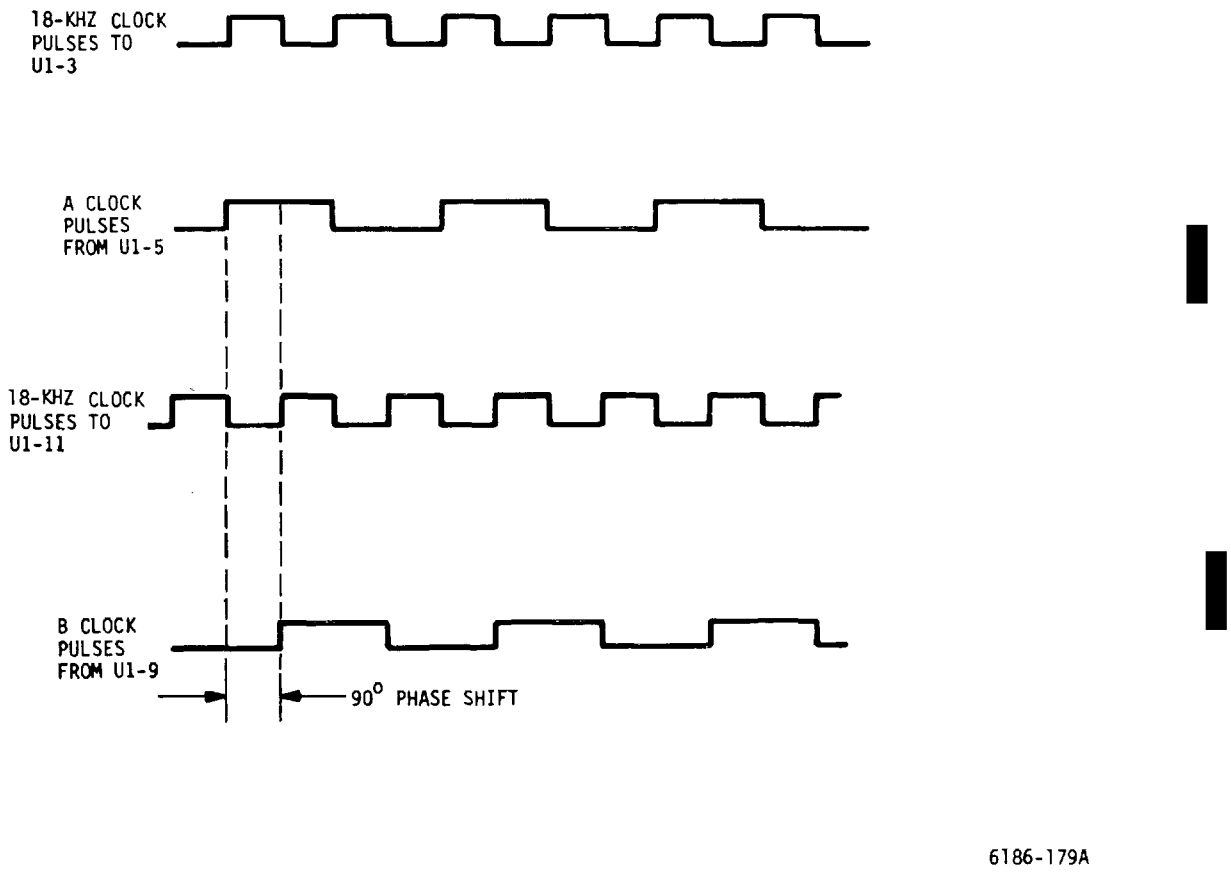


Figure 5-49. A Clock and B Clock Waveform Diagram

At the same time, the dc ramp voltage is applied to the non- inverting input of AR7-5. Since the threshold voltage has increased, a more positive (longer time duration) dc ramp voltage level is required to cause the output voltage from AR7-10 to go more positive to cutoff switch Q8. The longer it takes to cutoff Q8, the longer that one-shot multivibrator U3 is allowed to conduct when it is triggered on by a B clock pulse. In turn, the more negative that the regulated -12 volts be- comes, a less positive voltage level is established for the threshold voltage applied to AR6-7. This lower threshold voltage level results in a narrower pulse being produced from U3.

5-640. The functional operation of the four +5-volt regulators on the +5-volt regulator card A2 are basically the same as the operation described in paragraph 5-639. As shown on the +5-volt regulator card schematic, one voltage comparator circuit and error amplifier serve the four +5-volt regulator circuits. Any change in the +5-volt regulated out- put is sensed by voltage comparator AR4-12. The comparator, in turn, produces a voltage change to the input of AR4-10. The output from AR4-10 is applied as the threshold voltage to the inverting inputs of the high-speed comparators in the four +5-volt power regulator circuits. The four drive pulses from the four regulators are produced through pulse transformers T2, T4, T6, and T8.

5-641. The Q1 drive pulses from the +12-volt regulator circuit and the Q4 drive pulses from the +5-volt regulator circuits are applied through the +12- volt driver card A3 to switches Q1, Q2 and Q3, Q4. The Q5, Q8, and Q9 drive pulses are applied through +5-volt driver card A4 to switches Q5, Q6, Q7, Q8, and Q9, Q10. The operation of each of the four pairs of drive switches are functionally the same. Therefore only the +12-volt drive switches Q1, Q2 are described in paragraph 5-462.

5-642. As shown on the +12-volt driver card schematic, the current feed- back voltage applied to the +12-volt regulator circuit is developed across emitter resistor R4 that is associated with switch Q2. Capacitor C7 and diode CR2 on card A3 are part of the bias circuit for switch Q1, Q2. The Q1 drive pulse from the +12-volt regulator circuit on card A1 is applied through resistor R2 and capacitor C6 to the base of switch Q1. The drive pulses for switch Q4 in one of the +5-volt power supply circuits is also routed through this card. The drive pulses for three of the +5-volt power supply circuits are processed through similar circuits on the +5-volt driver card.

5-643. Switches Q1, Q2, as shown on the overall power supply schematic, are switched on during the time a Q1 drive pulse is applied to them. When the switches are on, energy is stored in the primary winding (pins 1 and 2) of transformer T1. The amount of energy stored in the winding is proportional to the time that a drive pulse is applied to the switches. When the drive pulse terminates, Q1, Q2 are switched off and the energy is coupled through the secondary windings (pins 7 and 8 for +12 volts) (pins 3 and 4 for -12 volts) of transformer T1 to the +12- and -12-volt filter circuits. The +12-volt output from T1 is filtered by choke L1 and its associated components. The -12-volt output from T1 is filtered by choke L2 and its associated components.

5-644. The four switch circuits for the four +5-volt power supplies are identical and are functionally the same as the $\pm$12-volt switch circuit described in paragraph 5-462. In the generation of the +5-volt regulated output, the four sets of switches (Q3 through Q10) are each pulsed at 90-degree intervals to provide a constant energy input to the +5-volt filter network. Each of the four drive pulses applied to the four switch circuits have the same pulse widths to provide the same energy levels to the filter network. The timing relationship of the four drive pulses are shown in figure 5-50. Choke L3 and its associated components form the +5-volt filter network.

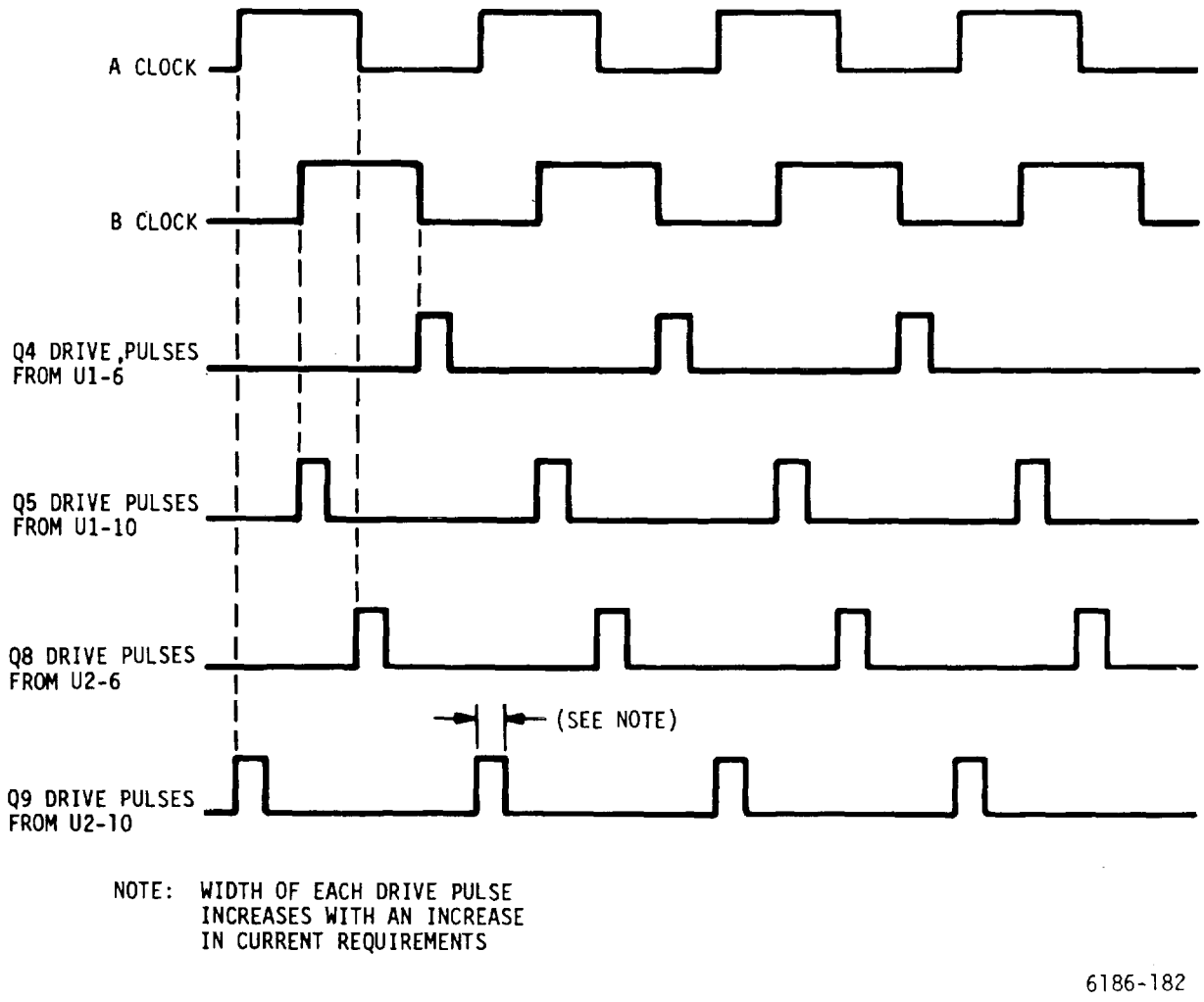


Figure 5-50. +5- Volt Drive Pulses - Waveform Diagram

CHAPTER 6

MAINTENANCE

SECTION I

ORGANIZATIONAL AND INTERMEDIATE LEVEL MAINTENANCE

6-1. INTRODUCTION.

6-2. This section provides instructions and data necessary for the performance of organizational and intermediate level maintenance of the multiplexer set. Included are procedures for the use of built-in test features, and repair and replacement procedures for major multiplexer components. Data useful for isolation of faults not treated by built-in test features are also provided, as are procedures for all required preventive maintenance activities.

6-3. The multiplexer set represents a mixture of high-performance solid state logic and analog technologies. Personnel attempting detailed intermediate level maintenance of the multiplexer set should be highly familiar with general maintenance and troubleshooting methods applicable to solid state integrated circuit equipment and should have a thorough understanding of the multiplexer set theory of operation.

6-4. GENERAL.

6-5. Maintenance of the multiplexer set at the organizational and intermediate levels encompasses both corrective and preventive tasks. Most malfunctions are detected and isolated to the replaceable item (printed circuit card or power supply) by the use of test features that are integral to the equipment design. Repair of such malfunctions is accomplished by item replacement, with de- tailed item repair reserved for a depot or other off-site facility. Malfunctions occurring in the chassis wiring, backplane wiring of the card file, and discrete chassis and front panel piece parts are diagnosed and isolated by the use of conventional troubleshooting techniques. Repair of such malfunctions is accomplished by wire or piece part re- placement as applicable.

6-6. MAINTENANCE SUPPORT EQUIPMENT.

6-7. Table 6-1 lists the tools and test equipment required for support of organizational and intermediate level maintenance of the multiplexer set. Brief summaries of pertinent performance characteristics are also provided. The items listed in table 6-1 are preferred for multiplexer set maintenance.

6-8. FAULT ISOLATION, USING BUILT-IN DIAGNOSTIC FEATURES.

6-9. GENERAL. Most multiplexer set malfunctions are detected and isolated by the use of built-in diagnostic features. The built-in diagnostics operate in three modes: automatic, self- test, and lamp test. Self-test and lamp test modes are manually initiated.

6-10. AUTOMATIC MODE. In the automatic mode, both power supply and printed circuit card malfunctions are automatically detected and isolated. A front panel display (figure 4-1) identifies the malfunctioning items. For power supply faults, the front panel POWER SUPPLY indicator is lighted. For card faults, either the MULTIPLEXER CARD or DEMULTI- PLEXER CARD indicator is lighted and the slot number of the faulty card appears in the FAULT LOCATION display. Whenever an automatic display of a power supply or card fault occurs, perform steps 1 through 10 (power supply fault) or 11 through 15 (card fault) as follows:

Table 6-1. Organizational/Intermediate Level Support Equipment (Equivalent equipment is authorized.)

Item	National Stock No./ Part No.	Pertinent Characteristics
Digital communications test set: Model 7003 (or equivalent data test set)	None Harris	a. Output rate of 10 Hz to 3 MHz. b. Self-clocking comparator. c. Pseudorandom output pattern of 2^{3-1} or greater bits in length. d. Error insertion and detection.
Electronic equipment tool kit TK-105/G	5180-00-610-8177	
Frequency counter: Hewlett-Packard Model 5245M--8	6625-00-992-3586	a. Frequency range of 0 to 10 MHz. b. Accuracy of $\pm$1 count plus time base accuracy of 4.5×10^{-8}. c. Time base aging rate of less than 5×10^{-10} parts/day. d. Sensitivity of 100 mv rms. e. Eight-digit display.
Multimeter: Triplett Model 630A	6625-00-553-0251	a. Accuracy of $\pm$1.5% dc, and $\pm$3.0% ac. b. Resistance measurement accuracy of $\pm$10% over range of 1.0 ohm to 10 megohms.
Oscilloscope, consisting of:	6625-00-115-2402	a. Vertical bandwidth of r50 MHz. b. Rise time of 2.4 nsec.
Oscilloscope main frame: Tektronix Model R7704A		c. Dual-trace operation. d. Calibrated vertical deflection over range of 2 mv/division to 5 v/division.
Dual vertical amplifier: Tektronix Model 7A26		e. Calibrated horizontal defection over range of 20
Probe: Tektronix Model P6063A		
Time base: Tektronix Model 7B92		
Universal counter: Tektronix Model 7D15		

Table 6-1. Organizational/Intermediate, Level Support Equipment (Cont) (Equivalent equipment is authorized.)

Item	National Stock No./ Part No.	Pertinent Characteristics
Portable test set: Hewlett-Packard Model 3550B	6625-00-244-3032	a. Generates audio frequency of 1 kHz ±5% at -16 ±0.1 dBm. b. Measures audio voltage of +7 dBm at 1 kHz ±5% to accuracy of ±0.1 dBm. c. Input/output impedance of 600 ohms (balanced).
Wire-wrap repair kit, consisting of:	Martin Marietta P/N SK62759367	
Cut/strip accessory	Gardner-Denver P/N 515654	Accepts 28 AWG solid insulated wire.
Unwrapping tool	Gardner-Denver P/N 511203	Unwraps left-hand or right-hand wrapped connections of 28 AWG solid wire.
Wire wrapping tool	Gardner-Denver P/N 14XA2-B3C-(28)	Accepts 28 AWG wrapping bits and sleeves.
Wrapping bit	Gardner-Denver P/N 508748	Accepts 28 AWG solid wire.
Wrapping sleeve	Gardner-Denver P/N 507100	Accepts 28 AWG solid wire.

1. Observe which display is lighted. If a card error is displayed, also observe the card number appearing in the FAULT LOCATION display.

2. Momentarily press front panel DISPLAY RESET switch.

NOTE

Reappearance of the initial error display indicates that the detected error is not transitory in nature and must therefore be corrected.

3. Upon release of DISPLAY RESET switch, observe that the initially displayed error reappears. If a power supply error is displayed, proceed to step

4. If a card error is displayed, proceed to step 11.

WARNING

Hazardous voltages are present at the power supply electrical connectors. Turn off operating power and disconnect power cord before attempting power supply replacement; otherwise, personnel death or injury may result.

4. Set POWER CONTROL switch to OFF.

5. Disconnect multiplexer set power cord from its source outlet.

6. Replace power supply assembly as prescribed in paragraph 6-23.

7. Connect multiplexer set power cord to its source outlet.

8 Set POWER CONTROL switch to ON.

9. Momentarily press DISPLAY RE-SET switch.

10. Upon release of DISPLAY RESET switch, observe that all front panel error displays remain out and POWER CON- TROL ON indicator is lighted.

11. If the card number appearing in the FAULT LOCATION display is 15 or less, replace card as prescribed in paragraph 6-22. If the displayed card number is 16 or greater, set POWER CONTROL switch to OFF, and then replace card as prescribed in paragraph 6-22.

12. If POWER CONTROL switch was previously set to OFF, set switch to ON.

13. Momentarily press DISPLAY RE-SET switch.

NOTE

MULTIPLEXER OUT OF TOL indicator may be lighted after step 14 is per- formed. When indicator is lighted, wait approx- imately 40 seconds and repeat step 14.

14. Upon release of DISPLAY RESET switch, observe that all front panel error displays remain out and POWER CON TROL ON indicator is lighted.

15. Perform a self-test of the multiplexer set diagnostic circuits as prescribed in paragraph 6-32.

6-11. SELF-TEST MODE. A manually initiated self-test mode is provided for detection and isolation of faults occurring in the diagnostic circuits on the multiplexer set printed circuit cards. Faults detected during self-test are displayed by front panel error indicators. In the self-test mode, the MULTIPLEXER CARD and DEMULTIPLEXER CARD indicators are normally lighted and the number 00 appears in the FAULT LOCATION display. (Refer to paragraph 6-32 for self-testing procedures.) An abnormal display is indicative of a card with faulty diagnostic circuits; perform corrective action as follows:

1. With SELF TEST switch in on (up) position, observe which error indicator (MULTIPLEXER CARD or DEMULTI- PLEXER CARD) is not lighted, and the card number that appears in the FAULT LOCATION display.

NOTE

The SELF TEST switch must remain in the on (up) position for approximately 15 seconds before final error information is displayed.

2. If the card number appearing in the FAULT LOCATION display is 15 or less, replace card as prescribed in paragraph 6-22. If the displayed card number is 16 or greater, set POWER CONTROL switch to OFF, and then replace card as pre- scribed in paragraph 6-22.

3. If POWER CONTROL switch was previously set to OFF, set switch to ON.

4. Set SELF TEST switch of off (down) position.

5. Momentarily press DISPLAY RE-SET switch.

6. Upon release of DISPLAY RESET switch, observe that all front panel error indicators remain out and POWER CONTROL ON indicator is lighted.

7. Perform a self-test as pre- scribed in paragraph 6-32.

6-12. LAMP TEST MODE. A lamp test feature is provided for detection and isolation of defective front panel indicator lamps and displays. Perform detection and isolation procedures as follows:

1. Press LAMP TEST switch and observe which front panel indicator lamp or FAULT LOCATION display is not lighted or is indicating an incorrect number.

NOTE

During lamp test, the correct numerical indication for the FAULT LOCATION display is 88.

2. Release LAMP TEST switch and set POWER CONTROL switch to OFF.

3. Replace indicator lamp or numerical display-element observed in step 1 as prescribed in paragraph 6-25 or 6-26, respectively.

4. Set POWER CONTROL switch to

5. Momentarily press front panel DISPLAY RESET switch.

6. Upon release of DISPLAY RESET switch, observe that all error indicators remain out and POWER CONTROL ON indicator is lighted.

7. Perform a lamp test as pre- scribed in paragraph 6-33.

6-13. TROUBLESHOOTING.

6-14. GENERAL. Although the multiplexer set has many built-in diagnostic features, certain limited types of mal- functions must be isolated by the use of conventional troubleshooting techniques. The following paragraphs provide useful information for performance of such troubleshooting.

6-15. Table 6-2 lists a number of abnormal multiplexer set operating symptoms, together with their probable causes. Appropriate corrective actions are also listed. Table 6-3 lists, by name, the signals appearing within the multiplexer set. The function of each signal is also listed. Special purpose switch data useful in troubleshooting the equipment are listed in table 6-4.

6-16. Many numbered test points are located at the outer edges of the cards within the multiplexer set. Most maintenance-significant operating and diagnostic signals are routed to these test points. The signals appearing at these test points are listed in table 6-3. The signals appearing at other card edge test points may be identified by referring to the logic diagrams in the circuits diagram manual.

6-17. EXTENDER CARD USAGE. Monitoring of a signal on a card that does not appear at a card edge test point is accomplished by using the extender card (extender card assembly P/N 61864080- 009), which is stored in slot 22 of the

Table 6-2. Troubleshooting Symptoms

SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
	Thermal Indications	
TEMPERATURE indicator lighted; equipment previously operating normally	a. Dirty air filters.	Clean filters.
	b. Defective cooling blower,	Replace blower.
	c. Defective thermostat.	Replace power supply.
	d. Defective front panel relay K2 or associated component.	Replace K2 or associated component as required.
TEMPERATURE indicator lighted; POWER CONTROL switch in OFF position.	Power removed with SELF TEST switch in on position.	Momentarily open circuit breaker to unlatch front panel relay K2.
Cooling blower inoperative following replacement of blower panel.	Blower panel retaining screws not sufficiently tightened to activate interlock switch.	Tighten screws.
	Power Indications	
POWER SUPPLY indicator lighted; equipment operates normally.	Marginally low power supply output voltage.	Replace power supply.
Power supply shuts down automatically; equipment temperature normal.	a. Defective power supply.	Replace power supply.
	b. Defective front panel isolator AT1 or associated component. P/N 61861028.	Replace or repair front panel card assembly
	c. Loose connection in secondary distribution bus.	Tighten terminal connections. (See paragraph 6-23.)
POWER CONTROL ON indicator out; equipment operates normally.	Defective POWER CONTROL ON indicator lamp.	Replace lamp.

Table 6-2. Troubleshooting Symptoms (Cont)

SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
	Out-of-Tolerance Indications	
OUT OF TOL indicator lighted and multiple-channel numbers appearing in FAULT LOCATION display; equipment previously operating normally.	a. Input data rates out of tolerance.	Correct data source.
	b. Reference timing oscillator out of calibration.	Calibrate reference timer card.
	c. Defective reference timer card.	Replace card.
OUT OF TOL indicator lighted and a single-channel number appearing in FAULT LOCATION display; source is within tolerance.	a. Defective channel card. b. Defective gated clock/Replace card. data mux card.	Replace card.
OUT OF TOL indicator lighted and multiple-channel numbers appearing in FAULT LOCATION display immediately following equipment reconfiguration.	Improper strapping of sequencer card.	Correct card strapping.
	Card Error Indications	
Demultiplexer channel card error not correctable by card replacement.	Shorted output cable.	Replace or repair cable.
Any card error not correctable by card replacement.	Signal short on card(s) being driven by indicated card.	Sequentially replace driven cards until error is removed.
Multiple demultiplexer channel card errors not correctable by card replacement (digital only).	Defective error rate detector/remote alarms card.	Replace card.

Table 6-2. Troubleshooting Symptoms (Cont)

SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
Miscellaneous Indications		
LOSS OF MUX TIMING indicator lighted.	a. External reference timing signal missing.	Correct signal source.
	b. Defective reference timer card.	Replace card.
LINK ERROR RATE indicator continuously lighted or lights intermittently.	a. Data errors being inserted by data transmission system.	Correct transmission system.
	b. Defective error rate detector/remote alarms card.	Replace card.
DISPLAY RESET switch does not reset error indicators.	a. Defective DISPLAY RESET switch.	Replace switch.
	b. Defective display card.	Replace card.
Improper SELF TEST switch operation.	a. Defective SELF TEST switch.	Replace switch.
	b. Defective display card.	Replace card.
Improper display in lamp test.	a. Defective LED element (U1 or U2) or defective indicator lamp.	Replace LED element or lamp as required.
	b. Defective LAMP TEST switch.	Replace switch.
	c. Defective front panel circuit U3, U4, or U8.	Replace or repair front panel card assembly P/N 61861028.
LOSS OF DEMUX TIMING indicator lighted.	a. Demultiplexer input timing signal missing.	Correct signal source.
	b. Defective overhead enable generator card.	Replace card.
	c. Defective frame sync card.	Replace card.

Table 6-2. Troubleshooting Symptoms (Cont)

SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
Miscellaneous Indications (Cont)		
LOSS OF FRAME A indicator lighted; equipment previously operating normally.	a. Demultiplexer input data signal missing.	Correct signal source.
	b. Defective frame sync card.	Replace card.
LOSS OF FRAME A indicator lighted immediately following equipment reconfiguration.	Demultiplexer port strapping not same as transmitting multiplexer port strapping.	Correct port strapping error.

Table 6-3. Signal Name and Test Point List

Signal Name	Function	Test Point[1]
NOTE **To locate a signal name prefixed by M (multiplexer) or D (demultiplexer), delete the prefix and locate the remainder of the signal name. For example, signal MNSE- is listed as NSE-, etc.**		
ACFANH	Fan ac (hot)	
ACFANN	Fan ac (neutral)	
ACINH	AC input (hot)	
ACINN	AC input (neutral)	
ACPSH	Power supply ac (hot)	
ACPSN	Power supply ac (neutral)	
ATA	Demux input data	
ATA-	Demux input data	
CHAD 1	Channel address 1 (binary 1)	M/D21-10
CHAD 2	Channel address 2 (binary 2)	M/D21-11
CHAD 4	Channel address 4 (binary 4)	M/D21-12
CHAD 8	Channel address 8 (binary 8)	M/D21-13

See footnote at end of table.

Table 6-3. Signal Name and Test Point List (Cont)

Signal Name	Function	Test Point[1]
CHMAXO	Maximum channel number (binary 1)	
CHMAX1	Maximum channel number (binary 2)	
CHMAX2	Maximum channel number (binary 4)	
CHMAX3	Maximum channel number (binary 8)	
CHSGRD	Chassis ground	
DM-	Mux data mux diagnostic	M20-8
DON	Demux diagnostics on	
DTOXX	Mux channel data out (1 thru 15)	_ _ _2
ENAO	No-action stuff code errors (binary 1)	
ENA1	No-action stuff code errors (binary 2)	
ENA2	No-action stuff code errors (binary 4)	
ENSO	Negative stuff code errors (binary 1)	
ENS1	Negative stuff code errors (binary 2)	
ENS2	Negative stuff code errors (binary 4)	
EOS	End of scan	
EOS-	End of scan	
EOS2	End of scan + 2 bits	M/D21-1
EOS2B	End of scan + 2 bits, buffered	
EOS2B-	End of scan + 2 bits, buffered	
EOS3NX	End of scan 3 (1 thru 4)	
EPSO	Positive stuff code errors (binary 1)	
EPS1	Positive stuff code errors (binary 2)-	
EPS2	Positive stuff code errors (binary 4)	
ERD-	Error rate detector diagnostic	

See footnotes at end of table.

Table 6-3. Signal Name and Test Point List (Cont)

Signal Name	Function	Test Point[1]
ERRS	Demux error reset	
ERRS-	Demux error reset	M17-6
ERST	Error reset	
ERST-	Error reset	
ERSTSW	Error reset switch	
ERSTSW-	Error reset switch	
FAIL	Card failure	M22-7
FAILC1	Card failure (remote alarm contact 1)	
FAILC2	Card failure (remote alarm contact 2)	
FS	Frame sync	D16-11
FSD-	Frame sync diagnostic	D16-6
GC-	Gated clock	M/D20-7
GCXX	Gated clock (1 thru 15)	_ _ _3
GDXX	Output data ground (1 thru 15)	
GNDD	Ground	
GRD1	Signal ground	
GRD2	Signal ground	
GRD3	Signal ground	
GRD4	Signal ground	
GTXX	Output timing ground (1 thru 15)	
HOT-	Overtemperature	
IPSE-	Inhibit power supply	
IXX	Mux channel data in (1 thru 15)	_ _ _4, 5
IXX-	Mux channel data in (1 thru 15)	_ _ _4, 5

See footnotes at end of table.

Table 6-3. Signal Name and Test Point List (Cont)

Signal Name	Function	Test Point[1]
LBS-	Loss of bit sync	D16-3
LDCRD	Demux card error (to lamp)	
LDTIM	Loss of demux timing (to lamp)	
LEOS	Loss of end of scan	
LEOS-	Loss of end of scan	M/D21-15
LERRC1	Link error rate (remote alarm contact 1)	
ILERRC2	Link error rate (remote alarm contact 2)	
LLER	Link error rate (to lamp)	
LLOFA	Loss of frame A (to lamp)	
LLOFB	Loss of frame B (to lamp)	
ILMCRD	Mux card error (to lamp)	
1, MOOT	Mux out of tolerance (to lamp)	
LOF	Loss of frame	
LOFAC1	Loss of frame A (remote alarm contact 1)	
LOFAC2	Loss of frame A (remote alarm contact 2)	
LOFBC1	Loss of frame B (remote alarm contact 1)	
LOFBC2	Loss of frame B (remote alarm contact 2)	
LOT-	Loss of timing	
LOTRA-	Loss of timing remote alarm	
LT	Lamp test	
LTIM	Loss of mux timing (to lamp)	
LW28-	Loss of word 28	D20-8
MF=PS	Minor frame = port sequence	M/D21-7
MF31X-	Minor frame terminal count (A thru D)	_ _ _6, 7

See footnote at end of table.

Table 6-3. Signal Name and Test Point List (Cont)

Signal Name	Function	Test Point[1]
MFC0	Minor frame count 0 (binary 1)	
MFC1	Minor frame count 1 (binary 2)	
MFC2	Minor frame count 2 (binary 4)	
MFC3	Minor frame count 3 (binary 8)	
MFC4	Minor frame count 4 (binary 16)	M20-16
NAC	No-action code	D20-12
NSA	Negative stuff acknowledge	M/D19-7
NSC	Negative stuff code	D20-11
NSE	Negative stuff enable	D16-4, M/D20-4
NSTXX-	Negative stuff request (1 thru 15)	_ _ _8
OD-	Demux overhead data (to minor frame counter)	
OH0	Overhead address count 0 (binary 1)	
OH1	Overhead address count 1 (binary 2)	
OH2	Overhead address count 2 (binary 4)	
OH3	Overhead address count 3 (binary 8)	
OOTC1	Out of tolerance (remote alarm contact 1)	
OOTC2	Out of tolerance (remote alarm contact 2)	
OOTXX-	Out of tolerance (1 thru 15)	
OXX	Demux channel data out (1 thru 15)	_ _ _9
OXX-	Demux channel data out (1 thru 15)	_ _ _10
PSA	Positive stuff acknowledge	M/D19-5
PSA-	Positive stuff acknowledge	
PSC	Positive stuff code	D20-10

See footnotes at end of table.

Table 6-3. Signal Name and Test Point List (Cont)

Signal Name	Function	Test Point[1]
PSE	Positive stuff enable	D16-5, M/D20-3
PSF-	Power supply failed	
PSFC1	Power supply fail (remote alarm contact 1)	
PSFC2	Power supply fail (remote alarm contact 2)	
PSFLT-	Power supply failed lamp test	
PSFR	Power supply fail	
PSTXX-	Positive stuff request (1 thru 15)	_ _ _11
PUB0	Ports in use 0 (binary 1)	
PUB1	Ports in use 1 (binary 2)	
PUB2	Ports in use 2 (binary 4)	
PUB3	Ports in use 3 (binary 8)	
PUB4	Ports in use 4 (binary 16)	
RBI	Ripple blanking input	
RI	Demux input system clock	
RIO	System clock	M/D 20-1, _ _ _5
RIOX-	System clock (1 thru 8)	M/D 19-15, _ _ _7
RO	Mux output system clock	M16-13
RT-	Reference timer diagnostic	M16-14
RTA	Reset temperature alarm	
SD	Serial data	
SD-	Serial data	
SDATAO	Serial data out	M16-3
SDATAO-	Serial data out	M16-4
SEQ-	Sequencer diagnostic	M/D21-16

See footnotes at end of table.

Table 6-3. Signal Name and Test Point List (Cont)

Signal Name	Function	Test Point[1]
ST1-	Self-test enable No. 1	
ST2-	Self-test enable No. 2	M17-8
STPS	Self-test power supply	
STS	Self-test switch	
STS-	Self-test switch	
SYNC-	Demux frame sync	D16-14
T3600X	3600 Hz to transition encoder (A thru C)	M16-16
T4800X	4800 Hz to transition encoder (A thru C)	M16-15
TA0	Tens address (binary 1)	
TA1	Tens address (binary 2)	
TEMPC1	Temperature (remote alarm contact 1)	
TEMPC2	Temperature (remote alarm contact 2)	
TERDXX	Input data ground (1 thru 15)	
TERTXX	Input timing ground (1 thru 15)	
TIMIN	Multiplexer timing in	M16-5
TIMIN-	Multiplexer timing in	M16-6
TIMOUT	Multiplexer timing out	M16-12
TIMOUT-	Multiplexer timing out	M16-ll
TIX-	Demux channel data	_ _ _12
TIXX	Channel timing in (1 thru 15)	_ _ _5, 13
TIXX-	Channel timing in (1 thru 15)	_ _ _5, 13
TM+	Demux input timing	
TM-	Demux input timing	

See footnotes at end of table.

Table 6-3. Signal Name and Test Point List (Cont)

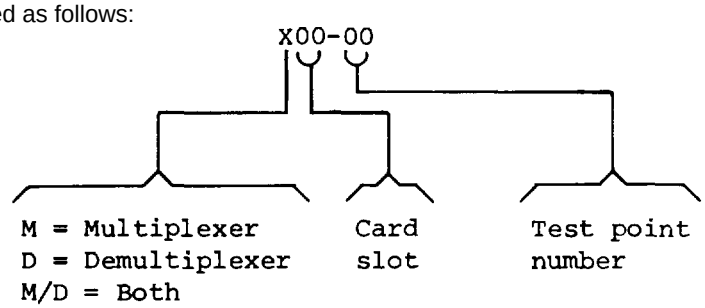
Signal Name	Function	Test Point[1]
TMOG-	OEG card diagnostic	M/D19-9
TOXX	Demux channel timing out (1 thru 15)	_ _ _ 14
TOXX-	Demux channel timing out (1 thru 15)	_ _ _ 15
UA0	Units address (binary 1)	
UA1	Units address (binary 2)	
UA2	Units address (binary 4)	
UA3	Units address (binary 8)	
W240X-	Word 24 bit 0 (1 thru 4)	_ _ _ 16
W2429	Word 24 thru word 29	D/M 19-13, _ _ 7-
W24NX-	Word 24 (1 thru 4)	
W28	Word 28	
W29	Word 29	
W29-	Word 29	
WC0	Word count 0	
WC1	Word count 1	
WC2	Word count 2	
WC4	Word count 4	
WPR-	Demux word counter preset	_ _ _ 5, 17
-12V	-12 volts	M17-2
+12V	+12 volts	M17-4
+12PSF	+12 volts to power supply failed lamp	
-12PSFR	-12 volts to power supply failed relay	
24EOS2	Word 24 end of scan 2	
+5A1	+5 volts (phase locked loop)	

See footnotes at end of table.

Table 6-3. Signal Name and Test Point List (Cont)

Signal Name	Function	Test Point[1]
+5A2	+5 volts (phase locked loop)	
+5R	+5 volts thru resistor	_ _ _ 5, 19
+5V1	+5 volts	M17-14
+5V2	+5 volts	M17-14
+5V3	+5 volts	M17-14

[1]Test point location data are listed as follows:



[2]Signal appears at TP1 on RCB card, at TP16 on VE card, and at TP6 on TE/TR card.

[3]Signal appears at TP12 on TE/TR card and at TP8 on TD card.

[4]Signal appears at TP12 on RCB and VE cards.

[5]Input signal after buffering, level shifting, or inversion.

[6]Signal appears at TP13 on GC/DM card in multiplexer.

[7]Output signal before buffering, level shifting, or inversion.

[8]Signal appears at TP16 on RCB card and at TP11 on TE/TR card.

[9]Signal appears at TP2 on SB, NBSB, and TD cards, and at TP1 on VD card.

[10]Signal appears at TP1 on SB, NBSB, and TD cards.

[11]Signal appears at TP15 on RCB card, at TP13 on VE card, at TP9 on TE/TR card, at TP14 on VD card, at TP16 on SB and NBSB cards, and at TP13 on TD card.

[12]Signal appears at TP15 on SB card and at TP6 on TD card.

[13]Signal appears at TP4 on RCB card.

[14]Signal appears at TP6 on SB and NBSB cards.

[15]Signal appears at TP5 on SB and NBSB cards.

[16]Signal appears at TP13 on TE/TR card and at TP8 on OEG card.

[17]Signal appears at TP9 on GC/DM card in demultiplexer.

[18]Signal M24EOS2 appears at TP1 and signal D24EOS2 appears at TP2 on display card.

[19]Signal appears at TP9 on GC/DM card in multiplexer.

Table 6-4. Special Purpose Switch Data

Location	Switch	Function
Display card	S1	Diagnostic NORM/MUX OFF/DEMUX OFF switch. In the MUX OFF position, all multiplexer error displays are inhibited. In the DEMUX OFF position, all demultiplexer error displays are nhibited. In the NORM position, all multiplexer and demultiplexer error display circuits are enabled.
FS card	S3A, S3B	NORM/LOOPBACK switch. In LOOPBACK position, these switches connect serial data and timing outputs of the multiplexer to serial data and timing inputs of the demultiplexer.
OEG card	S1	Fifteen-section DIAGNOSTICS AND OVERHEAD switch. Each separate section has ON and OFF positions, and is associated with one channel. In OFF position, a positive stuff request (MPSTXX- or DPSTXX-) originating at a channel card is inhibited at the OEG card. This precludes the display of channel card errors, and prevents the channel card (multiplexer only) from receiving positive stuff overhead service.
RCB card	S6	DIAG ON/OFF switch. In OFF position, switch inhibits normally generated card error signals from leaving the RCB card. The error signal generated during self-test is not inhibited in either the OFF or ON switch position.
RCB card	S7	OOT out-of-tolerance ON/OFF switch. In OFF position, switch inhibits an out-of-tolerance signal from leaving the RCB card.
RT card	S3	Phase adjustment switch. Adjusts phasing of TIMOUT and TIMOUT- signals generated by RT card. Switch is set to position most nearly provided coincidence between transitions of TIMOUT and TIMOUT- signals.
SB card	S4	DIAG ON/OFF switch. Function of this switch is same as that described for S6 on the RCB card.
TD card	S1	DIAG ON/OFF switch. Function is same as that described for S6 on the RCB card.
TE/TR card	S8	NORM/DIAG OFF switch. Function is same as that described for S6 on the RCB card.

DEMULTIPLEXER row. Perform the following procedures when the extender card is required to monitor signals on a functional card:

1. Set POWER CONTROL switch to OFF.

2. Remove, from its normal card file position, the functional card to be extended.

CAUTION

The extender card must be installed properly to prevent shorting of power signals. Before installing extender card, ensure that part number (61864080-009) side of card is facing right-hand side of multiplexer set, and card edge having multiple keying slots is pointing toward bottom of multiplexer set.

3. Insert extender card into card slot from which functional card was removed.

CAUTION

Ensure that component (parts) side of functional card plugged into extender card is pointing toward right- hand side of multiplexer set.

4. Insert functional card into extender card.

5. Set POWER CONTROL switch to ON.

CAUTION

When probing individual integrated circuit (IC) pins, ensure that power and ground pins are not inadvertently shorted to each other or to other signal pins. See figure 6-1 for typical pin arrangements.

NOTE

Cards are coated with a fungus-preventive material. Use a sharply pointed probe to ensure penetration of coating.

6. Using typical integrated circuit pin arrangements shown in figure 6-1 as a reference, carefully probe desired point on extended card.

7. Upon completion of monitoring operations, set POWER CONTROL switch to OFF and return extender card to slot 22 and functional card to its normally installed position.

6-18. CONTINUITY CHECK. Complete multiplexer set wiring and cabling data are provided in the circuits diagram manual. When performing continuity checks of the card file wiring plane, it may be necessary to use extender card assembly P/N 61864080-009, which is located in slot 22 of the DEMULTIPLEXER row. To use the extender card for this purpose, proceed as follows:

1. Set POWER CONTROL switch to OFF.

2. Remove the functional card located in the slot associated with the connector to be monitored.

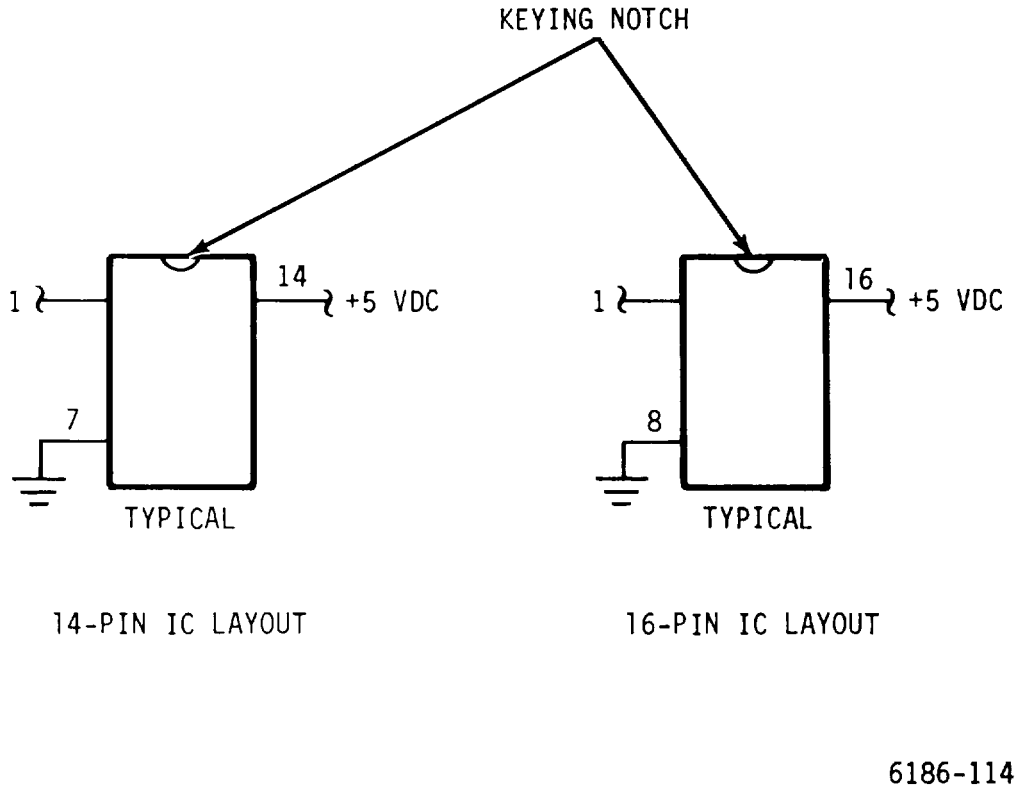


Figure 6-1. Typical integrated Circuit Pin Arrangement - Top View

CAUTION

The extender card must be installed properly. Before installing extender, ensure that part number (61864080-009) side of extender card is facing right-hand side of multiplexer set, and card edge having multiple keying slots is pointing toward bottom of multiplexer set.

3. Insert extender card into desired card connector and perform continuity measurements of the desired pin(s). Pin number references are etched on the extender card surface.

4. Upon completion of continuity measurements, return extender card and previously removed functional card to their normally installed positions.

6-19. SPECIAL PURPOSE SWITCH USAGE. The plug-in cards in the multiplexer set contain switches that are potentially useful during certain maintenance and troubleshooting processes. Generally, these switches allow selected diagnostic or error signals to be inhibited or with- held from the error display circuits. The ability to withhold certain error signals may be useful in cases involving two or more simultaneous malfunctions or when transient error conditions are being experienced. Table 6-4 lists the special purpose switches located in the multiplexer set and briefly describes the function of each. Reference to appropriate logic diagrams located in the circuits diagram manual is suggested for specific switch function details.

6-20. REPAIR AND REPLACEMENT.

6-21. GENERAL. Repair and/or replace- ment of multiplexer set items subject to corrective maintenance at the organizational/intermediate level are contained in paragraphs 6-22 through 6-29. Included are procedures for replace- ment of printed circuit cards, the power supply, the front panel, front panel lamps and display LED elements, and the power supply cooling blower. Card file backplane wiring repair and paint touchup procedures are also included.

WARNING

Hazardous voltages are present within the multiplexer set chassis. Un- less otherwise directed, always set POWER CONTROL switch to OFF before replacing multiplexer set assemblies, subassemblies, or parts. The 115-volt ac is always applied to the POWER CONTROL switch on the front panel when source power is applied through the power cable to the multiplexer set.

6-22. PRINTED CIRCUIT CARD. Replace a printed circuit card as follows:

1. Loosen the 20 captive screws securing front cover (figure 6-2) to the chassis.

2. Remove front cover and set aside.

3. Locate desired card by the numbers etched on bar at middle of card file (figure 6-2). Cards comprising the multiplexer function are located in the upper (MULTIPLEXER) row of card slots, and demultiplexer cards are located in the lower (DEMULTIPLEXER) row of card slots.

4. Grasp ejector devices at up- per and lower corners of desired card, and remove card by lifting ejectors away from card edge.

5. Carefully align replacement card with desired card slot, ensuring that component side of card faces right- hand side of chassis.

6. Insert card into card slot until card connector just meets back- plane receptacle.

7. Firmly press outer edge of card until card is felt to snap into its mating backplane receptacle.

8. Install front cover and tighten captive screws securing cover to chassis.

6-23. POWER SUPPLY. Replace the power supply assembly as follows:

CAUTION

Use care when extending and rotating the chassis upon its slides. Extend and/or rotate chassis slowly and ensure that slides lock in desired position before starting power supply replacement.

NOTE

Replacement of the power supply requires free access to the top of the multiplexer set chassis. If the set is installed in an equipment rack, the set must be loosened from the rack and extended on its mounting slides before power supply replacement is started. Depending upon the particular installation, the chassis may also have to be rotated downward to the 900 (horizontal) position to enable power supply replacement.

1. Loosen and remove power supply access cover (figure 6-2) located at top of chassis.

2. Loosen and remove nuts and washers securing the +5V and 5V COM cables to power supply terminal studs W1-1 and W2-1 (figure 6-3).

3. Loosen and remove screws securing the -12, COM, and +12 leads to TB1 terminals 1 through 3 (figure 6-3).

4. Unlock connector mating with J1 (figure 6-3) by sliding locking strip until it is free of locking pins; then disconnect connector.

5. Loosen eight captive fasteners securing power supply to multiplexer set chassis.

6. Carefully move all disconnected cables away from power supply to provide a free path for power supply removal.

CAUTION

The power supply assembly weighs approximately 25 pounds. Grasp handles securely before lifting power supply from chassis.

7. Using handles provided, carefully lift power supply from chassis.

8. Install nuts and washers re- moved in step 2.

9. Carefully install replace- ment power supply in multiplexer set chassis, ensuring that previously disconnected cables are not wedged under power supply.

10. Engage and tighten eight power supply securing fasteners.

11. Connect and lock connector J1.

CAUTION

Ensure that connections to TB1 are firmly secured to prevent excessive voltage drops due to contact resistance.

Torque nuts on W1-1 and W1-2 to proper value to prevent possible intermittent operation of equipment.

12. Connect and tighten the -12, COM, and +12 leads to TB1 terminals 1, 2, and 3, respectively.

13. Torque lower level nuts on W1-1 and W2-1 between 25 to 30 inch- pounds. Install +5V and 5V COM cables to studs W1-1 and W2-1. Torque upper level nuts between 25 to 30 inch-pounds.

14. Place lifting handles in storage (horizontal) position.

15. Install and secure power supply access cover.

16. If the chassis was previously extended and/or rotated on its mounting

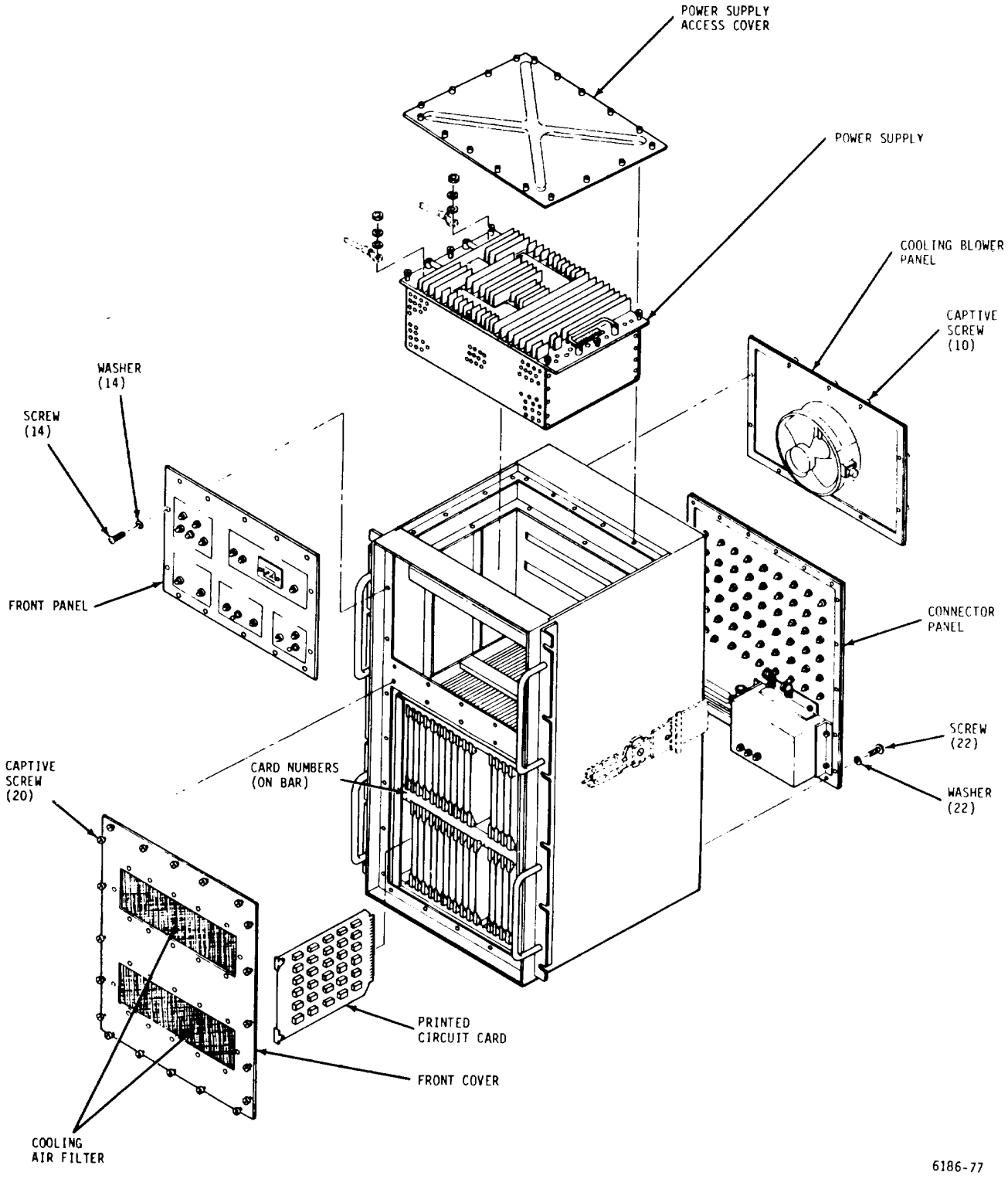


Figure 6-2. Multiplexer Set Physical Arrangement

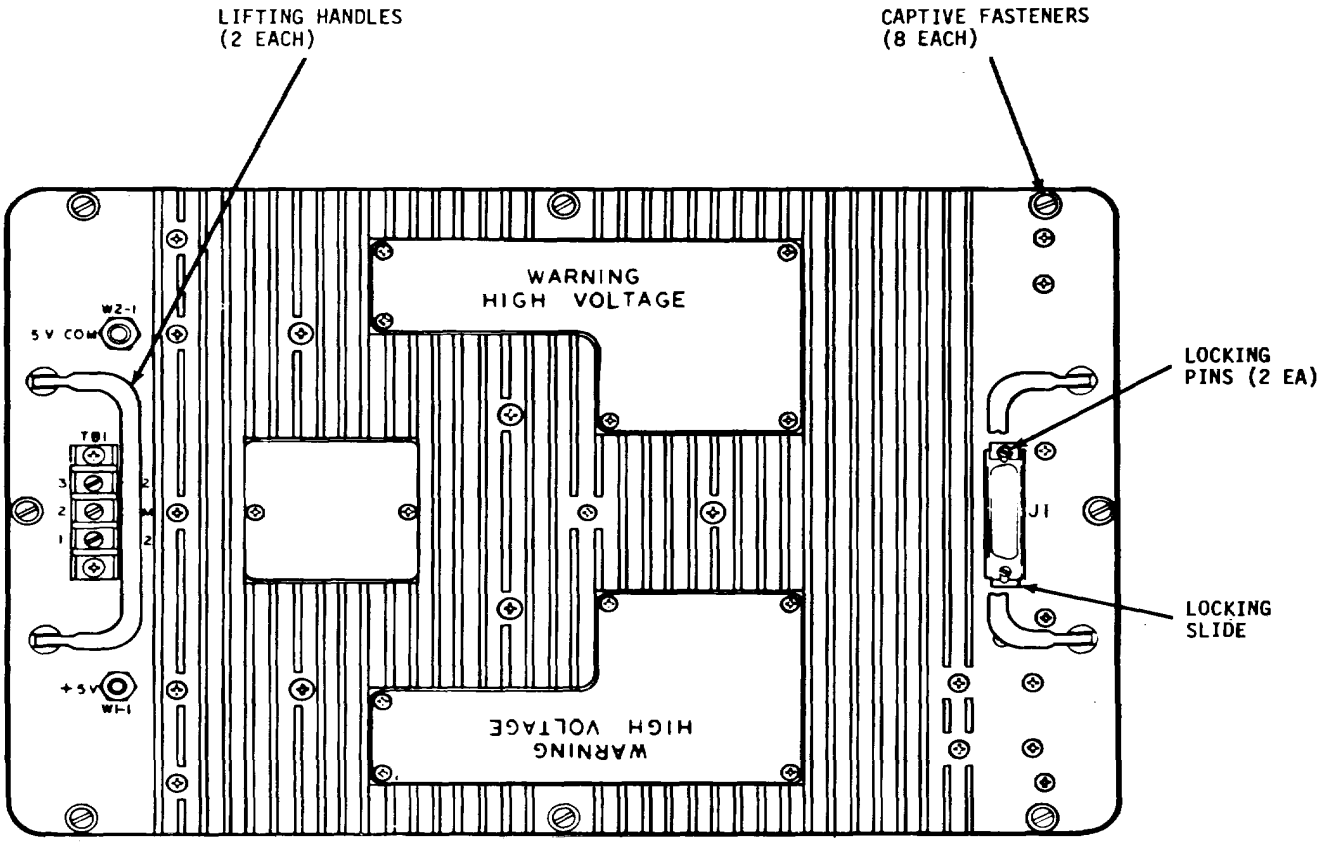


Figure 6-3. Power Supply - Top View

slides, return it to its normally installed position and secure chassis to its mounting rack.

6-24. FRONT PANEL ASSEMBLY. Replace the front panel assembly (figure 6-2) as follows:

WARNING

Hazardous voltages are present within the front panel. The 115-volt ac is always applied to the POWER CONTROL switch on the front panel when source power is applied through the power cable to the multiplexer set.

1. Disconnect power cable from POWER INPUT connector on rear of multiplexer set.

2. Loosen and remove 14 screws and washers securing front panel to multiplexer set chassis.

3. Carefully tilt top of front panel out from chassis to gain access to the two interconnecting cables.

4. Remove two screws securing each cable connector and separate each cable connector from front panel.

5. Remove front panel assembly.

6. Position replacement front panel assembly to enable mating of the two interconnecting cable connectors to connectors on the panel.

7. Mate and secure each connector, using screws removed in step 4.

8. Position front panel assembly on multiplexer set chassis and install 14 screws and washers to secure front panel to chassis.

9. Reconnect power cable to POWER INPUT connector on rear of multiplexer set.

6-25. FRONT PANEL INDICATOR LAMP. Replace an individual front panel indicator lamp as follows:

1. Remove screw-on indicator lens cap.

2. Pull plug-in lamp from its socket.

3. Align pins of replacement lamp with its socket and press lamp firmly into place.

4. Install and tighten indicator lens cap.

6-26. LED ELEMENT. Replace a light- emitting diode (LED) element of the FAULT LOCATION display as follows:

1. Remove two screws securing FAULT LOCATION display bezel and filter (figure 6-4) and remove bezel and filter assemblies.

2. Using an orange-wood stick or other similar instrument, carefully pry plug-in LED element from its socket.

3. Align replacement LED element with front panel socket and press firmly into place.

4. Install filter and bezel assemblies and secure with two retaining screws.

6-27. COOLING BLOWER. Replace the multiplexer set cooling blower as follows:

WARNING

Exercise care to ensure that hands or foreign objects are not placed in contact with the rotating blower fan.

CAUTION

- Use care when extending and rotating the chassis upon its slides. Extend and/or rotate chassis slowly and ensure that slides lock in the desired position before starting blower replacement.

- Don't leave equipment ON with fan removed for more than 20 minutes.

NOTE

- The cooling blower panel is fitted with electrical inter- locks that enable blower replacement without removal of multiplexer set operating power.

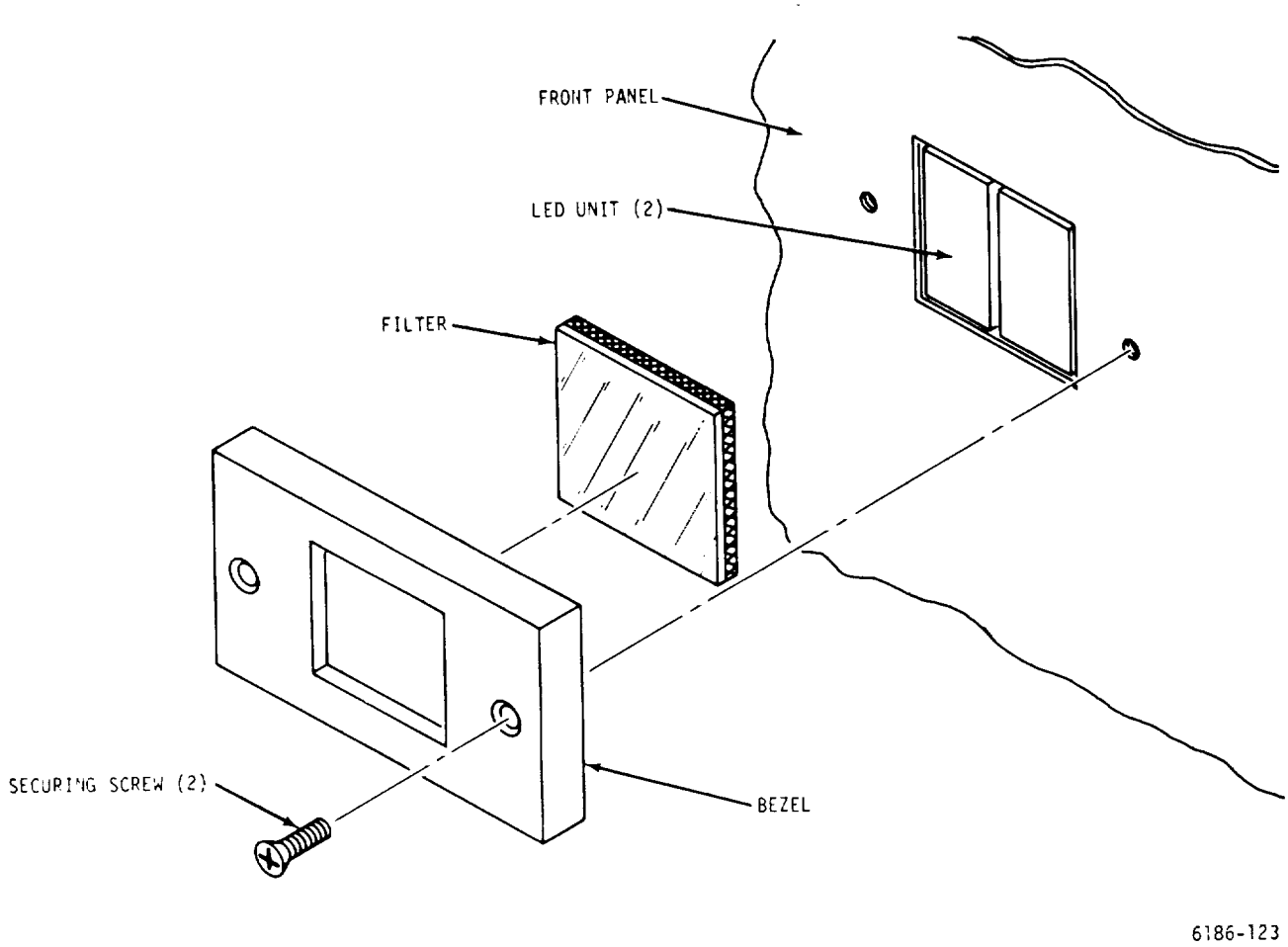


Figure 6-4. LED Element Replacement

Blower replacement requires free access to the rear of the multiplexer set chassis. The chassis may have to be extended and rotated on its mounting slides before blower replacement is started.

1. Loosen 10 captive fasteners securing cooling blower panel (figure 6-2) to rear of multiplexer chassis.

2. Tilt top of blower panel out from chassis until electrical interlock is actuated. Interlock actuation is evidenced by an audible and visible slowing of the cooling blower fan.

3. When fan comes to a full stop, carefully lift blower panel from chassis and disconnect the blower's partial-turn power connector. Set panel on a bench or other suitable work surface.

4. Loosen but do not remove three screws securing blower to blower panel.

5. Align three flat-sided nuts on blower retaining screws so that flat side of each is parallel with blower housing.

6. Remove blower assembly.

7. Position replacement blower assembly onto blower panel and rotate three flat-sided retaining screw nuts so that flat side of each is perpendicular to blower housing. Tighten retaining screws while preventing nuts from turning out of alignment with blower housing.

8. Position blower panel near chassis and mate blower power connector.

9. Install blower panel and tighten its 10 captive fasteners to secure blower panel to chassis. Observe that blower fan rotates at its normal operating speed.

10 When applicable, rotate and retract chassis to its normal vertical installation position and secure it to mounting rack.

6-28. BACKPLANE WIRING. Repair the card file backplane wiring as follows:

WARNING

Hazardous voltages are present within the multiplexer set chassis. Turn off operating power and disconnect power cord before attempting repair; otherwise, personnel death or injury may result.

CAUTION

Use care when extending and rotating the chassis upon its slides. Extend and/or rotate chassis slowly and ensure that slides lock in the desired position before starting repairs.

NOTE

Repair of the backplane wiring requires free access to the rear of the multiplexer set chassis. If the set is installed in an equipment rack, the set must be loosened from the rack and extended on its mounting slides before repair is started. Depending upon the particular installation, the chassis may have to be rotated downward to the 900 (horizontal) position to enable repair.

1. Set POWER CONTROL switch to OFF.

2 Disconnect multiplexer set power cord from its source outlet.

3. Disconnect and tag or otherwise label all external signal cables connected to connector panel (figure 6-2) on rear of multiplexer set chassis.

4. Disconnect cables from POWER INPUT and REMOTE ALARMS receptacles on connector panel.

5. Remove 22 screws and washers securing connector panel to chassis.

6. Lift top of connector panel away from chassis to provide working access to interface connectors P1 and P2.

7. Disconnect connectors P1 and P2; remove connector panel from chassis and set it down to provide working access to card file wiring plane.

CAUTION

Backplane wires are solid. To avoid wire breakage, do not bend or flex the wires excessively.

8. Using a soldering aid or other suitable tool, locate and expose the wire to be repaired or replaced. See figure 6-5 for typical connector pin identification and layout information.

WARNING

When unwrapping backplane wires, ensure that broken wire ends do not drop into wiring backplane. Failure to remove all loose conductive materials from the backplane can result in serious equipment damage.

NOTE

If there is sufficient unused space on the terminal posts associated with the wire to be replaced, it may not be necessary to unwrap the ends of the defective wire. When sufficient post space exists, carefully cut each end of the wire being replaced as shown in figure 6-6, view A. The new wire is then installed on the previously unused post space as shown in figure 6-6, view B, and as prescribed in steps 10 through 14.

9. Using unwrapping tool P/N 511203 (figure 6-7), carefully unwrap each end of the wire to be replaced. Remove wire from backplane.

NOTE

When more than one wire is attached to a terminal post, it may be necessary to unwrap one or more wires before reaching the wire to be replaced. Tag or otherwise label these wires to facilitate their replacement.

10. Cut a replacement wire approximately 4 to 6 inches longer than the wire being replaced. Strip each end approximately 1 inch, using cut/strip accessory P/N 515654 attached to the wire wrapping tool (figure 6-7, view A).

NOTE

Before proceeding, determine that wire wrapping tool P/N 14 XA2-B3C-(28) is fitted with wrapping bit P/N 508748 and wrapping sleeve P/N 507100.

11. Insert and anchor one end of replacement wire as far as possible into small hole of wrapping bit (figure 6-7, view B).

12. Position wrapping tool and slide wrapping bit onto desired terminal post (figure 6-7, view B).

13. Momentarily trigger wrapping tool until tool backforce ceases and tool runs free. Remove wrapping tool from terminal post.

NOTE

Rewrapping of the stripped portion of a previously unwrapped wire should not be attempted. Always cut and restrip a wire end before wrapping is attempted.

14 Repeat steps 11 through 13 for each wire end to be wrapped.

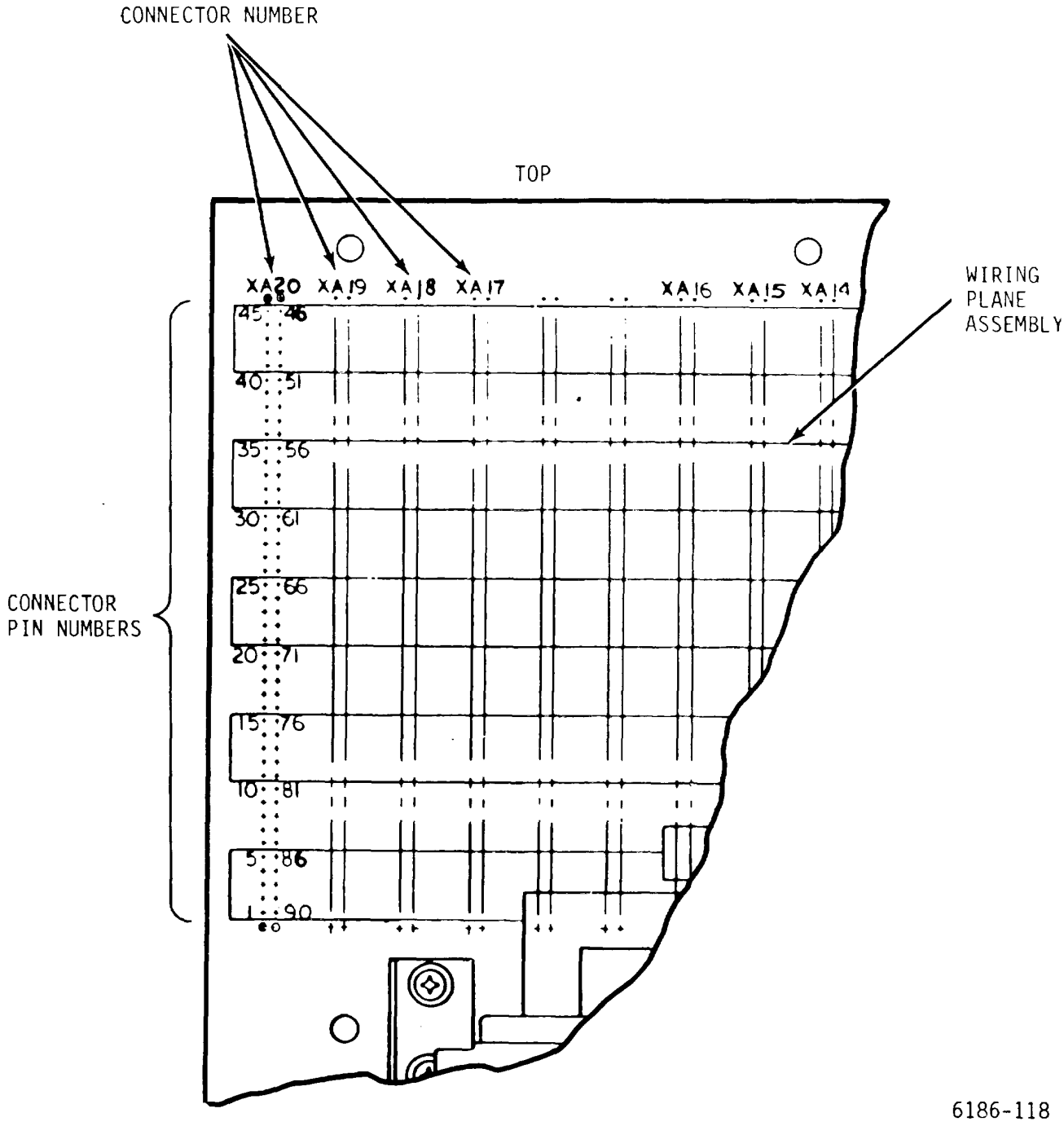


Figure 6-5. Typical Backplane Connector Pin Location Arrangement

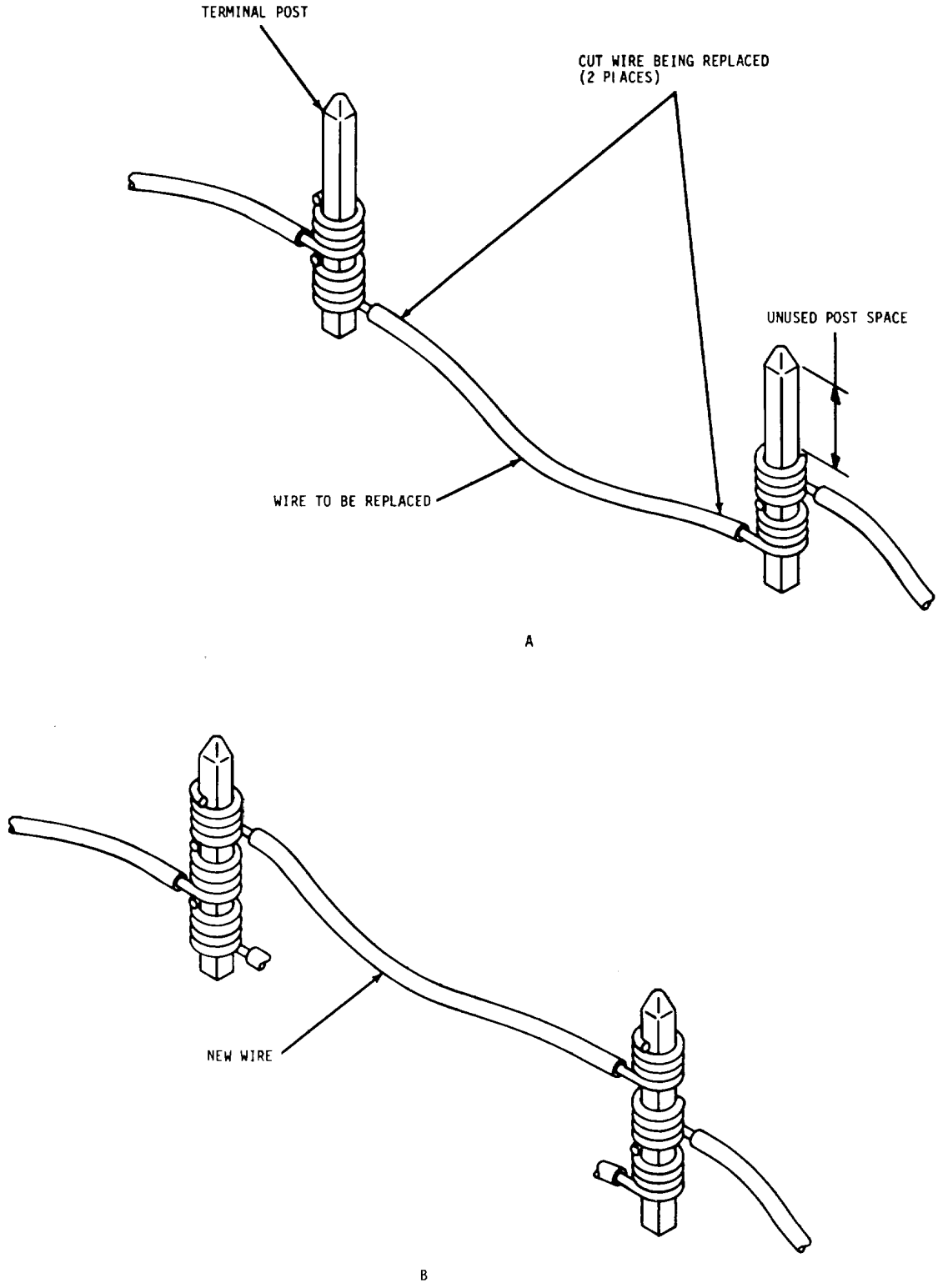


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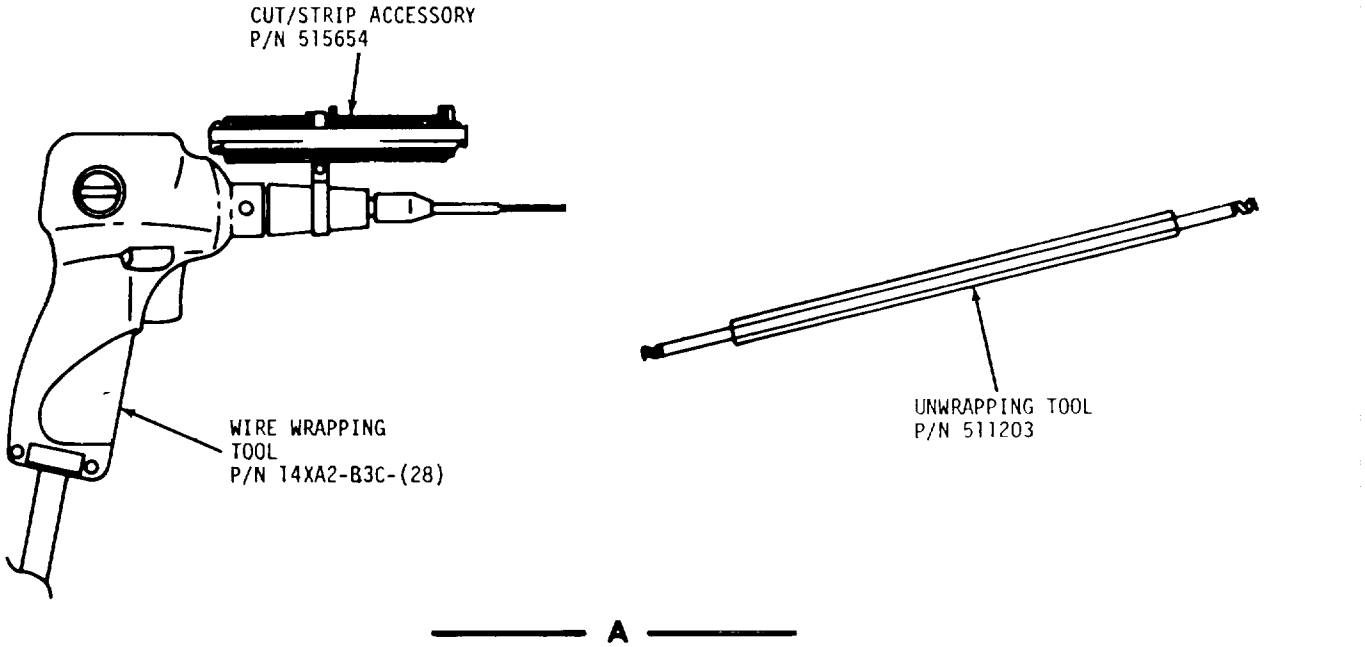
Figure 6-6. Backplane Wire Replacement Diagram

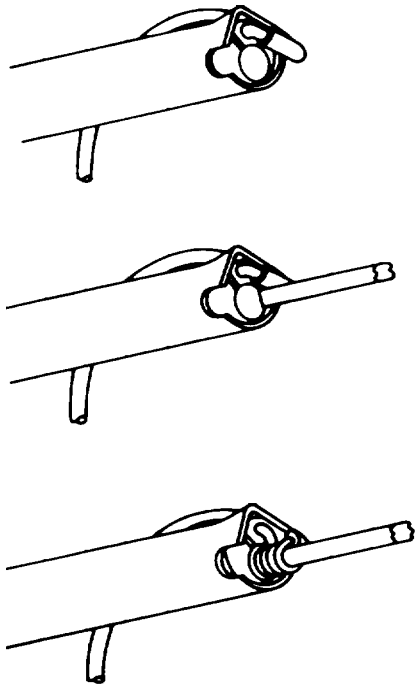


A

1. WIRE INSERTION AND ANCHORING THE WIRE IS INSERTED INTO THE WIRE SLOT OF THE WRAPPING BIT AS FAR AS POSSIBLE. A FUNNEL-SHAPED INDENTATION AT THE TIP OF THE SLEEVE ALLOWS EASY INSERTION. THE WIRE IS THEN BENT (ANCHORED) BACK INTO THE NOTCH OF THE WRAPPING SLEEVE.

2. TERMINAL INSERTION TOOL IS POSITIONED WITH THE TERMINAL HOLE OF THE WRAPPING BIT OVER THE TERMINAL POST TO BE WRAPPED.

3. WRAPPING THE TRIGGER IS SQUEEZED AND A SLIGHT AMOUNT OF BACKFORCE IS APPLIED. (BACKFORCE IS THE FORWARD PRESSURE APPLIED BY THE OPERATOR AND VARIES WITH WIRE SIZE.)



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6186-122

Figure 6-7. Wire Wrapping Tools and Simplified Wire Installation Procedures

15. Carefully inspect entire wiring plane surface for evidence of loose foreign materials such as broken wire ends. Remove such items before proceeding

16. Tilt connector panel partially into place and mate connectors P1 and P2 disconnected in step 7

17 .Place connector panel against multiplexer set chassis and install 22 screws and washers removed in step 5.

18. Connect cables removed in step 4 to POWER INPUT and REMOTE ALARMS receptacles.

19. Mate all signal cables disconnected in step 3 to connector panel.

20. If multiplexer set chassis was extended and/or tilted prior to start of backplane repair, return chassis to its normally installed position and secure it to mounting rack.

6-29. PAINT TOUCHUP. Touch up chips, scratches, or other minor damage on exterior painted surfaces of the multiplexer set chassis as follows:

1. Lightly sand the affected surface area, using a medium grade of sandpaper. Ensure that any visible signs of corrosion are removed.

2. Using a small clean brush, apply one coat of zinc chromate primer per MIL-P-8585 to any exposed metal surface area. Let surface dry.

3. Using a small clean brush, apply one coat of semigloss enamel per TT-E-529 (color No. 26440 per FED-STD595) to entire sanded area. Let surface dry

6-30. PREVENTIVE MAINTENANCE.

6-31. GENERAL. Preventive maintenance of the multiplexer set consists of periodic self-testing and lamp testing, calibration of reference timing sources, and routine inspection and cleaning. Table 6-5 lists required preventive maintenance tasks, together with their performance frequency. Preventive maintenance procedures are presented in the following paragraphs.

Table 6-5. Preventive Maintenance Summary

Preventive Maintenance Task	Task Frequency
Perform diagnostic self-test.	Daily
Perform lamp test	Daily
Calibrate reference timer assembly.	28 days
Calibrate transition encoder/timing recover assembly.	28 days
Clean cooling air filters	28 days
Perform visual inspection.	28 days

6-32. DIAGNOSTIC CIRCUIT SELF-TESTING. Self-testing of the multiplexer set diagnostic circuits is performed to determine that the circuits are capable of detecting and displaying faults occurring in the operating circuits. Perform a diagnostic self-test as follows:

NOTE

- **Self-testing of the multiplexer set requires that the set be properly configured (chapter 3).**

- **The performance of self-test procedures overrides the diagnostic function while in the self-test mode, but does not affect or interrupt the functional operation of the circuits in the multiplexer set.**

1. Observe that all front panel alarm and error indicators are out and POWER CONTROL ON indicator is lighted.

2 Set front panel SELF TEST switch to on (up) position.

3. Observe that all front panel indicators are lighted and the number 00 appears in the FAULT LOCATION display.

NOTE

For multiplexer output rates (R_o) above 10 kbps, the time required for a final display of self-test results is approximately 10 seconds. For output rates below 10 kbps, the test time increases as R_o decreases. Maximum test time at an output rate (Ro) of 155 bps can reach approximately 10 minutes. Maximum test time for output rates below 10 kbps may be estimated, using the expression:

Time (seconds)= $\frac{90{,}000}{R_o}$

4. Set front panel SELF TEST switch to off (down) position. If the proper display was observed in step 3, the self-test procedure is complete. If an incorrect display was observed, refer to paragraph 6-11 for corrective maintenance instructions.

6-33. LAMP TESTING. Lamp testing is performed to determine that the front panel alarms and displays are capable of indicating detected alarm and error conditions. Perform a lamp test as follows:

NOTE

The performance of lamp test procedures does not affect or interrupt the functional operation of the circuits in the multiplexer set.

1. Press front panel LAMP TEST switch and observe that all front panel indicators are lighted and the number 88 appears in the FAULT LOCATION display.

2 .Release LAMP TEST switch. If a proper display was observed in step 1, the lamp test is complete. If an incorrect display was observed, refer to paragraph 6-12 for corrective maintenance instructions.

6-34. RT CARD CALIBRATION. Calibration of the RT card is performed to ensure that the output frequencies of the reference timing and transition encoding oscillators are within prescribed tolerances. The calibration is performed, using a Hewlett-Packard Model 5245M frequency counter. The RT card is located in multiplexer card file slot 16 (figure 1-2). Perform calibration procedures as follows:

NOTE

To ensure proper calibration, allow the frequency counter to warm up for approximately 15 minutes before making frequency measurements.

1. Loosen and remove printed circuit access cover (figure 6-2) located at front of chassis.

NOTE

Steps 2 through 4 are applicable only when the multiplexer is operating from an internally generated reference timing signal (paragraph 3-74). If the multiplexer is operating from a station clock or other external reference timing signal, proceed to step 5.

2 Connect frequency counter to test point TP-10 of RT card (figure 6-8) and measure output frequency of reference timing oscillator Y1.

NOTE

The multiplexer set is initially delivered with a reference timing oscillator whose nominal output frequency is 9.8304 MHz. For certain applications, oscillators of different frequencies may be installed. If the frequency measured at TP-10 is not approximately 9.8304 MHz, determine the specified nominal frequency of the installed oscillator before proceeding.

3. Determine if the frequency measured in step 2 is within plus or minus one part in 107 of the oscillator's specified output frequency. If the measured frequency is within this tolerance, proceed to step 5. If the measured frequency exceeds this tolerance, proceed to step 4.

NOTE

When the nominal specified frequency of the installed oscillator is 9.8304 MHz, the acceptable tolerance is
$\frac{+9.8304 \times 10^6}{10^7}$ **or approximately Hz.**

4. Using a standard screwdriver, remove protective cover from RT card reference timing oscillator adjustment control (figure 6-8). Using an electronic tuning tool, slowly rotate oscillator adjustment control until frequency measured at TP-10 of RT card is within the tolerance established in step 3. Replace protective cover.

5. Connect frequency counter to TP15 of RT card (figure 6-8) and measure frequency of transition encoding signal.

6 Determine that the frequency measured in step 5 is 4800 $\pm$0.24 Hz.

7 .If the measured frequency is within tolerance, proceed to step 8. If the measured frequency is not within tolerance, set POWER CONTROL switch to OFF and replace RT card as prescribed in paragraph 6-22. Set POWER CONTROL switch to ON and repeat steps 5 through 7.

8. Install and tighten printed circuit card access cover.

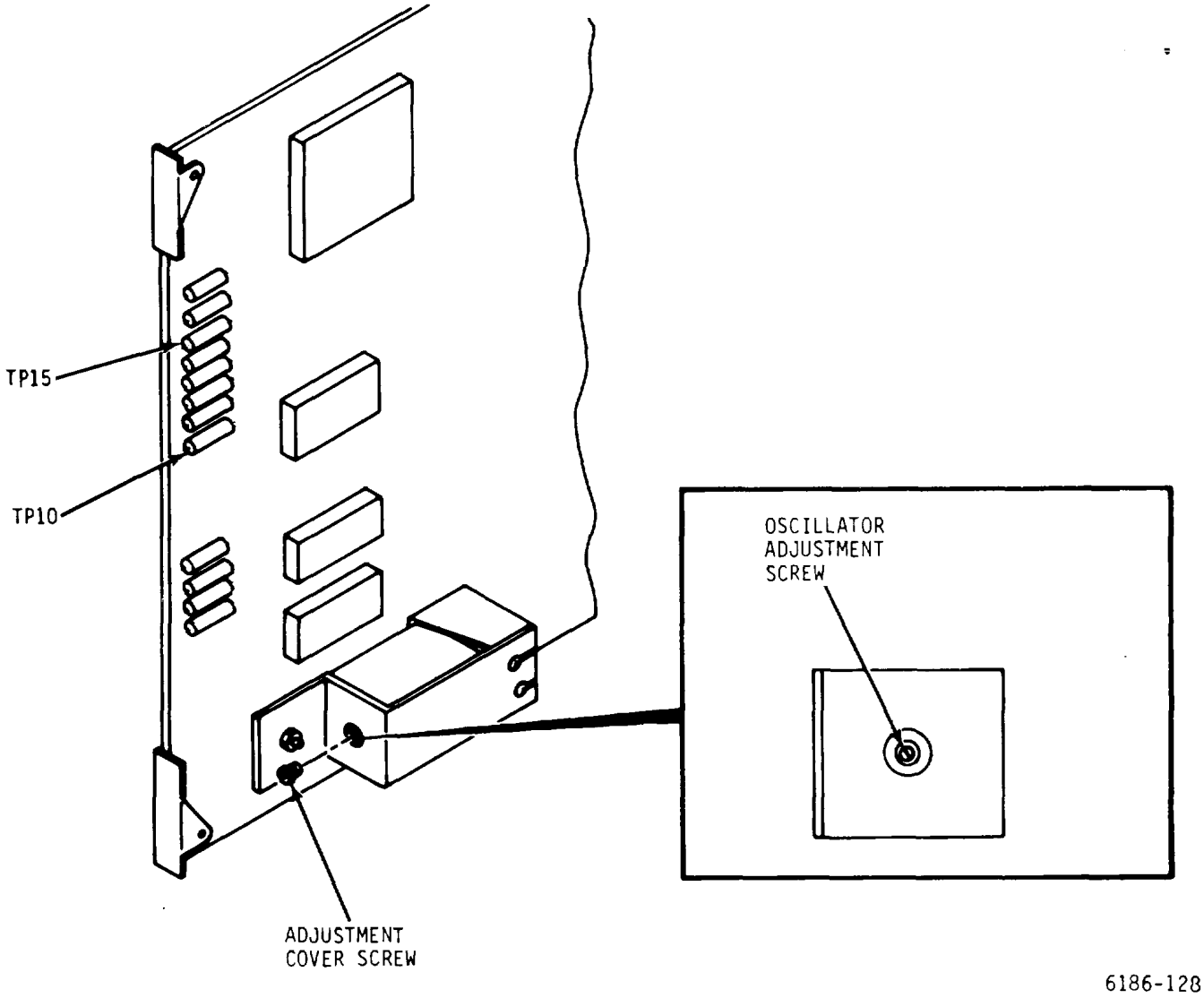

Figure 6-8. RT Card - Test Point and Alignment Location Diagram

NOTE

If the transition encoder/timing recover (TE/TR) assem-bly oscillators are to be calibrated at this time, the printed circuit card access cover may be left off.

6-35. TE/TR CARD CALIBRATION. Calibration of the TE/TR card is performed to ensure that the frequency of the timing recovery oscillator is within prescribed limits. The calibration is performed, using a Hewlett-Packard Model 5245M frequency counter. Perform calibration procedures as follows:

NOTE

To ensure proper calibration, allow the frequency counter to warm up for approximately 15 minutes before making frequency measurements.

1. Loosen and remove printed circuit card access cover (figure 6-2) located at front of chassis.

NOTE

Steps 2 through 4 must be repeated for each TE/TR card in slots 1 through 15 of MUX row.

2. Connect frequency counter to test point TP8 of the TE/TR card and measure output frequency of oscillator Y1.

3. Determine that the frequency measured at TP8 is 9.8304 MHz ± 4915 Hz.

4. If the measured frequency is within tolerance and all TE/TR cards have been calibrated, proceed to step 5. If the measured frequency is not within tolerance on a given TE/TR card, replace the card as prescribed in paragraph 6-22 and repeat steps 2 through 4 for the replaced card.

5. Install and tighten printed circuit card access cover.

NOTE

If the cooling air filter is to be cleaned at this time, the printed circuit card access cover may be left off.

6-36. COOLING AIR FILTER CLEANING. The cooling air filters located on the printed circuit card access cover (figure 6-2) will be cleaned monthly to ensure a free flow of air through the multiplexer set. Perform cleaning procedures as follows:

1. Loosen and remove printed circuit card access cover (figure 6-2) located at front of chassis.

2. From reverse (inner) side of cover, dislodge and remove any dust and foreign matter from the filters, using a low-pressure stream of compressed air.

NOTE

If dust and foreign matter cannot be removed with compressed air, the entire access cover assembly may be carefully cleaned by immersing it in a mild solution of soap and water. If cleaned with soap and water, ensure that the entire cover assembly is thoroughly dried before installing it on the multiplexer set chassis.

3. Install and tighten printed circuit card access cover.

6-37. INSPECTION. Visual inspection of the multiplexer set is performed to detect faulty wiring and general degradation of protective finishes. Perform inspection procedures as follows:

1. Visually examine exposed painted surfaces of multiplexer set chassis for evidence of chipped or scratched paint.

2. If damage to painted surface is evident, refer to paragraph 6-29 for corrective maintenance instructions.

NOTE

Extension of the multiplexer set upon its mounting slides solely for purposes of inspecting the cabling is not recommended. If the cabling is not readily visible with the equipment in its normally installed position, it is recommended that inspection of the cables be postponed until the equipment is extended for corrective maintenance or other reasons.

3. If a multiplexer set is installed so that the input/output cabling is readily visible, carefully inspect all cables for evidence of insulation deterioration due to aging, fraying, severe bending or flexing, or other such causes.

4. If cabling or connector damage is observed, refer to paragraph 6-65 for corrective maintenance instructions.

6-38. PERFORMANCE STANDARDS

6-39. GENERAL. The tests in the following paragraphs are performed for purposes of checking that the multipelxer set is operating properly. The tests include self-testing and lamp testing, a voice processing performance test, and a bit count integrity (BCI) test. The tests may be performed with the multiplexer set in its normally installed position or in a maintenance shop. Testing should be performed following major multiplexer set repairs and whenever improper operation is suspected.

6-40. SELF-TESTING AND LAMP TESTING. Perform self-testing and lamp testing of the multiplexer set as prescribed in paragraphs 6-32 and 6-33, respectively.

6-41. VOICE PROCESSING PERFORMANCE TEST. Perform a voice processing performance test as follows:

NOTE

Testing of voice processing performance requires that the multiplexer set be set up in a full duplex configuration. Refer to chapter 3 for setup instructions
.

1. Connect cables between multiplexer MUX DATA OUT and demultiplexer DEMUX DATA IN connectors, and between multiplexer MUX TIMING OUT and demultiplexer DEMUX TIMING IN connectors (figure 6-9).

NOTE

The test setup cables required for these procedures are identified in figure 6-10.

2. If testing is performed in a shop area, connect multiplexer set to a source meeting the power requirements specified in table 1-1.

3. Set POWER CONTROL switch to .ON.

4. Momentarily press DISPLAY RESET switch.

5. Observe that POWER CONTROL ON indicator is lighted and the following indicators are out:

LOSS OF MUX TIMING

LOSS OF DEMUX TIMING

LOSS OF FRAME A

LOSS OF FRAME B

LINK ERROR RATE

POWER SUPPLY

TEMPERATURE

MULTIPLEXER CARD

DEMULTIPLEXER CARD

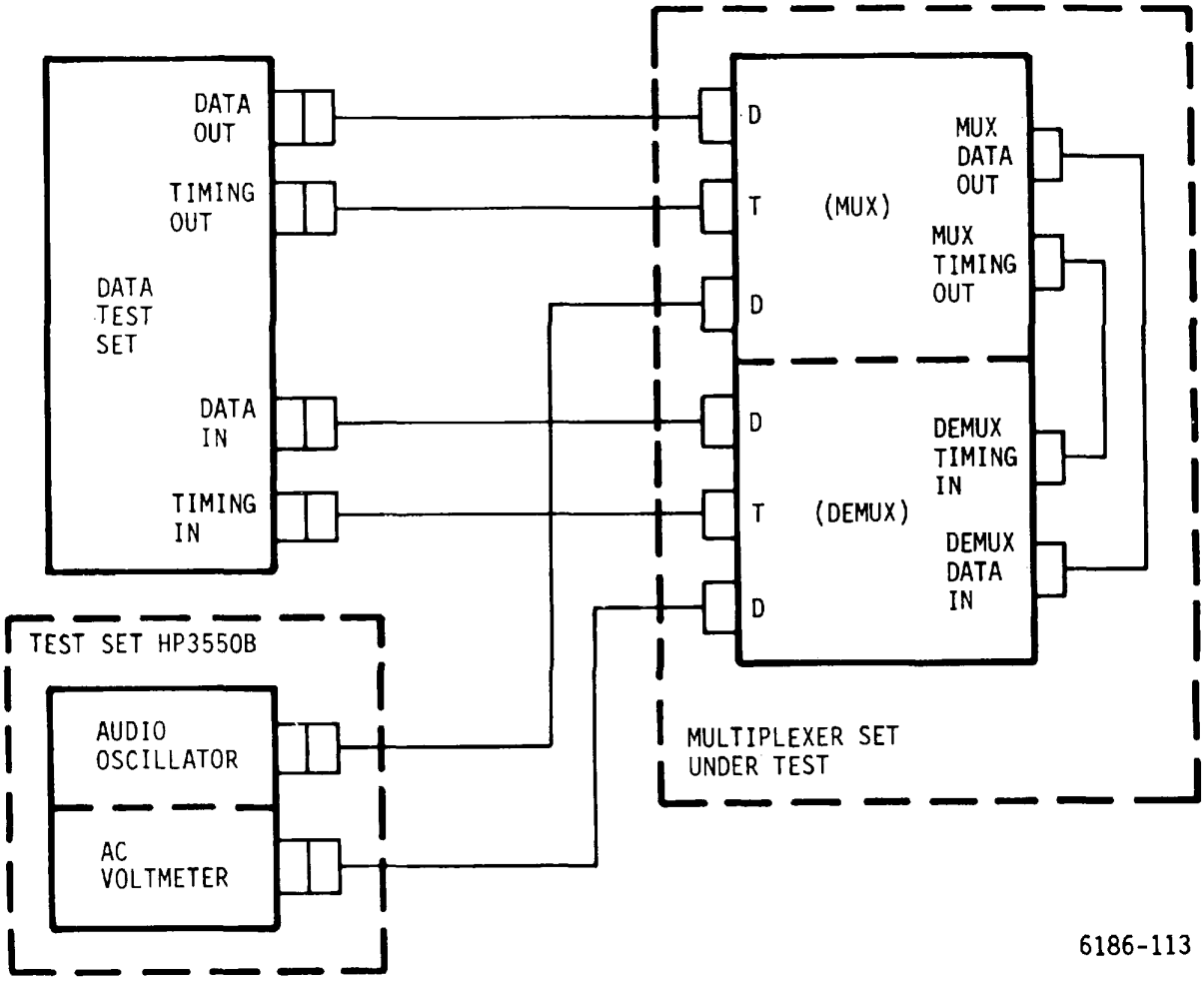

Figure 6-9. Typical Performance Test Setup Diagram

NOTE

At very low multiplexer output rates (R_o), the time for initial frame synchronization by the demultiplexer may approach 6 minutes. Also, it may be necessary to momentarily press the DISPLAY RESET switch to extinguish the LOSS OF FRAME B indicator following initial frame acquisition by the demultiplexer.

6. For the voice channel, involving a pair of VE and VD cards, to be tested (figure 6-9), connect audio oscillator output to multiplexer channel D (data) input connector on the connector panel. Connect the voltmeter input to the channel's demultiplexer D (data) output.

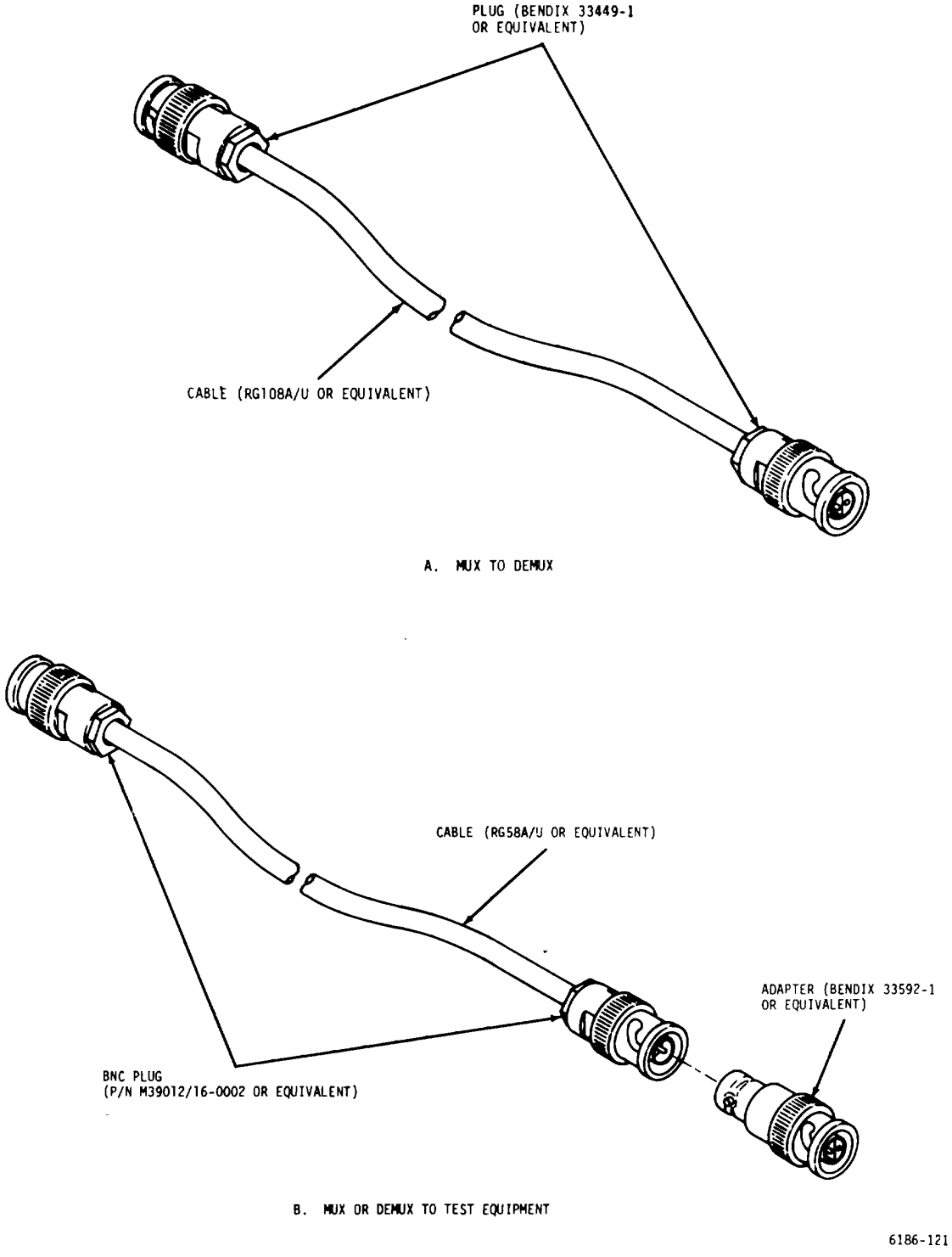

Figure 6-10. Test Setup Cable Diagram

NOTE

The audio oscillator and voltmeter used in the following procedures are Hewlett-Packard Models 204C (option 25) and 403B (option 001), respectively, configured as part of the Hewlett-Packard Model 3550B portable test set. Equivalent items may be substituted. Voice channel input/output impedance is 600 ohms (balanced).

7. Set audio oscillator output frequency to 1000 Hz ±5 percent.

8. Set audio oscillator output level to -16 ±0.1 dBm.

9. Measure audio voltage amplitude appearing at the channel's demultiplexer output. Amplitude should be +7 ±0.1 dBm.

10. Repeat steps 6 through 9 for each voice channel being tested.

11. Set POWER CONTROL switch to OFF and disconnect all test setup cables.

6-42. BIT COUNT INTEGRITY TEST. Perform digital channel bit count integrity (BCI) test as follows:

NOTE

Testing of the BCI requires that the multiplexer set be set up in a full duplex configuration. Refer to chapter 3 for setup instructions.

1. Connect cables between multiplexer MUX DATA OUT and demultiplexer DEMUX DATA IN connectors, and between multiplexer MUX TIMING OUT and demultiplexer DEMUX TIMING IN connectors (figure 6-9).

NOTE

Cable requirements are identified in figure 6-10.

2. If testing is performed in a shop area, connect multiplexer set to a source meeting the power requirements specified in table 1-1.

3. Set POWER CONTROL switch to ON.

4. Momentarily press DISPLAY RESET switch.

5. Observe that POWER CONTROL ON indicator is lighted and the following indicators are out:

LOSS OF MUX TIMING

LOSS OF DEMUX TIMING

LOSS OF FRAME A

LOSS OF FRAME B

LINK ERROR RATE

POWER SUPPLY

TEMPERATURE

MULTIPLEXER CARD

DEMULTIPLEXER CARD

NOTE

- **At very low multiplexer output rates (Ro), the time for initial frame synchronization by the demultiplexer may approach 6 minutes. Also, it may be necessary to momentarily press the DISPLAY RESET switch to extinguish the LOSS OF FRAME B indicator following initial frame acquisition by the demultiplexer.**

- **If the digital channel being tested is configured with a TE/TR card, the timing cable is not required. Cable requirements are identified in figure 6-10.**

- **The Harris Model 7003 Digital Communications Test Set or any other equivalent data test set that is available may be used for digital channel BCI testing. The selected data test set must satisfy the multiplexer input/output interface requirements specified in table 1-3, provide pseudorandom data patterns of 23-1 or greater bits in length, and be capable of injecting and detecting data bit errors. Proper test set operation without a timing input accompanying the digital data stream being monitored is also required.**

6. For the digital data channel to be tested, connect timing and data cables between the data test set output and the appropriate channel T (timing) and D (data) multiplexer inputs. Connect timing and data cables between the channel's demultiplexer T (timing) and D (data) outputs and the data test set input (figure 6-9).

7. Set data test set output for an error-free pseudorandom data pattern of 23-1 or greater bits in length.

8. Set data test set output rate to within ± 5 parts per million (ppm) of the channel's designated input rate (R_c).

9. Initiate pseudorandom data pattern and observe that no data bit errors are detected during a period of approximately 1 minute.

10. Set data test set to inject one or more errors in its output data pattern and observe that a corresponding number of errors is measured at the data test set input.

11 Set data test set for an error-free output.

12. If the channel under test is being processed using a multiplexer RCB channel card, set data test set output rate to a value approximately 2500 ppm greater than the channel's designated input rate (R_o). If a TE/TR card is used, proceed to step 15.

13. Observe that front panel MULTIPLEXER OUT OF TOL indicator lights and the number of the channel under test appears in FAULT LOCATION display.

NOTE

There may be several seconds of delay before the MULTIPLEXER OUT OF TOL indicator goes out when step 14 is performed.

14. Repeat step 8 and observe that MULTIPLEXER OUT OF TOL indicator goes out and the number of the channel under test disappears from FAULT LOCATION display.

15. Repeat steps 6 through 14 for each digital channel being tested.

16. Set POWER CONTROL switch to OFF and disconnect all test setup cables.

SECTION II

SPECIAL MAINTENANCE

6-43. INTRODUCTION.

6-44. This section provides instructions and data applicable to special and depot maintenance of the multiplexer set. Included are procedures for repair of backplane assembly connectors, and semipermanently mounted chassis mechanical parts. Repair of the power supply and the plug-in cards is performed at a depot facility as prescribed in paragraph 6-48.

6-45. Aside from certain specific areas discussed in this section, special maintenance practices performed on the multiplexer set are consistent with those applicable to other military electronic equipment. Personnel performing special maintenance should have a high degree of familarity with these practices, as well as a thorough understanding of the multiplexer set theory of operation.

6-46. GENERAL.

6-47. Repair of the multiplexer set at the special maintenance level generally entails correction of those malfunctions that are beyond the scope of the organizational and intermediate levels. The tasks include repair of the structural components and electrical connectors in the multiplexer set.

6-48. The testing, troubleshooting, and repair of the 12 plug-in cards and the power supply are performed at a depot facility. The detailed procedures are contained in supplemental manual T.O. 31W2-2GSC24-2-1 which is authorized for depot use only. The detailed instructions for removing and installing the plug-in cards and the power supply are contained in section I of this manual.

6-49. MAINTENANCE SUPPORT EQUIPMENT.

6-50. Table 6-6 lists tools and test equipment required in support of the multiplexer set at the special maintenance level. Brief summaries of pertinent performance characteristics are also provided. Special maintenance support equipment items that are also used at the organizational/intermediate maintenance levels are listed and described in table 6-1. The items listed in table 6-6 are preferred for multiplexer set special maintenance. Items having equivalent (or greater) functional capabilities, however, may be substituted when necessary.

6-51 THROUGH 6-64. DELETED.

6-65. CONNECTOR REPAIR.

6-66. Except for the connectors forming a part of the backplane wiring assembly, the connectors used throughout the multiplexer set are conventional types common in most military electronic equipment. Connectors not associated

Table 6-6. Depot/Special Level Support Equipment (Equivalent equipment is authorized.)

Item	National Stock No./ Part No.	Pertinent Characteristics
Chassis repair kit, consisting of:		
Dolly	ESNA P/N CDFB6	
Dolly	ESNA P/N CDFB8	
Hand insertion tool	Sealectro P/N HT-1	
Handle	ESNA P/N CHM1	
Handle	ESNA P/N CHM2	
Handle	Kaynar P/N KT7200	
Insertion tool	Sealectro P/N B22	
Installation tool	5120-00-169-3003	
Installation tool	Southco P/N 29-47-101-10	
Punch	ESNA P/N CPFA6	
Punch	ESNA P/N CPFA10	
Squeeze tool	Kaynar P/N KT7202-046	
Squeeze tool	Kaynar P/N KT7202-083	
Connector repair kit, consisting of:	Martin Marietta P/N SK63759367	
Crimp tool	5120-00-042-7076	
Crimp tool	5120-00-897-0188	
Extraction tool	5120-00-963-7661	
Extraction tool	ITT Cannon P/N CET-DL-2	
Extraction tool	ITT Cannon P/N CET-12-14	

Table 6-6. Depot/Special Level Support Equipment (Cont)

Item	National Stock No./ Part No.	Pertinent Characteristics
Hand crimp tool Insertion/extration tool	ITT Cannon P/N CCT-DL 5120-00-230-3770	
Digital multimeter: Hewlett-Packard Model 3490A	6625-00-188-3892	a. Measures dc voltages between 0 and ±25 vdc at accuracy of 0.1%. b. Measure ac voltages between 0 and 125 vac ±0.4%.
Distortion Analyzer: Hewlett-Packard Model 331A	----	Measures signal-to-noise ratio greater than -26 dBm below signal level.
Frequency counter: Hewlett-Packard Model 5245M	6625-992-3586	Measures frequency range between 0-50 x 106 Hz. Accuracy of 1 count, ± time base accuracy. Sensitivity is 100 mv rms.
Function generator: Hewlett-Packard Model 3310A	6625-00-466-0586	Generates 38.4 kHz ±3% square wave at 3.0 ±0.lv p/p.
Insulation resistance meter: Hewlett-Packard Model 4329A	6625-00-160-1131	Measures insulation resistance of 10 megohms minimum at 200 vdc.
Multimeter: Triplett Model 630A	6625-553-0251	a. Measures dc voltages between 0 and 6000 vdc at accuracy of ±1.5%. b. Measures ac voltages between 0 and 6000 vac ±3.0%.
Oscilloscope main frame: Tektronix Model R7704A with: Probe: Model P6063A Time base: Model 7B92 Dual vertical amplifier: Model 7A26	6625-00-115-2402	Provides visual display with a vertical bandpass of 150 mHz, with a rise time of 2.0 ns.
Power supply: Hewlett-Packard Model 6205B	6625-00-437-4861	Supplies 0 to ±15 vdc at 0.5 ampere.

Table 6-6. Depot/Special Level Support Equipment (Cont)

Item	National Stock No./ Part No.	Pertinent Characteristics
Power supply test set Martin Marietta P/N 61868300-009	6625-01-012-8779	Item peculiar to the multi- plexer set power supply.
Signal generator: Hewlett-Packard Model 204D	6625-00-489-3732	a. Generates audio fre- quency of 1 kHz ±5% at -16 ±0.1 dBm. b. Output impedance of 600 ohms (balanced).
Subassembly test set Martin Marietta P/N 61868000-009		Item peculiar to multi- plexer printed circuit cards.
Transmission and Noise Meter: Hewlett- Packard Model 3555B	6625-00-255-1083	Measures 1 kHz signals with signal levels of -46 ±0.2 dBm. Also, noise levels of -48 dBm.
Voltmeter: Hewlett- Packard Model 3400A	6625-00-727-4706	Measures audio voltage of +7 +0.1 dBm at frequency of 1 kHz ±5%.
Wattmeter: Weston Model 432	Weston P/N 432-9902005	a. Measures power levels between 0 and 1500watts ±0.5%. b. Operates on single- phase inputs of up to 200 vac.

Pages 6-46 through 6-48, including figures 6-11 through 6-13, deleted.

with the backplane wiring assembly are repaired in accordance with existing depot and special maintenance activity practices. The tools used for such repair are included in the connector repair tool set listed in table 6-6.

6-67. Repair card receptacle connectors located on the backplane wiring assembly by replacing individual contacts as follows:

NOTE

In the following procedures, it is assumed that the backplane wiring assembly has been previously removed from the multiplexer set chassis as prescribed in paragraph 6-76.

1. Select a flat clean work surface, preferably of metal.

2. Position backplane assembly with affected connector supported above work surface on square or rectangular metal bars and with contact tails facing upward as shown in figure 6-14. Use bars whose dimensions will allow a minimum clearance of 1 inch between connector and work surface.

3 Position a small nail set or other tool with a cupped point vertically over tail of connector pin being replaced (figure 6-14).

4. Tap nail set with a mediumweight hammer until contact falls free or, in the case of a power or ground contact, until contact is loosened from its normally installed position.

5. If the contact is retained by a ground bushing in the backplane or voltage bus bar, grasp the tail end of contact with needle-nose pliers and push contact until its engaging end emerges from connector insulator. Then grasp engaging end of contact with the pliers and pull contact from connector.

NOTE

Replacement contacts have slightly larger barbs than the original contacts. The larger barbs compensate for material removed from the insulator cavity during removal of the original contact. The part number of the replacement contact is 030-7311-003.

6. Insert replacement contact tail first into insulator cavity from the engaging side of insulator until contact bottoms in cavity.

CAUTION

When installing a contact, ensure that the holding pressure exerted on the pliers is sufficient to hold the contact securely. If the jaws of the pliers are allowed to slip on the surface of the contact, removal of contact plating may occur.

7. Using needle-nose pliers, grasp tail of contact near its end and pull contact until it is properly located within the insulator. The contact will be felt to snap into place when it is fully seated within the insulator cavity.

6-68. CHASSIS REPAIR.

6-69. GENERAL. The multiplexer set chassis is equipped with items such as captive screws, feed-thru terminals, and clinch nuts, which are installed in a semipermanent manner. Although these items are not intended to be replaced frequently, damage resulting from abnormal transportation, operation, or maintenance practices may necessitate their replacement.

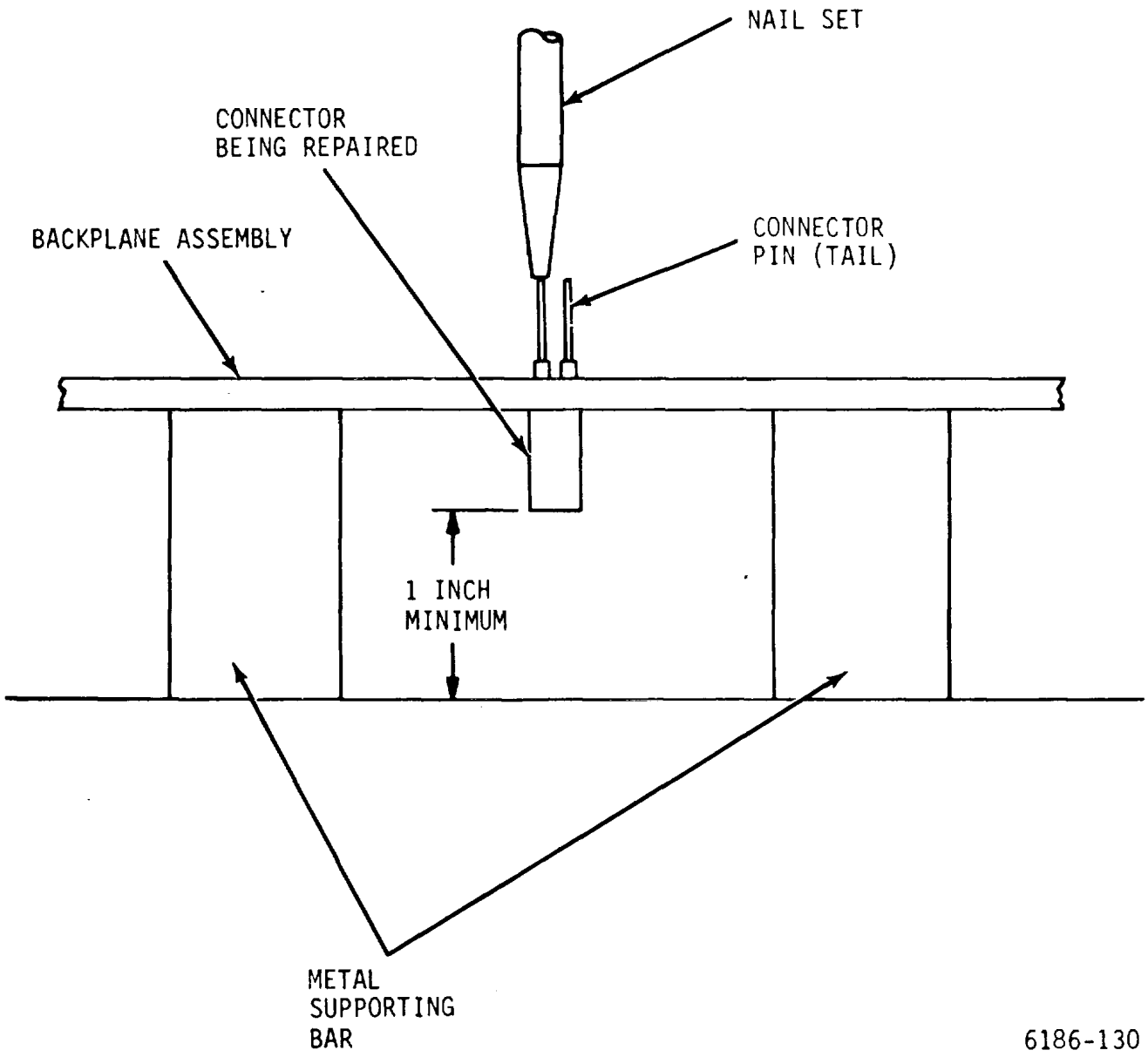

Figure 6-14. Backplane Connector Repair Diagram

The following paragraphs present replacement procedures for semipermanently mounted chassis parts.

6-70. CAPTIVE SCREW REPLACEMENT.

6-71. Captive retaining screws are provided as part of the printed circuit card access cover, the power supply access cover, and the cooling blower panel. Replace captive retaining screws as follows:

1. Place knurled heat of fastener being replaced between opened jaws of a bench vise as shown in figure 6-15.

2. Using a center punch, carefully drive screw portion of fastener

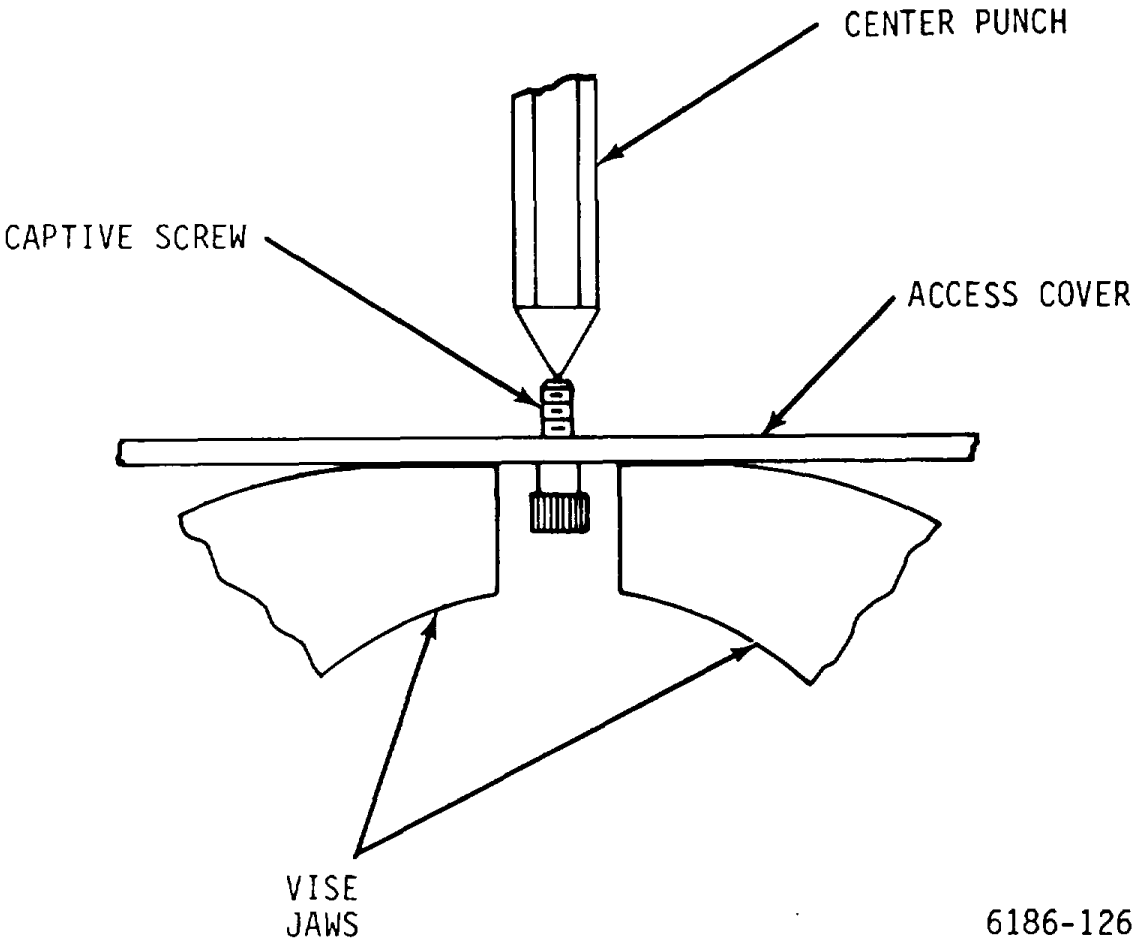

Figure 6-15. Captive Screw Removal Diagram

from access cover. Remove cover from vise.

3. Grasp remaining portion of fastener with slip-joint pliers, and gently rock fastener back and forth until it is released from access cover.

4. Insert replacement fastener through access cover hole (figure 6-16, view B).

5. Draw knob of installation tool P/N 29-47-101-10 (figure 6-16, view A) to open position, and position nose of tool against threaded end of fastener (figure 6-16, view B).

6. Return knob of installation tool to closed position, causing tool to thread onto screw.

7. Lightly squeeze installation tool lever, causing fastener ferrule to flare into countersink in access cover.

8. Draw installation tool knob to open position, causing tool to unthread from installed fastener. A properly installed fastener is shown in figure 6-16, view C

6-72. Replace captive retaining screws attached to the power supply heat sink (figure 6-3) as follows:

1. Place power supply, heat sink down, on a workbench or other suitable flat surface.

2. In a manner similar to that shown in figure 6-15, carefully drive center portion of retaining screw from heat sink.

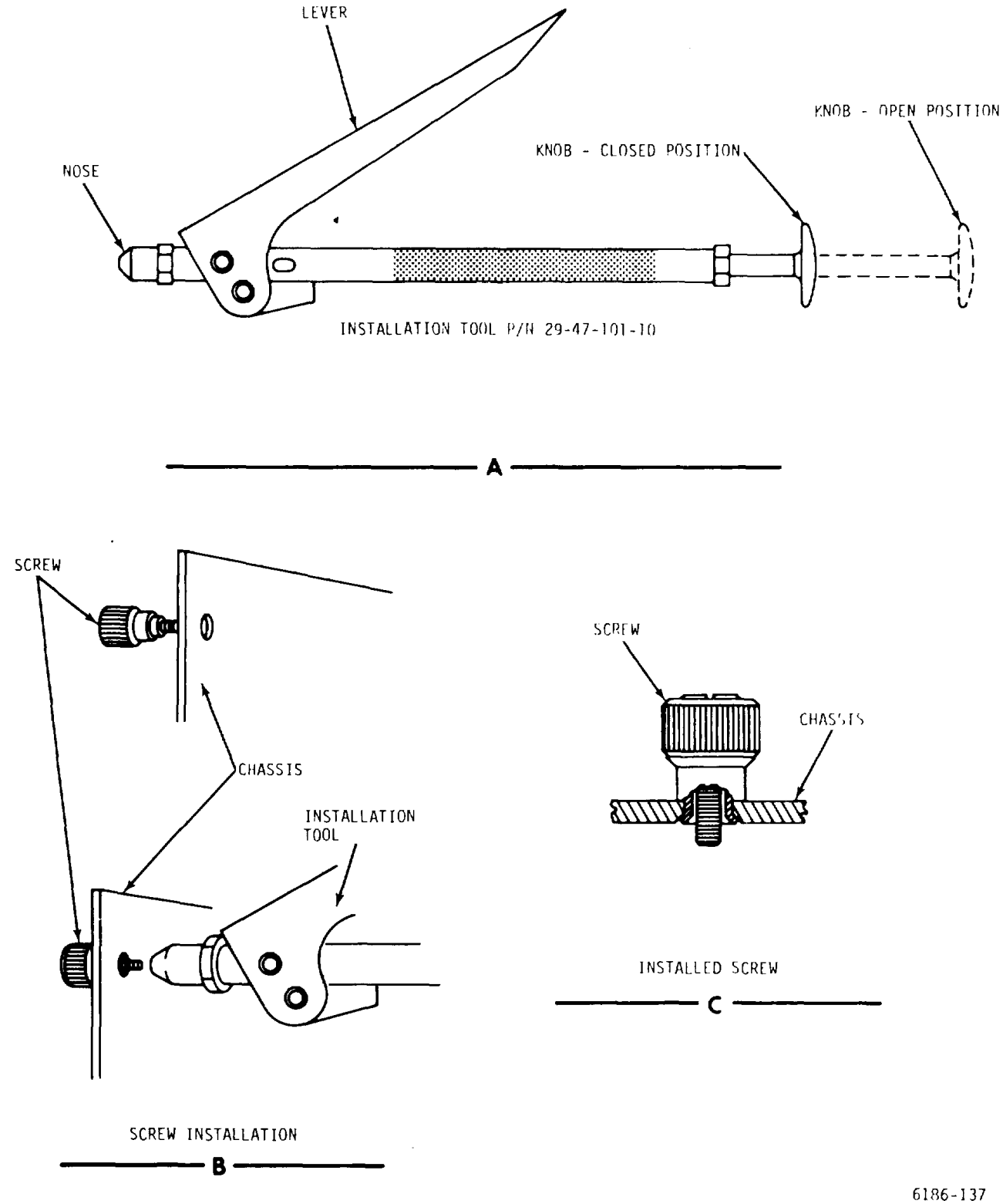

Figure 6-16. Access Cover Captive Screw Insertion Diagram

3. Turn power supply so that heat sink faces up and grasp remaining portion of captive screw with slip-joint pliers.

4. Gently rock remaining portion of captive screw back and forth until it is released from heat sink.

5. Turn power supply on its side and insert replacement captive screw through heat sink hole.

6. Turn threaded portion of screw into installation tool P/N H7503-10 (figure 6-17, view A) by rotating either the screw or the installation tool.

7. Firmly squeeze installation tool handle, causing end of screw ferrule to be swaged against heat sink surface.

8. Unscrew installation tool from installed captive screw. Figure 6-17, view B, shows a captive screw before and after installation

6-73. DELETED.

6-74. STAKE NUT REPLACEMENT. Stake nuts are used within the multiplexer set chassis for purposes of receiving the captive screws that secure the access covers and panel assemblies. Replace stake nuts as follows:

1. Select a drift or pin punch whose diameter will allow it to pass through chassis hole and rest on portion of stake nut swaged into chassis (figure 6-21).

2. Carefully drive stake nut from chassis.

3. Insert replacement nut into chassis hole.

NOTE

Squeeze tool P/N KT7202-046 is used for installing size 6-32 stake nuts, and squeeze tool P/N KT7202-083 is used for installing stake nuts size 8-32 and 10-32 (figure 6-22, view A).

4. Using appropriate size squeeze tool and handle P/N KT7200, carefully drive replacement stake nut into chassis until lands of nut are flush with chassis surface as shown in figure 6-22, view B.

6-75. DELETED.

Pages 6-55 through 6-58, including figures 6-17 through 6-20, deleted.

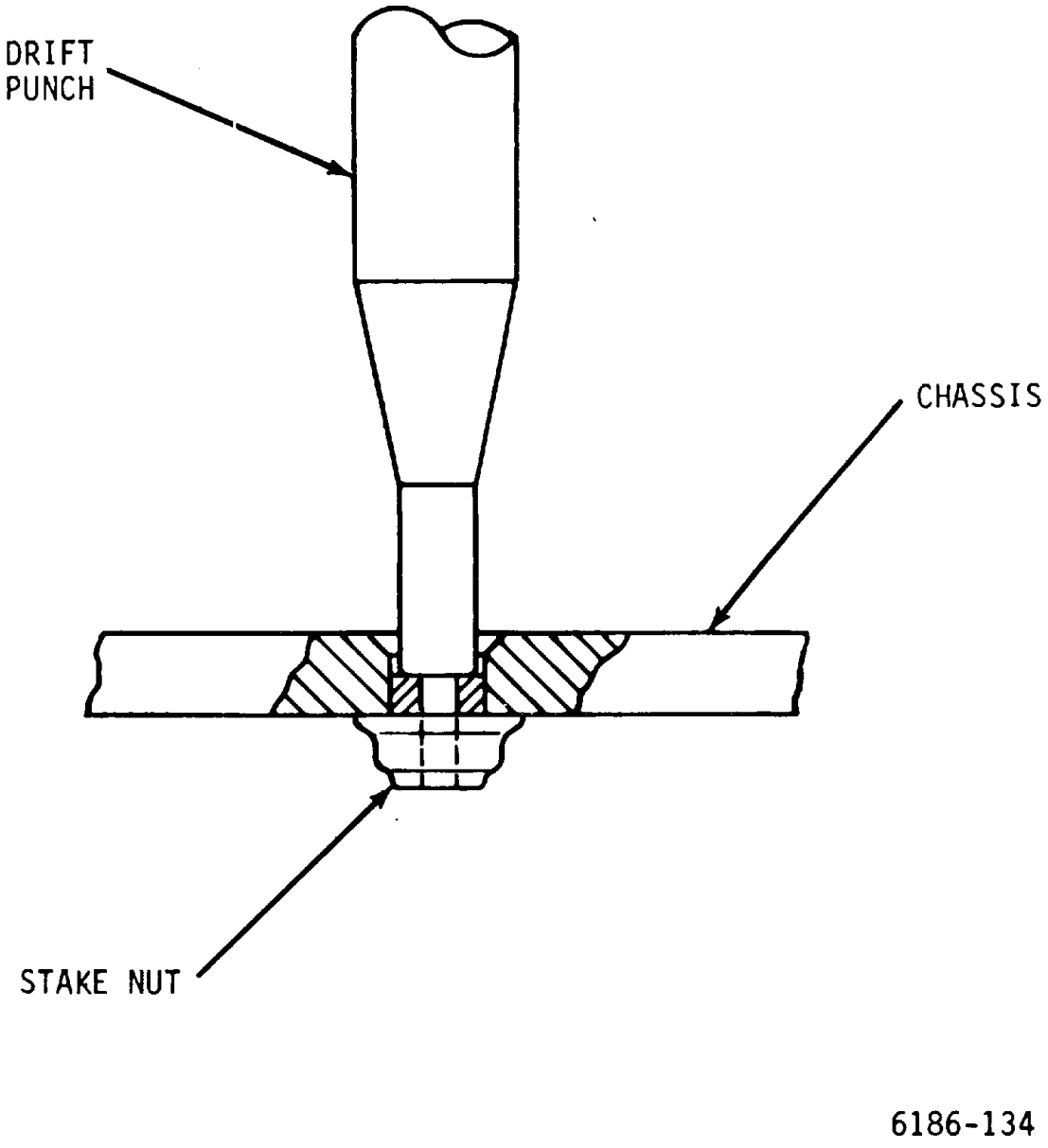

Figure 6-21. Stake Nut Removal Diagram

6-76. BACKPLANE CONNECTOR PANEL REMOVAL AND INSTALLATION. To remove a backplane connector panel, perform the procedures in steps 1 through 9. Perform steps 10 through 12 to install a replacement panel in a chassis. Attaching hardware locations are shown in figure 6-25.

1. Remove printed circuit card access cover (figure 6-2) and printed circuit cards from card file as prescribed in steps1 through 4 in paragraph 6-22. When cards are in card file and the cards are to be placed in the replacement card file, label each card with the proper slot assignment from which the card was removed from the card file to ensure that cards are placed in proper slots.

2. Inside the card file, remove four screws (figure 6-25) securing bottom of card file to chassis, four screws securing top of card file to chassis, and 10 screws securing left side of card file to chassis.

3. Remove rear connector panel and disconnect cable assemblies as prescribed in paragraph 6-28.

4 On rear of card file assembly, remove four screws on left side of chassis frame securing card file assembly to chassis.

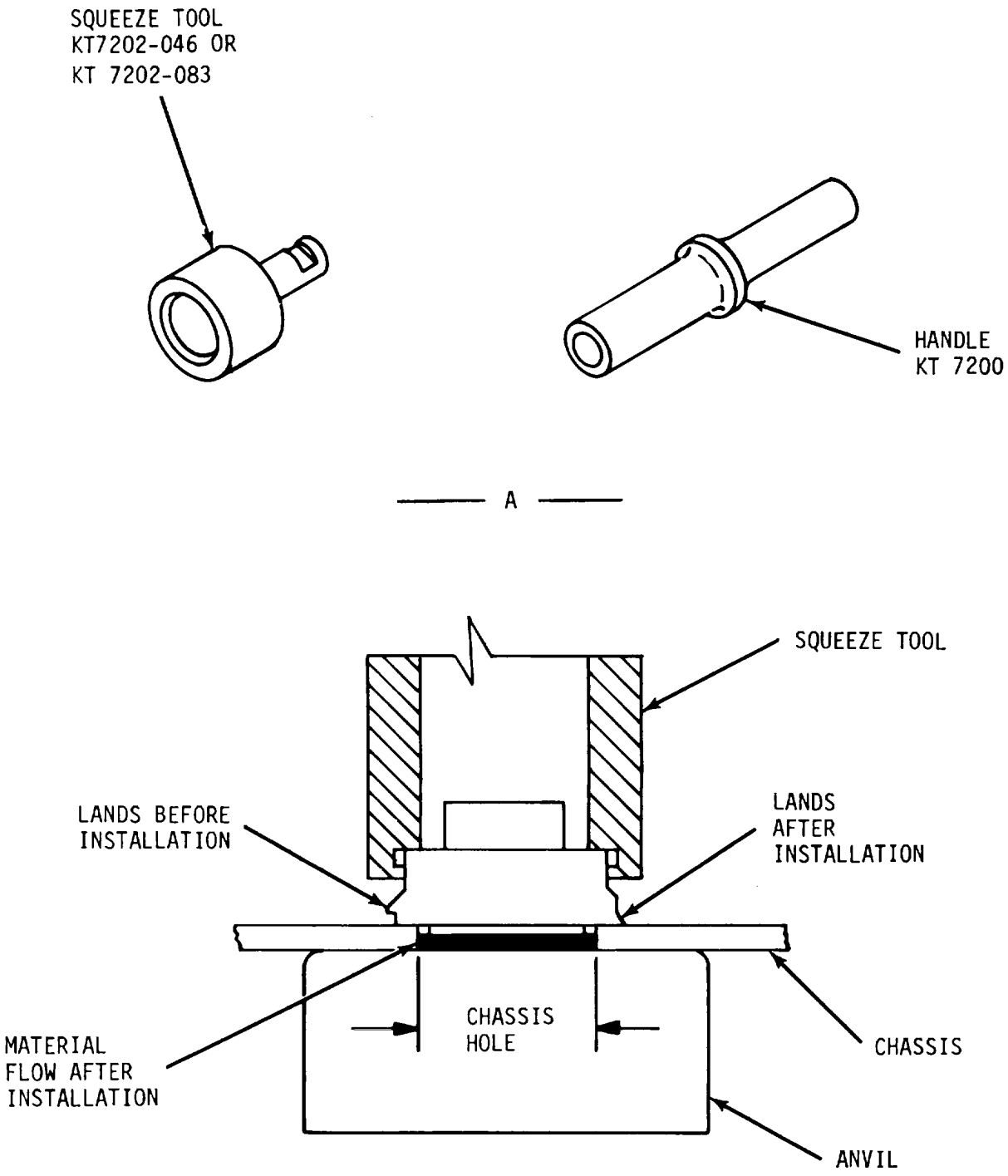

Figure 6-22. Stake Nut Insertion Diagram

Figure 6-23. DELETED.
Figure 6-24. DELETED.

On right side of chassis frame, remove four screws securing card file assembly to chassis.

5. Disconnect power cables from terminals E1, E2, E3, and E4 on backplane panel.

CAUTION

When performing steps 6 and 7, use care to prevent damage or wire breakage of fine wiring on rear of card file.

6. Remove four screws securing capacitor assembly on bottom rear of backplane connector panel to chassis.

CAUTION

When performing step 7, insure that capacitor assembly on rear of backplane connector panel is not subjected to any pressure that could cause damage to the assembly on backplane wiring.

7. Slide card file assembly forward in chassis and then lift from chassis.

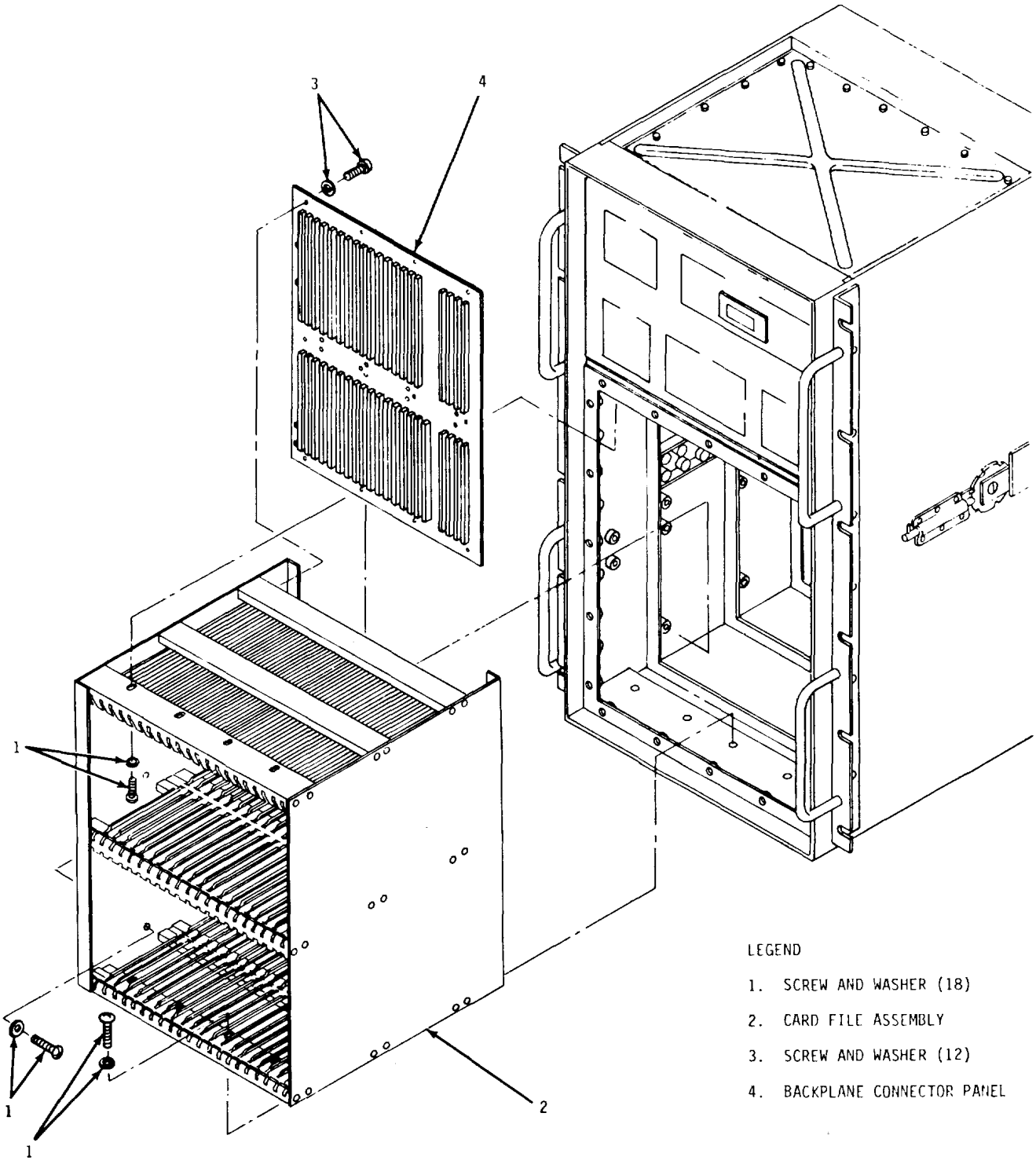

Figure 6-25. Card File - Mounting Hardware Location Diagram

NOTE

Perform steps 8 and 9 to remove and install backplane connector panel on rear of card file. Proceed to step 10 to install replacement card file in chassis when backplane connector panel is not removed from card file.

8. Remove 12 screws securing backplane connector panel to card file. Remove panel from card file.

9. Install replacement backplane connector panel to rear of card file. Secure panel to card file, using 12 screws removed in step 8

When performing step 10, insure that capacitor assembly on rear of backplane connector panel is not subjected to any pressure that could cause damage to the assembly or backplane wiring.

10. To install replacement or repaired backplane connector panel mounted in the card file assembly, slide rear of card file assembly into chassis, and position card file to attach mounting prescribed in step 11.

11. Mount card file to chassis, using screws removed in steps 2 and 4. Install screws removed in step 6 to secure capacitor assembly on rear of backplane connector panel to chassis.

Torque nuts on E1 through E4 on back plane panel down as prescribed in step 12. Otherwise, intermittent operation of equipment may occur.

12. Torque lower level nuts on E1 and E2 between 70 and 75-inch-pounds. Torque lower level nuts on E3 and E4 between 16 and 18 inch-pounds. Install cable terminals on E1 through E4 that were removed in step 5. Then torque upper level nuts on E1 and E2 between 70 and 75 inch-pounds. Torque upper level nuts on E3 and E4 between 16 and 18 inch-pounds.

13. Install rear connector panel and cable assemblies that were removed in step 3 as prescribed in paragraph 6-28.

SECTION III

PERFORMANCE TEST CHECKS

6-77. Multiplexer set performance test checks are applicable to individual power supply assemblies and printed circuit cards and to the overall multiplexer set.

6-78. The performance test checks applicable to the power supply and printed circuit cards are in supplemental manual F.O. 31W2-2GSC24-2-1.

6-79 The performance test checks applicable to the overall multiplexer set include self-testing, lamp testing, voice processing performance tests, and digital channel bit count integrity (BCI) tests. The procedures for these tests are contained in paragraphs 6-32, 6-33, 6-41, and 6-42, respectively.

A

ASYNCHRONOUS - Signals or events which are not synchronous or not of a common period and phase (frequency) relationship one to another.

B

BIT COUNT INTEGRITY - (BCI) - A measure of the multiplexer set's ability to process applied channel data without inducing data errors.

C

CHANNEL - A single subscriber's interface with the multiplexer set.

CHANNEL CARD - See MULTIPLEXER CHANNEL CARD and DEMULTIPLEXER CHANNEL CARD.

CHANNEL DATA RATE - (R_c) - The rate at which channel data enter the multiplexer or leave the demultiplexer.

CHANNEL DATA SAMPLING RATE - (KR_p) The product of the port sampling (R_p) rate and the number (K) of ports assigned to the channel.

COMMON CARD See - MULTIPLEXER COMMON CARD and DEMULTIPLEXER COMMON CARD.

D

DATA SAMPLING RATE See CHANNEL-DATA SAMPLING RATE.

DATA WORD - One multiplexer port scan containing one bit from each used port plus one bit from the overhead port. Maximum length of a data word is 32 bits; the minimum length is 16 bits.

DEMULTIPLEXER CHANNEL CARD - One of four functional printed circuit cards that receives one demultiplexed data channel and processes the data (with or without timing) into the original form in which it was applied to the far end multiplexer.

DEMULTIPLEXER COMMON CARD - One of the five functional printed circuit cards that perform the demultiplexing of the high-speed serial data input stream into the original channel data inputs that are applied to the demultiplexer channel cards.

DIAGNOSTIC CIRCUITS - The multiplexer, demultiplexer, and power supply circuits that detect and signal the occurance of faulty functional circuit operation.

F

FRAME SYNCHRONIZATION - Synchronization of the bit and word format intervals of receiving demultiplexer with those of the transmitting multiplexer.

FUNCTIONAL CIRCUITS - Multiplexer and demultiplexer circuits other than the diagnostic circuits.

M

MAJOR FRAME - A major frame contains 31 minor frames of data. Each minor frame contains channel data, and overhead data pertaining to one of the 31 ports.

MINOR FRAME - A minor frame contains 29 channel data words and overhead data for one port.

MULTIPLEXER CHANNEL CARD One of three functional printed circuit cards that performs the input function of converting incoming asynchronous data for one channel into a synchronous form that is subsequently applied to the multiplexer common cards for multiplexing.

MULTIPLEXER COMMON - CARD One of four functional printed circuit cards that perform the timing functions associated with multiplexing associated channel data inputs of the channel cards into high-speed data output stream.

MULTIPLEXER OUTPUT RATE (R,) The rate at which multiplexed channel and overhead data leave the multiplexer. Maximum value of R_o is 10 MBPS.

N

NEGATIVE STUFF - Overhead function performed in the multiplexer to compensate for a channel data rate (R_c) is less than the multiplexer channel sampling rate (KR_P).

NO ACTION - Overhead function performed in the multiplexer when the channel data rate (R_c) is equal to the multiplexer channel sampling rate (KR_p).

0

OVERHEAD DATA - See OVERHEAD MESSAGE FORMAT.

OVERHEAD MESSAGE FORMAT - The overhead message format consists of one 29bit overhead word. One bit of this word occupies bit zero of the 29 data words in each minor frame.

OUTPUT RATE See MULTIPLEXER OUTPUT RATE.

OVERHEAD WORD See - OVERHEAD MESSAGE FORMAT.

P

PORT - An interval of time during which data from a particular channel are allowed into the output stream in the multiplexer. There are 31 ports available for use by the 1 to 15 channels in a given system application.

PORT SAMPLING RATE - (R_p) The nominal rate at which the porting occurs. See CHANNEL SAMPLING RATE.

PORT STRAPPING - (K) The number of ports assigned to each input/output channel. Value of K is an integer between 1 and 25. See CHANNEL SAMPLING RATE.

POSITIVE STUFF - Overhead function performed in the multiplexer to compensate for a channel data rate (R_c) that is greater than the multiplexer channel sampling rate (KR_p).

STANDARD ERROR ENVIRONMENT - A random error environment of, on the average, one error per hundred bits.

STUFFING - See NEGATIVE STUFF, POSITIVE STUFF, and NO ACTION.

SYNCHRONOUS - Signals or events happening at the same time or having the same period and phase relationship.

SYSTEM CLOCK RATE - The multiplexer internal master timing rate (MRIO or DRIO) equal to the multiplexer output rate (R_o).

T

TANDEMING - The function of inputting one multiplexer with the output of another multiplexer.

U

USED PORT A port that is assigned to a channel.

CROSS-REFERENCE INDEX

A

B

C

D

E

F

G

M

N

O

P

R

S

T

V

CRI-7/CRI-8 blank)

ALPHABETICAL INDEX

A

B

C

D

E

F

G

H

I

L

M

N

O

P

R

S

T

U

V

W

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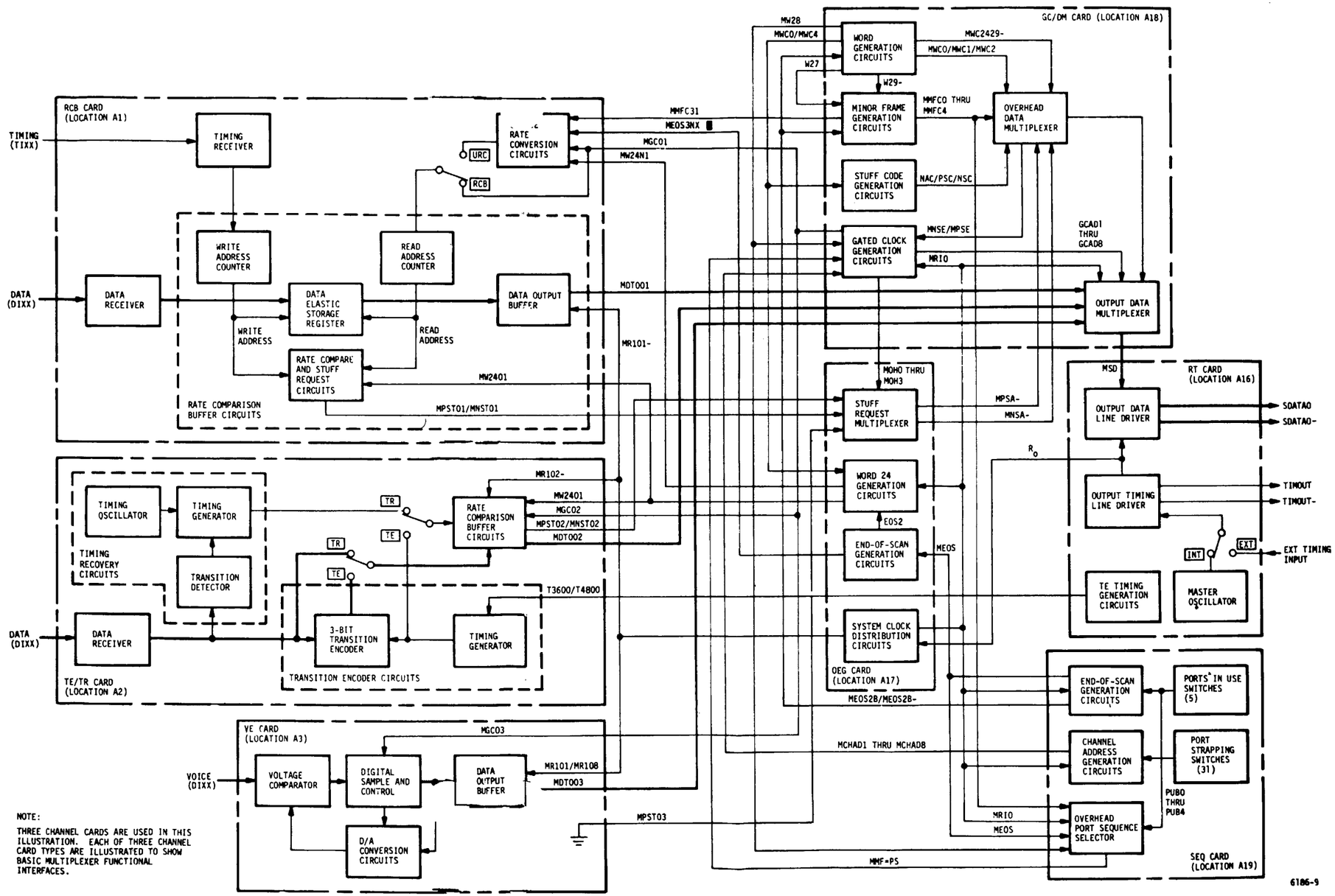


Figure FO-1. Overall Multiplexer System - Block Diagram

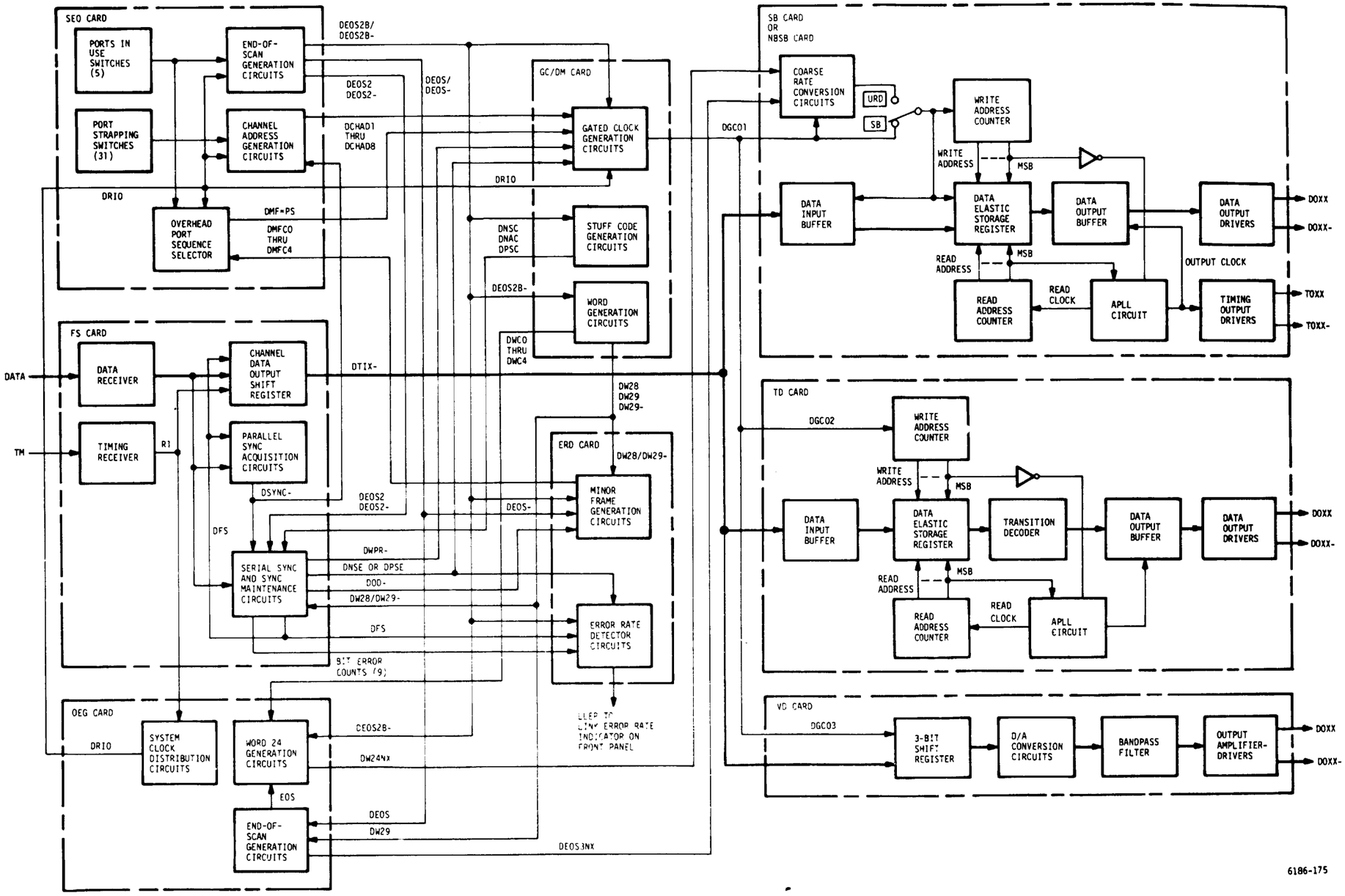


Figure FO-2. Overall Demultiplexer System - Block Diagram

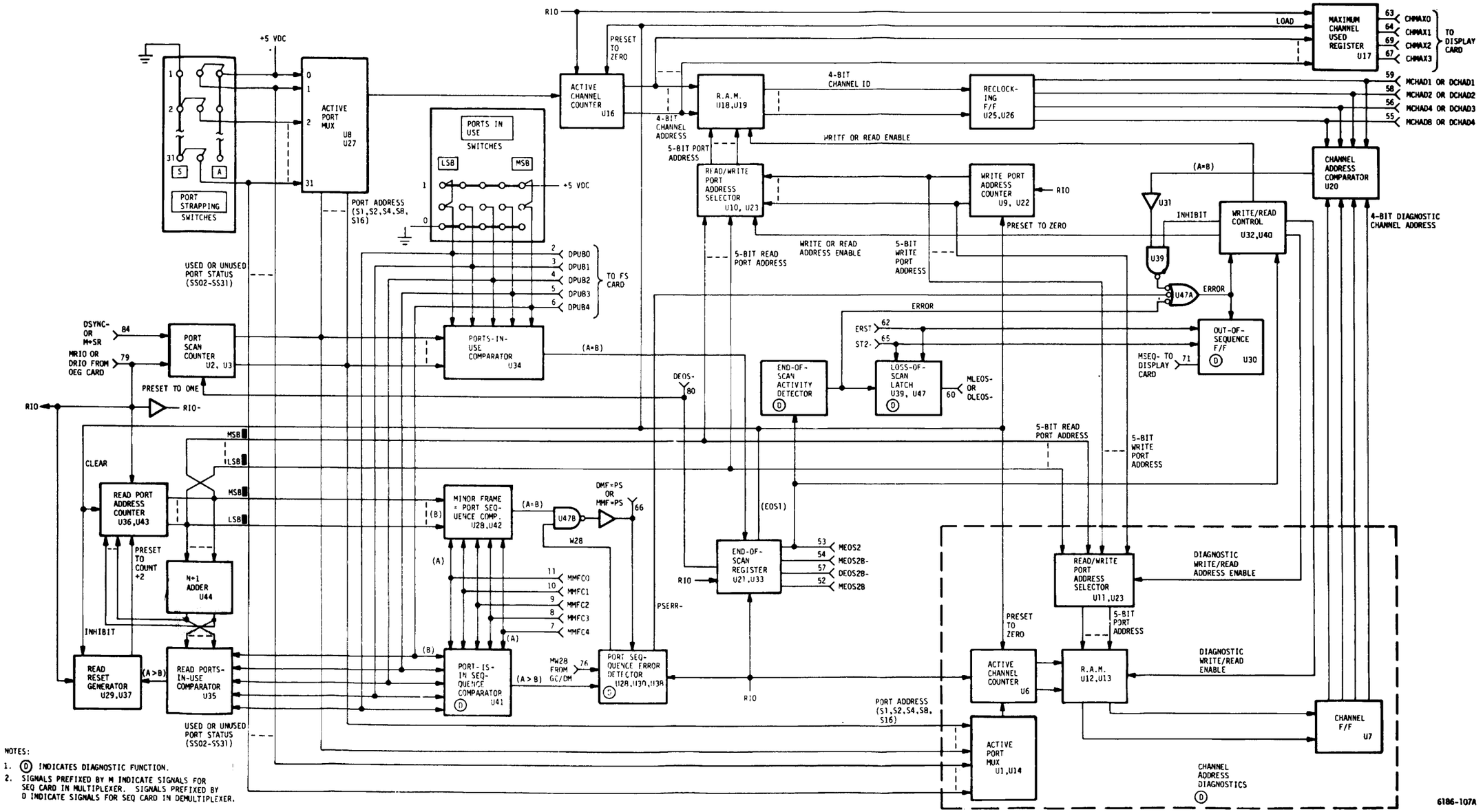


Figure FO-3. Seq Card - Block Diagram

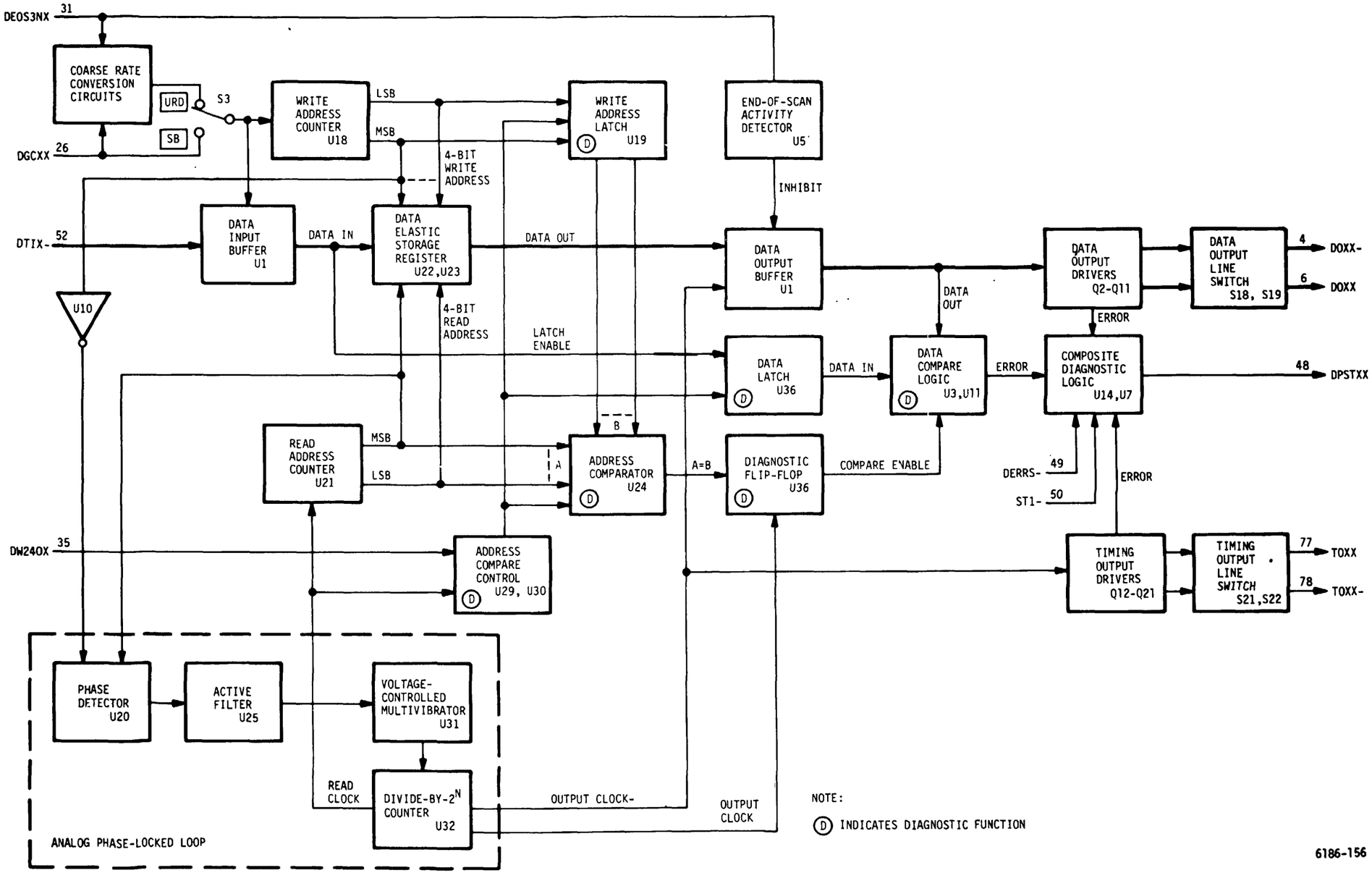
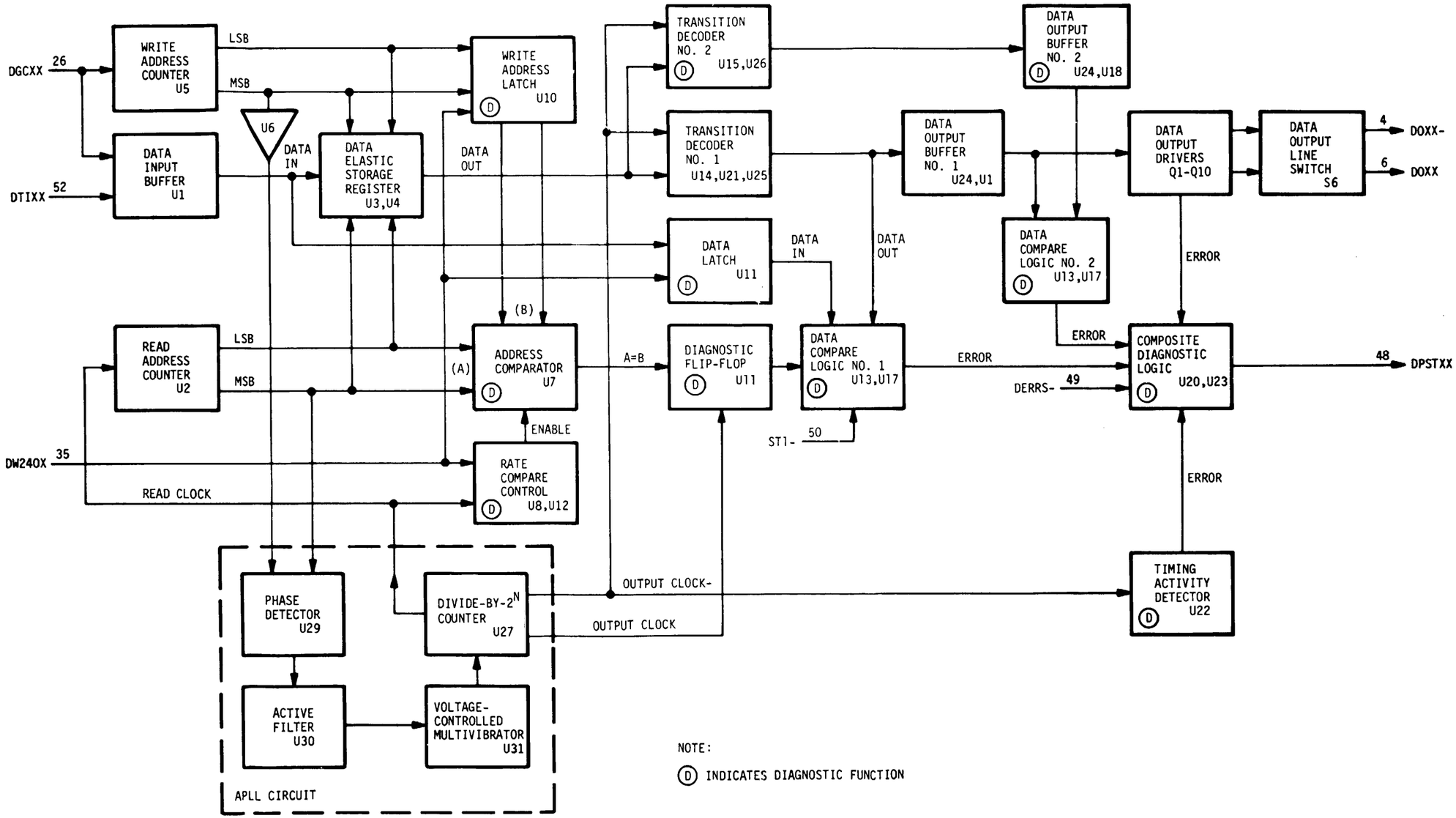
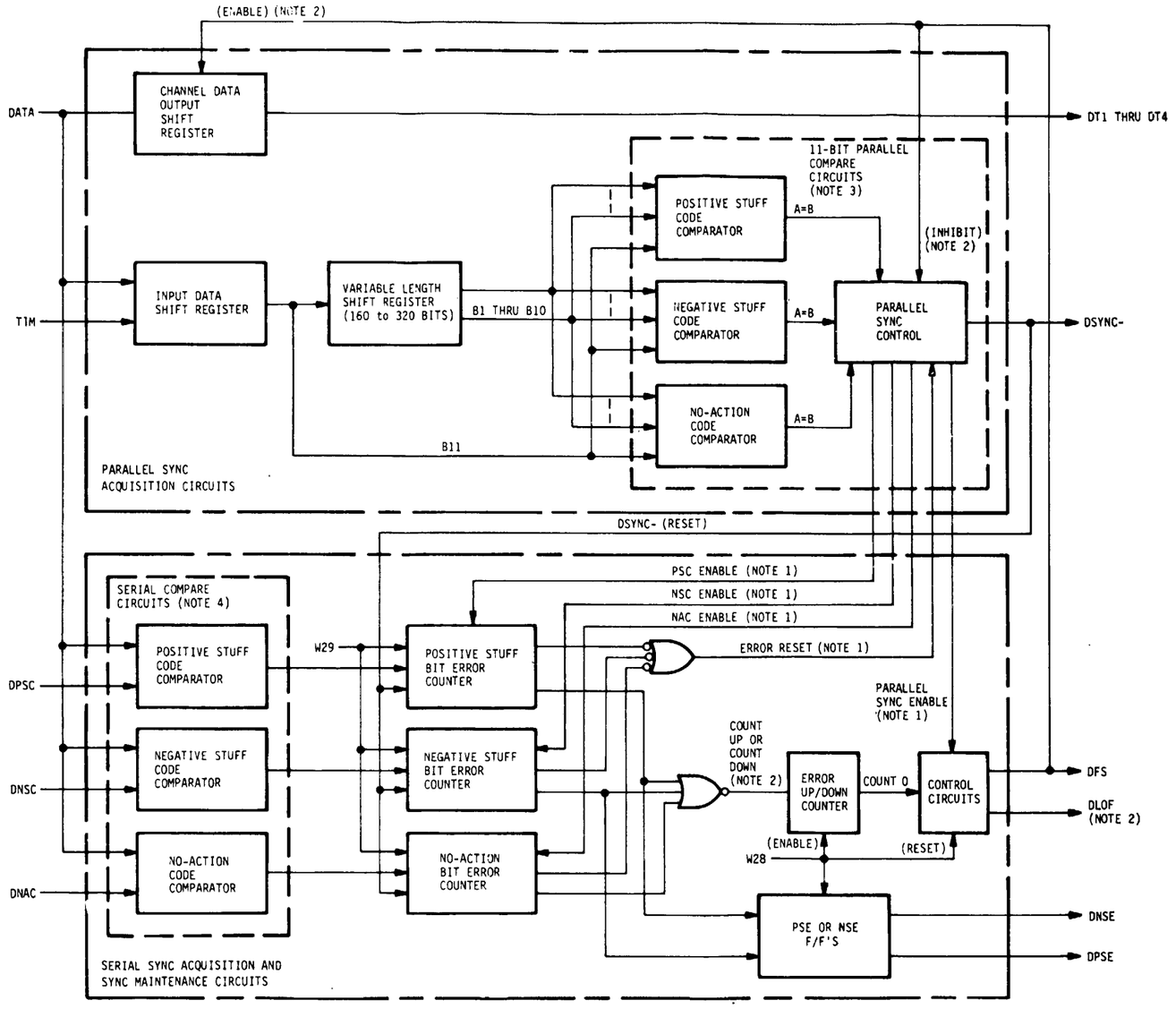


Figure FO-4. SB Card - Block Diagram



6186-157

Figure FO-5. TD Card - Block Diagram



NOTES:

1. PART OF SYNC ACQUISITION FUNCTION.
2. PART OF SYNC MAINTENANCE FUNCTION.
3. B1 THRU B11 COMPARED
4. B12 THROUGH B23 SERIAL COMPARE IN SYNC ACQUISITION FUNCTION. B1 THROUGH B23 SERIAL COMPARE IN SYNC MAINTENANCE FUNCTION.

Figure FO-6. Overall FS Card - Simplified Block Diagram

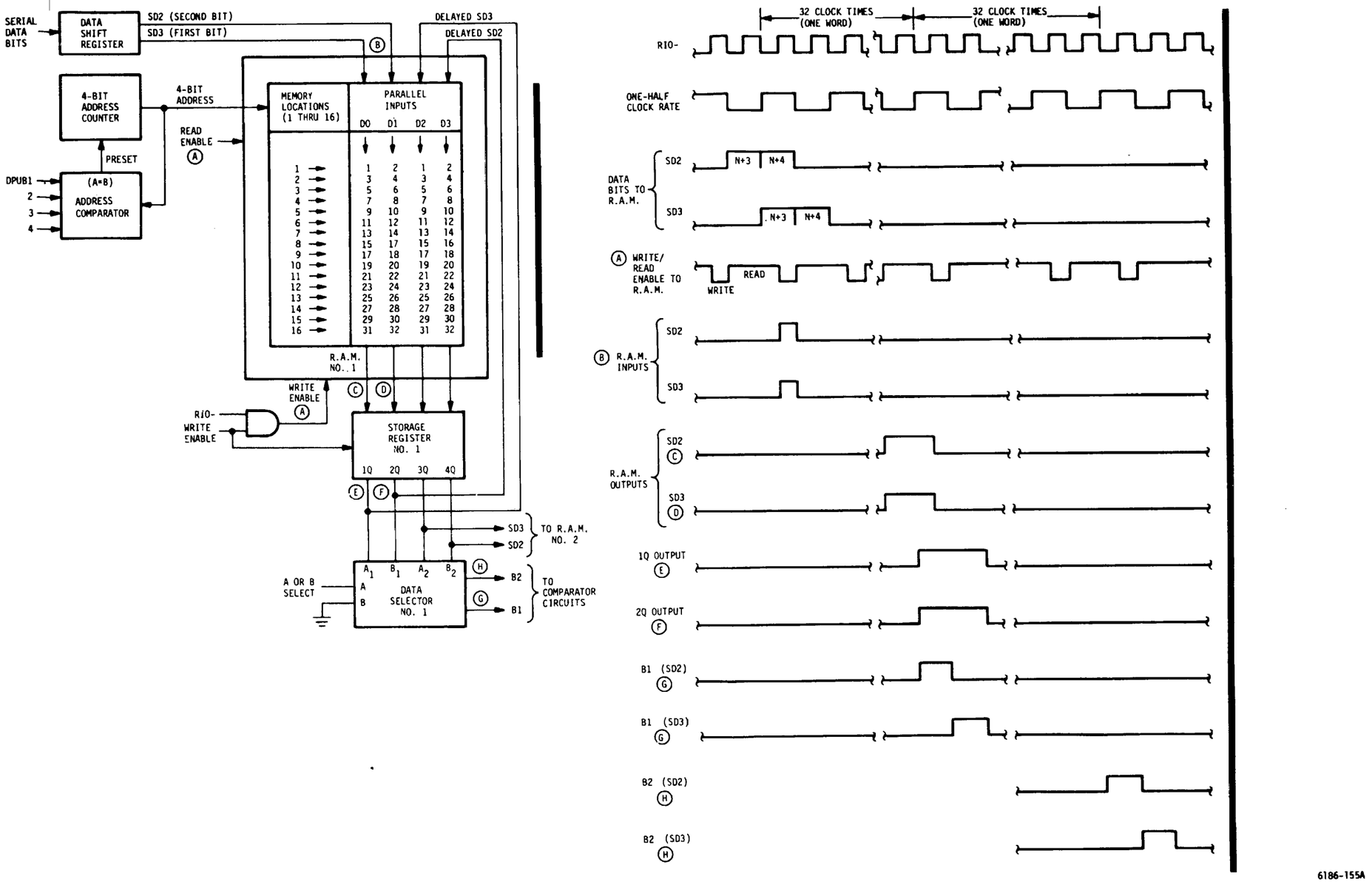
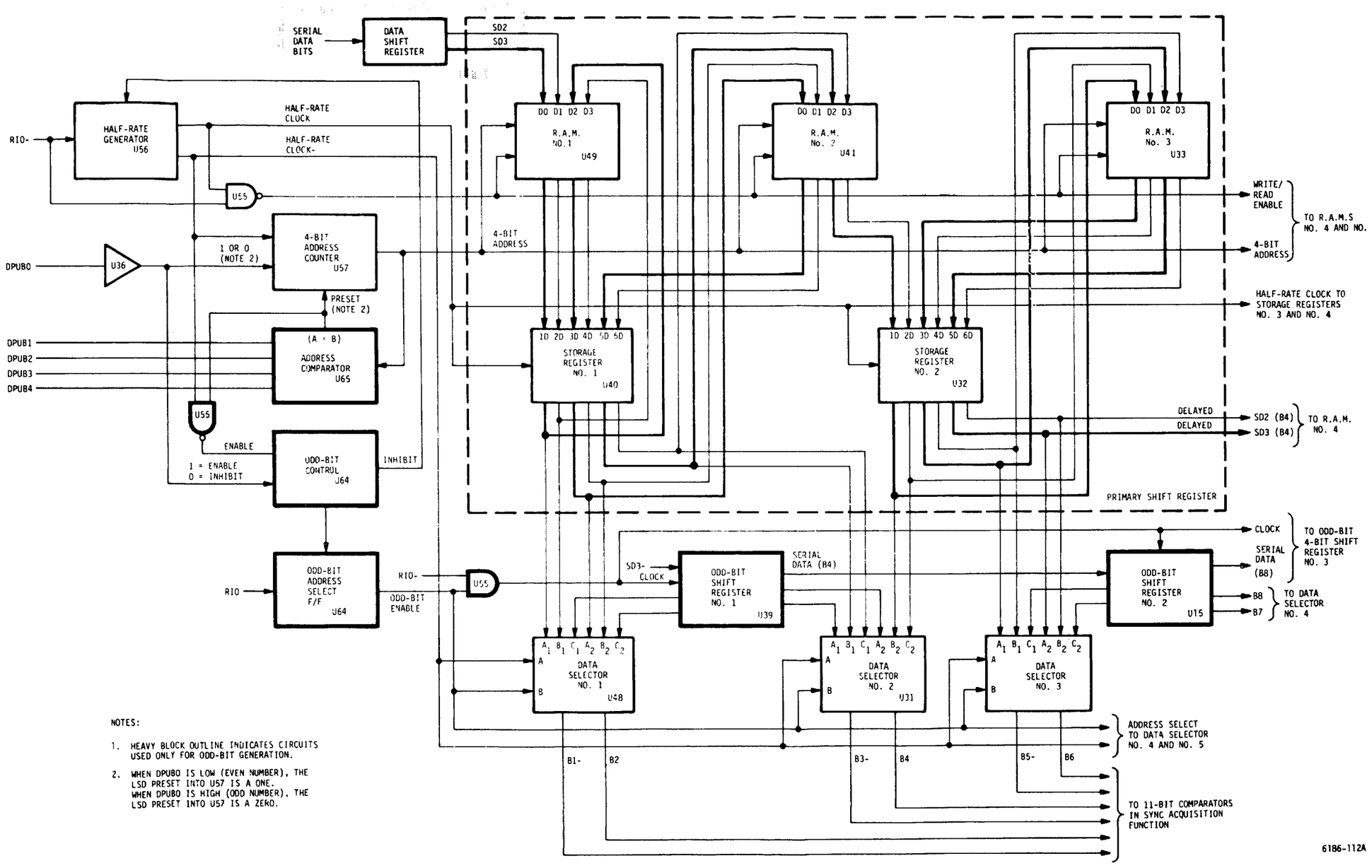


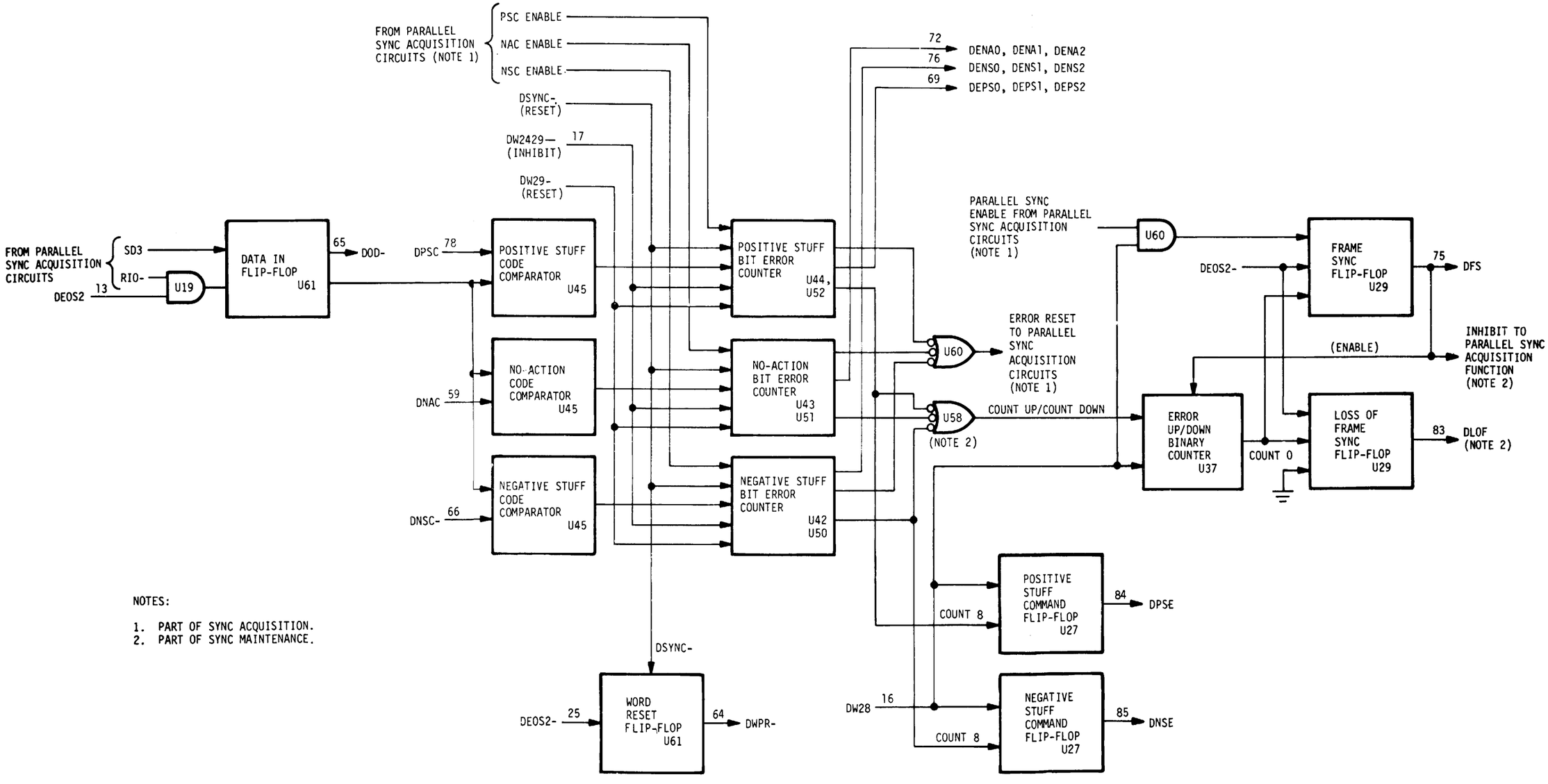
Figure FO-7. FS Card, Primary Shift Register Simplified Block Diagram



NOTES:

1. HEAVY BLOCK OUTLINE INDICATES CIRCUITS USED ONLY FOR ODD-BIT GENERATION.
2. WHEN DPUB0 IS LOW (EVEN NUMBER), THE LSD PRESET INTO U57 IS A ONE. WHEN DPUB0 IS HIGH (ODD NUMBER), THE LSD PRESET INTO U57 IS A ZERO.

Figure FO-8. FS Card, VLSR Circuits Block Diagram



NOTES:

1. PART OF SYNC ACQUISITION.
2. PART OF SYNC MAINTENANCE.

6186-108

Figure FO-9. FS Card, Serial Sync Acquisition and Sync Maintenance Circuits - Block Diagram

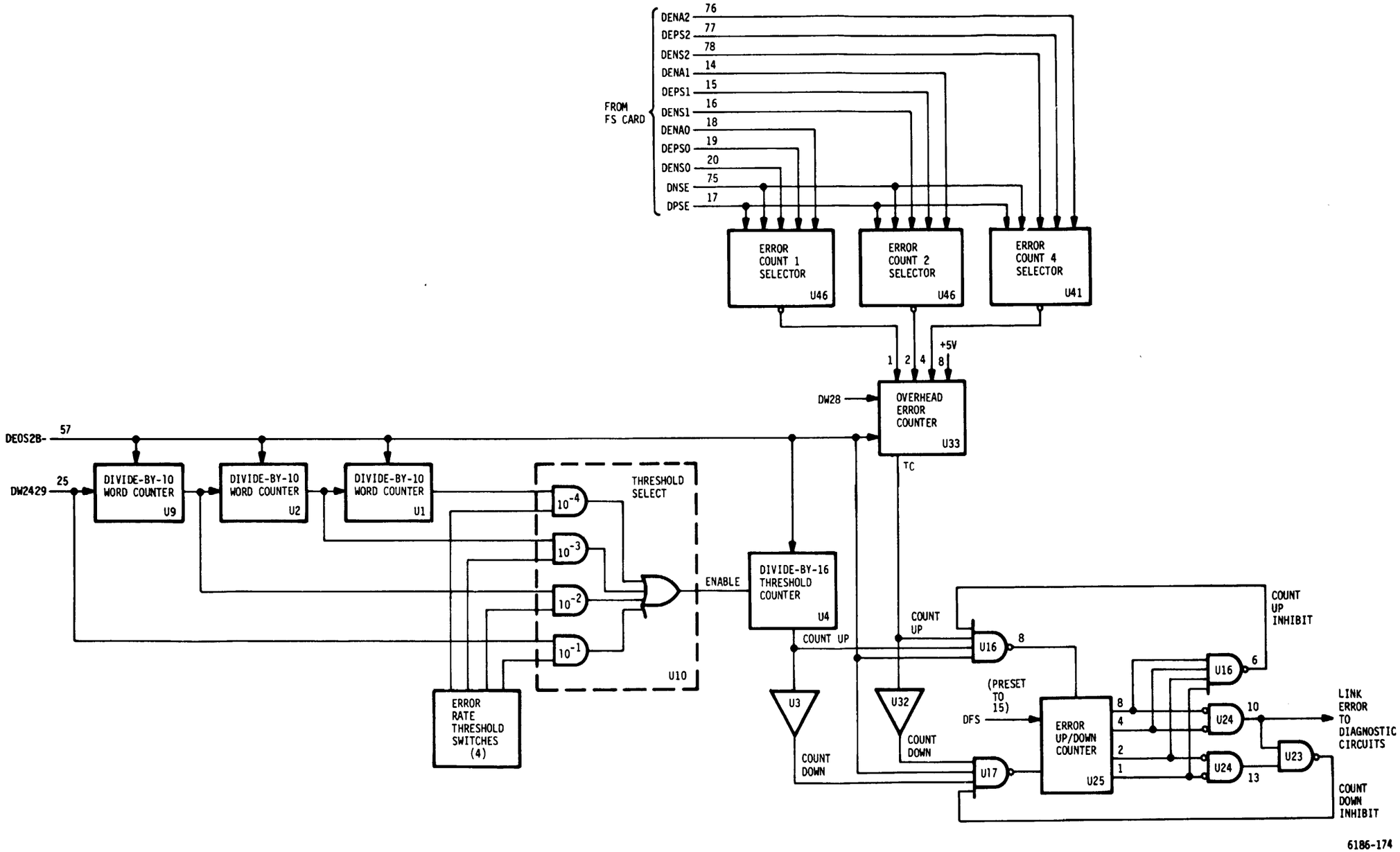


Figure FO-10. ERD Card, Error Rate Detector Circuits - Block Diagram

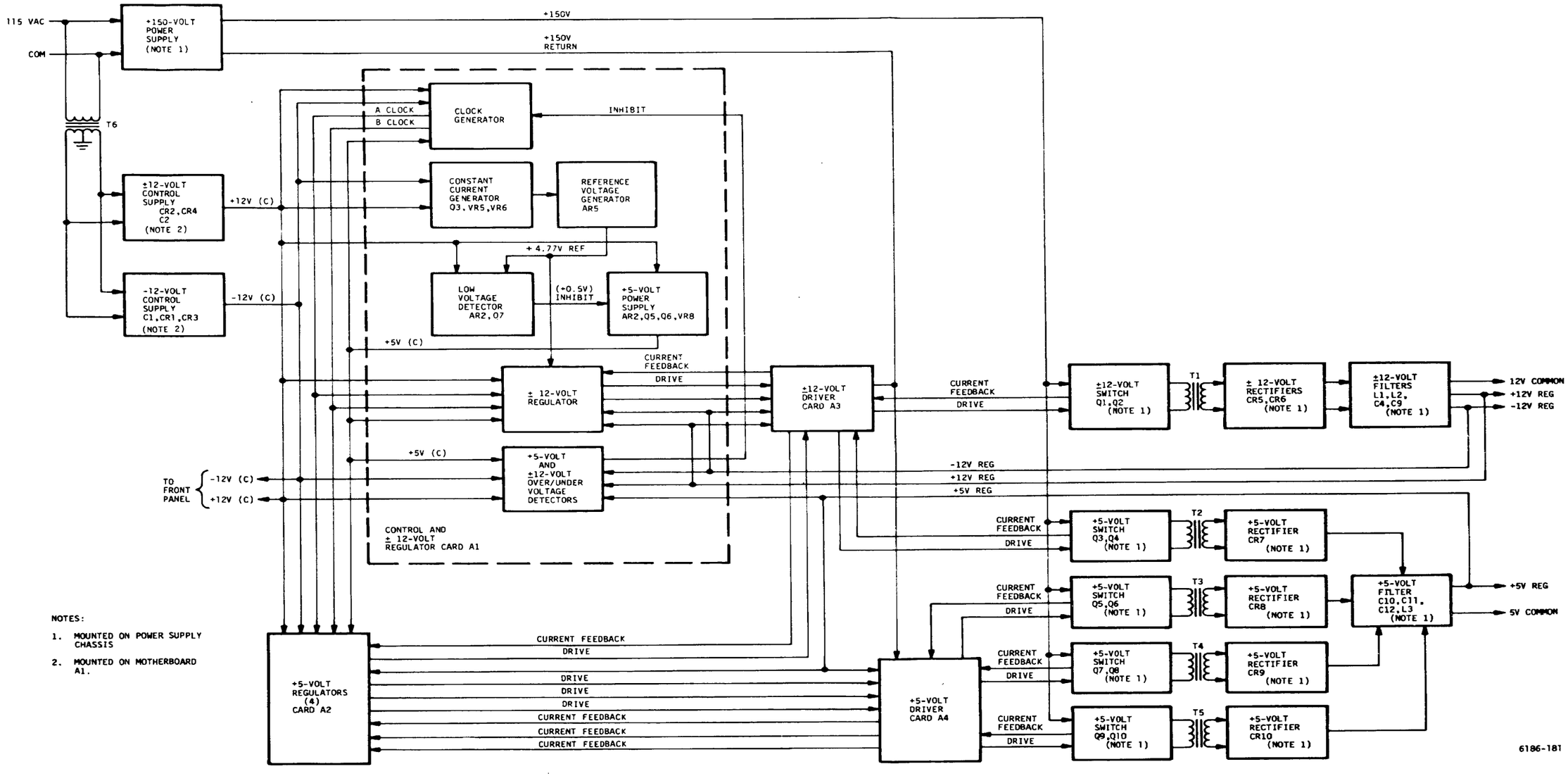


Figure FO-11. Overall Power Supply - Block Diagram

FO-21/ (FO-22 blank)

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